

Digital System design with PLDs and FPGAs - Video course

COURSE OUTLINE

Design: Hierarchy, controller (FSM), case study, meta-stability, synchronization, FSM issues, timing issues, pipelining, resource sharing.

VHDL: Different models, simulation cycles, process, concurrent and sequential statements, loops, delay models, library packages, functions, procedures, synthesis, test bench.

PLD: SPLD and CPLD architecture, timing, applications.

FPGA: Logic block and routing architecture, Virtex-II, Stratix architectures, constraints, STA, case study.

Hardware-software co-simulation, bus function models, SoPC.

COURSE DETAIL

Sl.No.	Topics	No.of Hours
1	Revision of basic Digital systems. <ul style="list-style-type: none"> • Combinational Circuits. • Sequential Circuits. • Timing. • Electrical Characteristics. • Power Dissipation. 	6
2	Current state of the field. <ul style="list-style-type: none"> • SoC, IP Design, SoPC. • Design methodology, System Modeling, Hardware-Software Co-design. • Device Technology. • Application Domains. 	6
3	Digital system Design. <ul style="list-style-type: none"> • Top down Approach to Design, Case study. • Data Path, Control Path. • Controller behavior and Design. • Case study Mealy & Moore Machines. • Timing of sequential circuits. • Pipelining, Resource sharing. 	7



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Electronics & Communication Engineering

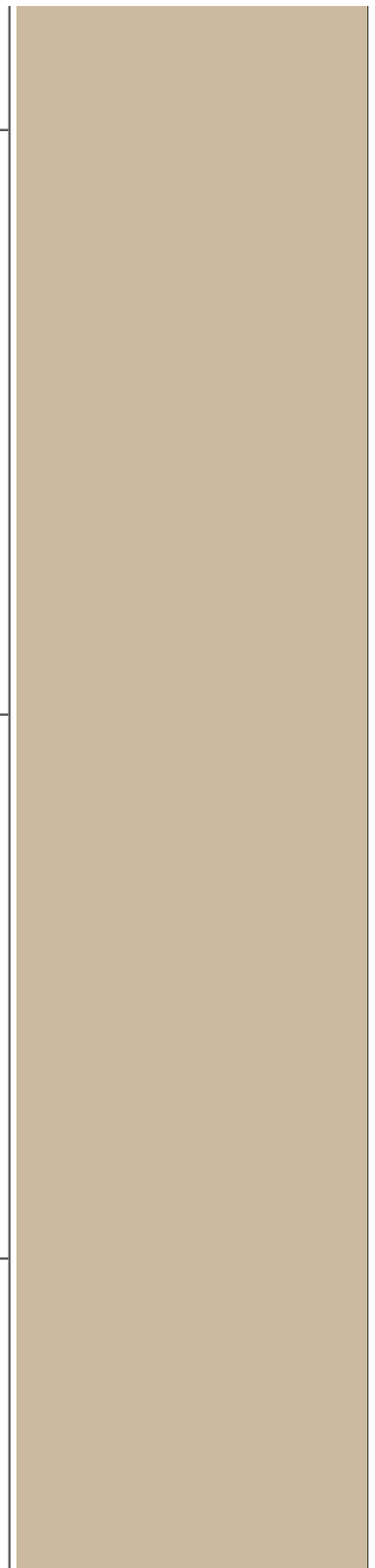
Pre-requisites:

1. Digital circuits.

Coordinators:

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Centre for Electronics Design and Technology IITSc Bangalore

	<ul style="list-style-type: none"> • FSM issues (Starring state, Power on Reset, State diagram optimization, State Assignment, Asynchronous Inputs, Output Races, fault Tolerance ...). 	
4	<p>VHDL for Synthesis.</p> <ul style="list-style-type: none"> • Introduction. • Behavioral, Data flow, Structural Models. • Simulation Cycles. • Process. • Concurrent Statements. • Sequential Statements. • Loops. • Delay Models. • Sequential Circuits, FSM Coding. • Library, Packages. • Functions, Procedures. • Operator Inferencing. • Test bench. 	7
5	<p>Programmable Logic Devices.</p> <ul style="list-style-type: none"> • Introduction. • Evolution: PROM, PLA, PAL. • Architecture of PAL's. • Applications. • Programming PLD's. • Design Flow. • Programmable Interconnections. • Complex PLD's (MAX - 7000, APEX). • Architecture, Resources. • Applications. • Tools. • Demonstration of the tool. 	7
6	<p>DFPGA's.</p> <ul style="list-style-type: none"> • Introduction. • Logic Block Architecture. • Routing Architecture. • Programmable Interconnections. • Design Flow. • Xilinx Virtex-II (Architecture). • Altera Stratix, Actel 54SX Architecture. 	7



	<ul style="list-style-type: none"> • Boundary Scan. • Programming FPGA's. • Constraint Editor, Static Timing Analysis. • One hot encoding. • Applications. • Tools. • Case Study. • Xilinx Virtex II Pro, Embedded System on Programmable Chip. • Hardware-software co-simulation, Bus function models, BFM Simulation. • Debugging FPGA Design, Chipscope Pro. 	
	Total	40

References:

1. Jon F Wakerly, Digital Design: Principles and Practices, Prentice Hall.
2. Kevin Skahil, VHDL for programmable logic, Addison Wesley.
3. Zainalabedin Navabi, VHDL, analysis and modeling of digital systems, McGraw-Hill.
4. PLD, FPGA data sheets.