



DESIGN AND ANALYSIS OF VLSI SUBSYSTEMS

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Engineering
IIIT Bangalore

TYPE OF COURSE : New | Elective | UG/PG

COURSE DURATION : 12 Weeks (24 Jan' 22 - 15 Apr' 22)

EXAM DATE : April 24, 2022

PRE-REQUISITES : Digital Electronics at Undergraduate level.

INTENDED AUDIENCE : Students interested in Digital VLSI

INDUSTRIES APPLICABLE TO : Samsung, Intel, Broadcom, Qualcomm, IBM

A course along similar contents will be taught to Samsung Semiconductor division, Bangalore from August to November, 2021.

COURSE OUTLINE :

The course will introduce students to the topics of Digital CMOS VLSI subsystem design using design metrics of delay, power, and area in detail. The course focuses more on power estimation, and interconnect aware designs and discusses on few power benefits designs. Approximate computing datapath subsystem designs will be analyzed along with the design, and error metrics. Different forms of standard cell design of latch, and flipflops will be discussed and the importance of timing parameters in sequential circuits will be explained.

ABOUT INSTRUCTOR :

Prof. Madhav Rao is an Associate Professor at IIIT-Bangalore. He teaches Digital VLSI Design, VLSI subsystem, Electronic devices and circuits, and basic electronics courses to IIIT-B students. He is a recipient of SERB Early Career Research Award (2014-2017), Visvesvaraya Young Faculty fellowship award (2016-2020), IBM Shared University Research Award (2018-20), 2021 IBM Global University Program Academic Award. He has also completed projects sponsored by MEITY in the past, and is currently involved in the project from MSJE, and GoK, IT-BT center.

COURSE PLAN :

Week 1: Digital CMOS, and Delay estimation

Week 2: Digital CMOS, and Delay estimation (Contd.)

Week 3: Interconnects

Week 4: Interconnects (Contd.)

Week 5: Power

Week 6: Power (Contd)

Week 7: Sequential design

Week 8: Sequential design (Contd)

Week 9: Combinational Circuit families

Week 10: Subsystems

Week 11: Subsystems (Contd)

Week 12: Approximate Computing