DIGITAL VLSI TESTING

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TYPE OF COURSE : Rerun | Core | UG/PG
COURSE DURATION : 12 weeks (20 Jul' 20 - 9 Oct' 20)
EXAM DATE : 17 Oct 2020

PRE-REQUISITES : Digital Design / Digital Logic

INTENDED AUDIENCE : CSE, ECE, EE

INDUSTRIES APPLICABLE TO : Companies involved in development of VLSI chips

COURSE OUTLINE :
Testing is an integral part of the VLSI design cycle. With the advancement in IC technology, designs are becoming more and more complex, making their testing challenging. Testing occupies 60-80% time of the design process. A well structured method for testing needs to be followed to ensure high yield and proper detection of faulty chips after manufacturing. Design for testability (DFT) is a matured domain now, and thus needs to be followed by all the VLSI designers. In this context, the course attempts to expose the students and practitioners to the most recent, yet fundamental, VLSI test principles and DFT architectures in an effort to help them design better quality products that can be reliably manufactured in large quantity.

ABOUT INSTRUCTOR :
Prof. Santanu Chattopadhyay received his PhD from Indian Institute of Technology (IIT) Kharagpur in 1996. He is currently a Professor in the Department of Electronics and Electrical Communication Engineering, IIT Kharagpur. His research interests include Embedded Systems, System-on-Chip (SoC) and Network-on-Chip (NoC) Design and Test, Power- and Thermal-aware Testing of VLSI Circuits and Systems. He has published more than 150 papers in reputed international journals and conferences. He has published several text and reference books in the related areas. He is a senior member of IEEE and an editorial board member of IET Circuits Devices and Systems.

COURSE PLAN :

Week 1**:** Introduction: Importance, Challenges, Levels of abstraction, Fault Models, Advanced issues

Week 2**:** Design for Testability: Introduction, Testability Analysis, DFT Basics, Scan cell design, Scan Architecture

Week 3**:** Design for Testability: Scan design rules, Scan design flow Fault Simulation: Introduction, Simulation models

Week 4**:** Fault Simulation: Logic simulation, Fault simulation

Week 5**:** Test Generation: Introduction, Exhaustive testing, Boolean difference, Basic ATPG algorithms

Week 6**:** Test Generation: ATPG for non stuck-at faults, Other issues in test generation Built-In-Self-Test: Introduction, BIST design rules

Week 7**:** Built-In-Self-Test: Test pattern generation, Output response analysis, Logic BIST architectures

Week 8**:** Test Compression: Introduction, Stimulus compression

Week 9**:** Test Compression: Stimulus compression, Response compression

Week 10**:** Memory Testing: Introduction, RAM fault models, RAM test generation

Week 11**:** Memory Testing: Memory BIST Power and Thermal Aware Test: Importance, Power models, Low power ATPG

Week 12**:** Power and Thermal Aware Test: Low power BIST, Thermal aware techniques