Advanced VLSI Design - Video course

COURSE OUTLINE

Historical Perspective of VLSI, CMOS VLSI Design for Power and Speed consideration, Logical Efforts: Designing Fast CMOS Circuits; Datapath Design, Interconnect aware design, Hardware Description Languages for VLSI Design, FSM Controller/Datapath and Processor Design, VLSI Design Automation, and VLSI Design Test and Verification.

COURSE DETAIL

Module	Lecture Topics
1: CMOS VLSI Design for Power and Speed consideration (Prof. A.N.Chandorkar)	1. Historical Perspective and Future Trends in CMOS VLSI Circuit and System Design- Part-I 2. Historical Perspective and Future Trends in CMOS VLSI Circuit and System Design - Part II 3. Logical Effort - A way of Designing Fast CMOS Circuits 4. Logical Effort - A way of Designing Fast CMOS Circuits -Part II 5. Logical Effort - A way of Designing Fast CMOS Circuits -Part III 6. Power Estimation and Control in CMOS VLSI circuits 7. Power Estimation and Control in CMOS VLSI circuits -Part II 8. Low Power Design Techniques- Part-I 9. Low Power Design Techniques -Part II

NP-TEL

NPTEL

http://nptel.iitm.ac.in

Electronics & Communication Engineering

Pre-requisites:

- **Basic course on VLSI Design**

Additional Reading:

- **Technical Papers in following Journals:** IEEE's Journal of Solid State Circuits, IEEE Trans. on CAD of ICs, IEEE Trans. on VLSI, IEEE Trans. on Circuits and Systems, Embedded System Letters(IEEE), IEEE Trans. On Computers

Coordinators:

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2: Datapath Design (Prof. A.N.Chandorkar)	11. Arithmetic Implementation Strategies for VLSI – Part I 12. Arithmetic Implementation Strategies for VLSI -Part II 13. Arithmetic Implementation Strategies for VLSI -Part III 14. Arithmetic Implementation Strategies for VLSI -Part IV
3: Interconnect aware design (Prof. Dinesh Sharma)	15. Interconnect aware design: Impact of scaling, buffer insertion and Inductive peaking 16. Interconnect aware design: Low swing and Current mode signaling 17. Interconnect aware design: Capacitively coupled interconnects
4: Hardware Description Languages for VLSI Design (Prof. Dinesh Sharma)	18. Managing concurrency and time in Hardware Description Languages 19. Introduction to VHDL 20. Basic Components in VHDL 21. Structural Description in VHDL 22. Behavioral Description in VHDL 23. Introduction to Verilog
5: FSM Controller/Datapath and Processor Design (Prof. Sachin Patkar)	24. FSM + datapath (GCD example) 25. FSM + datapath (continued) 26. Single Cycle MMIPS 27. Multicycle MMIPS 28. Multicycle MMIPS – FSM
6: VLSI Design Automation (Prof. Sachin Patkar)	29. Brief Overview of Basic VLSI Design Automation Concepts 30. Netlist and System Partitioning 31. Timing Analysis in the context of Physical Design Automation

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	32. Placement algorithm
7: VLSI Design Test and Verification (Prof. Virendra Singh)	33. Introduction to VLSI Testing 34. VLSI Test Basics - I 35. VLSI Test Basics - II 36. VLSI Testing: Automatic Test Pattern Generation 37. VLSI Testing: Design for Test (DFT) 38. VLSI Testing: Built-In Self-Test (BIST) 39. VLSI Design Verification: An Introduction 40. VLSI Design Verification: Equivalence Checking 41. VLSI Design Verification: Equivalence/Model Checking 42. VLSI Design Verification: Model Checking

References:

- **Module 1 and 2:** “Principles of CMOS VLSI Design” by Weste and Eshranghian, Second Edition, Pearson Education, India; “CMOS VLSI Design ” by Neil H. E. Weste, David F. Harris ,Pearson/Addison Wesley ; “Digital Integrated Circuits” , Jan M.Rabaey, Anant Chandrakasan, and Borivoje Nikoli?, Prentice Hall (India); “Logical Efforts: Designing Fast CMOS Circuits”, Ivan Suderland, Bob Sproull and D. Harris, Morgan Kaufmann, India. “Low Power CMOS VLSI Circuit Design”, Kaushik Roy, Wiley- Interscience.
- **Module 3:** “Modern VLSI Design”, Wayne Wolf, Third Edition, Pearson Education
- **Module 4:** “The designer's guide to VHDL”, Peter J. Ashenden, Second Edition, Morgan and Kaufmann/Harcourt India. “Verilog HDL” by Samir Palnitkar, Low Price Edition, Pearson Education, Asia
- Module 5: “CMOS VLSI Design” by Neil H. E. Weste, David F. Harris ,Pearson/Addison Wesley,“Computer Organization and Design, Fourth Edition: The Hardware/Software Interface” , David A. Patterson, John L. Hennessy,Morgan Kaufmann, 2008
- **Module 6:** “VLSI Physical Design: From Graph Partitioning to Timing Closure”, Kahng and Lienig,Springer, 2011
- **Module 7:** “Essential of Electronic Testing for Digital, Memory, and Mixed Signal VLSI Circuits”, M.L. Bushnell

and V.D Agrawal, Springer 2005 “VLSI Test Principles and Architectures”, L.W. Wang, C.W. Wu, W. Xioqing, Academic Press, 2006 . “Hardware Design Verification”, William Lam, Prentice Hall, “Logics in Computer Science”, M. Huth and M. Ryan, Cambridge University Press, 2006