PHASE LOCKED LOOPS

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PRE-REQUISITES : EE3002 (http://www.ee.iitm.ac.in/vlsi/courses/ee3002_2017/start)

INTENDED AUDIENCE : B.Tech (6th semester onwards), M.Tech./M.S./Ph.D. (1st semester onwards)

INDUSTRY SUPPORT : Texas Instruments, Intel, Qualcomm, Samsung, Cadence

COURSE OUTLINE :

This course will emphasize on developing intuition behind frequency synthesizer design, learning mathematical basis behind operation, and realizing PLLs at architecture and circuit level. The students will be exposed to state-of-the-art frequency synthesis techniques used in analog/digital integer-N PLLs. This course will equip students with skills to analyze, debug, and evaluate a PLL design at analytical and transistor levels both. The students will be able to use their knowledge and skills while generating a clock signal in a power-efficient manner for requirements of a synchronous system.

ABOUT INSTRUCTOR :

Prof. Saurabh Saxena (S'10–M'16) received the B.Tech. degree in electrical engineering, the M.Tech. degree in microelectronics and VLSI design from the Indian Institute of Technology Madras, Chennai, India, in 2009, and the Ph.D. degree in electrical and computer engineering from the University of Illinois, Urbana-Champaign, IL in 2015. He is currently an Assistant Professor in the Department of Electrical Engineering at Indian Institute of Technology Madras, Chennai, India. Prof. Saxena is a recipient of Young Faculty Research Fellowship of Visvesvaraya PhD programme of MeitY, GoI. He serves as a reviewer for the IEEE Journal of Solid-StateCircuits, IEEE Transactions on Circuits and Systems I, IEEE Transactions on Very Large Scale Integration Systems, and IEEE International Symposium on Circuits and Systems. His research interests include delta-sigma modulators, high speed I/O interfaces, and clocking circuits.

COURSE PLAN :

Week 1: Basic concepts in PLL, Type-I PLL
Week 2: Frequency acquisition in PLLs
Week 3: Phase/frequency error detectors, Charge-pump based type-II PLLs
Week 4: Noise analysis in charge-pump PLLs
Week 5: Design of PLL building blocks: PFD
Week 6: Design of PLL building blocks: Charge-pump
Week 7: Design of PLL building blocks: Ring oscillators
Week 8: Design of PLL building blocks: Supply regulated oscillators
Week 9: Design of PLL building blocks: Loop filter
Week 10: Split-tuned Analog PLL
Week 11: Digital PLLs
Week 12: Noise analysis in digital PLLs