



DIGITAL SYSTEM DESIGN

PROF. NEERAJ GOEL

Department of CSE
IIT Ropar

INTENDED AUDIENCE : CSE, EE, ECE undergraduate students

INDUSTRIES APPLICABLE TO : Any VLSI related company: Intel, AMD, TI, nVIDIA, Qualcomm, etc.

COURSE OUTLINE :

Digital system design course focuses on design digital system from scratch. The course focuses on designing combinational and sequential building blocks, using these building blocks to design bigger digital systems. During this course we also learn how to use Verilog to design/model a digital system.

ABOUT INSTRUCTOR :

Prof. Neeraj Goel is an Assistant Professor in the Department of Computer Science and Engineering at IIT Ropar. His research interest includes processor architecture, SoC design, SoC modeling and low power design. He received B.Tech degree in Electronics and communication from NIT Kurukshetra, M.Tech degree in VLSI Design Tools and Technology from IIT Delhi and PhD in Computer Science and Engineering from IIT Delhi.

COURSE PLAN :

Week 1: Introduction of digital systems. Number system

Week 2: Number representation: BCD, floating point numbers

Week 3: Boolean algebra, application of Boolean algebra in minimization of Boolean expressions

Week 4: Boolean minimization using K-map and Quine McCluskey method. Introduction to Verilog

Week 5: MSI Logic: Multiplexer, encoder, decoder

Week 6: Arithmetic circuits: Adder, subtractor, multiplier, comparator

Week 7: Latches and flipflop (SR, JK, T, D), counters

Week 8: Sequential logic like Registers, introduction to behavior modeling in Verilog

Week 9: Finite state machine, state graphs and tables.

Week 10: Reduction of state table and state assignments. Arithmetic circuits using sequential design.

Week 11: Register transfer level (RTL) design, RTL design examples

Week 12: FPGA, VLSI design flow using HDL, introduction to behavior, logic and physical synthesis.