

SYSTEM DESIGN THROUGH VERILOG

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PRE-REQUISITES: Digital Circuits

INTENDED AUDIENCE: Undergraduate, post graduate students, faculty and industry people

INDUSTRIES APPLICABLE TO: Cadence/Mentor graphics

COURSE OUTLINE:

A comprehensive resource on Verilog HDL for beginners and experts large and complicated digital circuits can be incorporated into hardware by using Verilog, a hardware description language (HDL). A designer aspiring to master this versatile language must first become familiar with its constructs, practice their use in real applications, and apply them in combinations in order to be successful. Design Through Verilog HDL affords novices the opportunity to perform all of these tasks, while also offering seasoned professionals a comprehensive resource on this dynamic tool.

ABOUT INSTRUCTOR:

Prof. Shaik Rafi Ahamed is a professor with more than 20 years teaching experience. He had taught Digital design including verilog nearly 10 times for undergraduate students at IIT Guwahati and other institutions. He have published several papers in reputed Journals like IEEE, Elsevier, IET and Springer.

COURSE PLAN:

Week 1: Introduction to Verilog

Week 2: Gate level modelling

Week 3: Behavioral modelling I

Week 4: Behavioral modelling II

Week 5: Data flow modelling

Week 6: Switch level modelling

Week 7: Synthesis of combinational logic using verilog

Week 8: Synthesis of sequential logic using verilog