Multi-Core Computer Architecture

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PRE-REQUISITES : Second-year undergraduate or above or any level of postgraduates in Computer Science and related fields (like ECE, EEE, IT etc.). A basic understanding of digital logic, microprocessors, computer organization will be added advantage.

INTENDED AUDIENCE : Anyone in CSE and related fields like ECE, EEE, IT etc. with an interest in exploring Computer Architecture.

INDUSTRIES SUPPORT : Intel, AMD, IBM, HP, Apple, Samsung etc.

COURSE OUTLINE :

The use of mobile gadgets and applications is crucial to maintaining comfort in modern living. These apps are supported by portable electronic devices with powerful microprocessors. We are in the era of multi-core systems where even the simplest of handheld devices like a smart phone houses many processors in a single chip. The core counts are ever increasing from 8 to 10 in smart phones to over 100s in super computers. This course will introduce the students to the world of multi-core computer architectures. With the unprecedented growth of data science, on-chip storage systems and inter-core communication framework are getting equal attention as that of processors. This course will focus on delivering an in-depth exposure in advanced computer architecture starting from the fundamentals of basic computer organization to advanced topics like multicore processors, GPUs, advanced cache memory optimizations, DRAM systems, on chip interconnects and domain specific accelerators. The course concludes with pointers to current research standings and on-going research directions for motivating the students to explore further.

ABOUT INSTRUCTOR :

Prof. John Jose is an Associate Professor in Department of Computer Science & Engineering, Indian Institute of Technology Guwahati, where he joined as an Assistant Professor in 2015. He completed his Ph.D degree from Indian Institute of Technology Madras in the field of computer architecture. He was a rank holder in M.Tech degree from Vellore Institute of Technology (VIT University). He did his B.Tech degree from College of Engineering Adoor, Cochin University, Kerala. He is the recipient of the prestigious Qualcomm Faculty Award 2021. He is also serving as the Vice-Chair of IEEE India Council. His research group in Multicore Architecture and Systems Lab at IITG explores the domain of network on chips, cache management techniques for large multicore systems, non-volatile memories, hardware security, domain specific hardware accelerators and disaggregated storage systems. He is the associated editor for IEEE-Embedded System Letter Journal. He has over 35 IEEE & ACM peer reviewed conference publications, over 15 ACM & IEEE transactions papers as well as Springer and Elsevier journal papers to his credit. He is a reviewer for many national and international peer reviewed journals and member of technical program committee and organizing committee for many IEEE/ACM national and international conferences. He is the investigator for several R&D projects under DST and MeitY. He is associated with many national pilot projects like NPTEL-MOOCS, SPARC, GIAN, TEQIP, ISEA, Ishan Vikas, Vigyan Jyoti etc. He has active academic research collaboration with University of Catania, Italy, University of Florida, USA, University of Essex, UK, Federal University Naples, Italy and Qualcomm India. He has offered two popular NPTEL Online Certification courses in the area of Computer Architecture. He was the recipient of ACM-SIGDA, IEEE-CEDA, IARCS and DRDO research grants for technical presentations in various international forums. He is a resource person for computer architecture and hardware security related symposia, workshops, short-term courses and faculty development programs in many organizations across the country. He is an invited speaker for many career guidance seminars/ teaching pedagogy workshops to various technical institutes, R&D houses and schools. He is also serving as Board of Studies members to various universities and autonomous colleges. He is an active member of professional societies like ACM, IEEE, ISTE and CSI.

COURSE PLAN:

Week 1 : Basic Computer Organization:

Review of Basic Computer Organization, Basic operational concepts, fundamental of program execution, memory and I/O addressing, Instruction set architecture- addressing modes, instruction set, instruction encoding and formats. CISC vs RISC ISA.

Week 2 : Instruction Pipeline Principles:

Performance Evaluation Methods, Introduction to RISC Instruction Pipeline, Instruction Pipeline and Performance.Pipeline Hazards and Analysis

Week 3 : Pipeline Hazards and Branch Prediction Techniques:

Pipeline Hazards Management Techniques,Branch Prediction, MIPS Pipeline for Multi-Cycle Operations.

Week 4 : Pipeline Scheduling and Speculative execution:

Compiler Techniques to Explore Instruction Level Parallelism, Dynamic Scheduling with Tomasulo's Algorithm, Speculative Execution.

Week 5 : Superscalar Processors and GPU architectures:

Advanced Pipelining, Multithreading and Hyperthreading, Superscalar Processors, GPU Architectures.

Week 6 : Cache Memory Principles

Introduction to Cache Memory, Block Replacement Techniques and Write Strategy, Design Concepts in Cache Memory.

Week 7 : Cache Memory Optimizations

Design issues for improving memory access time, Basic and Advanced Optimization Techniques in Cache Memory

Week 8 : Cache Coherence Protocols

Cache coherence and memory consistency, Snoop Based and Directory Based Cache coherence Protocols.

Week 9 : Primary Storage Systems

Introduction to DRAM System, DRAM organization, DRAM Controllers and Address Mapping.

Week 10 : Tiled Chip Multi-Core Processors & Network-on-Chip

Tiled Chip Multicore Processors (TCMP), Network on Chips (NoC), Routing Algorithms, NoC router – architecture, Routing and flow control

Week 11 : Energy Efficient NoCs

Introduction to deflection routing, Energy Efficient Buffer-less NoC Routers, Side-buffered Deflection Routers

Week 12 : Quality of Service for TCMPs

QoS of NoC and Caches in TCMPs, Emerging Trends in Network On Chips, Domain Specific Accelerators