Digital Electronic Circuits

Live Session Week 1
NPTEL Online Certification Course

29 January 2022

Brief Summary of Lecture 1 and 2

Lecture 1 : Introduction

- Why 'Digital' ?
- Switching and logic operation
- Diode as a switch.

Lecture 2 : Transistor as a switch

- Transistor as an inverter
- Input-output characteristics
- Noise margin, transition width, logic swing
- Fan-out

Brief Summary of Lecture 3, 4 and 5

Lecture 3 : Performance Issues and Introduction to TTL

- Propagation delay and power dissipation
- RTL NOR and NAND gate
- DTL NAND gate
- TTL NAND gate

Lecture 4 : Transistor Transistor Logic (TTL)

- TTL Transfer Characteristics and operating parameters
- TTL Open Collector configuration and TTL Tristate
- Schottky TTL

Lecture 5 : CMOS Logic

- CMOS Logic gate and its characteristics, CMOS Tristate and Open-drain
- CMOS – TTL Interface

Q 1. Considering the propagation delay of transistors, which of the following statements are true?

(1) Propagation delay occurs due to finite switching speed of transistor and circuit capacitor.

(2) Propagation delay is directly proportional to power dissipation.

(3) Propagation delay is associated with rise time and fall time.

(4) Propagation delay is quantified by averaging the time taken for high to low and low to high transitions.

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a. (1), (2), (3)

b. (1), (2), (4)

c. (2), (3), (4)

d. (1), (3), (4)

Q 2. The role of level-shifter diodes in DTL is to:

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a. Increase V_{IH}

b. Increase V_{IL}

c. Decrease V_{IL}

d. Decrease V_{IH}

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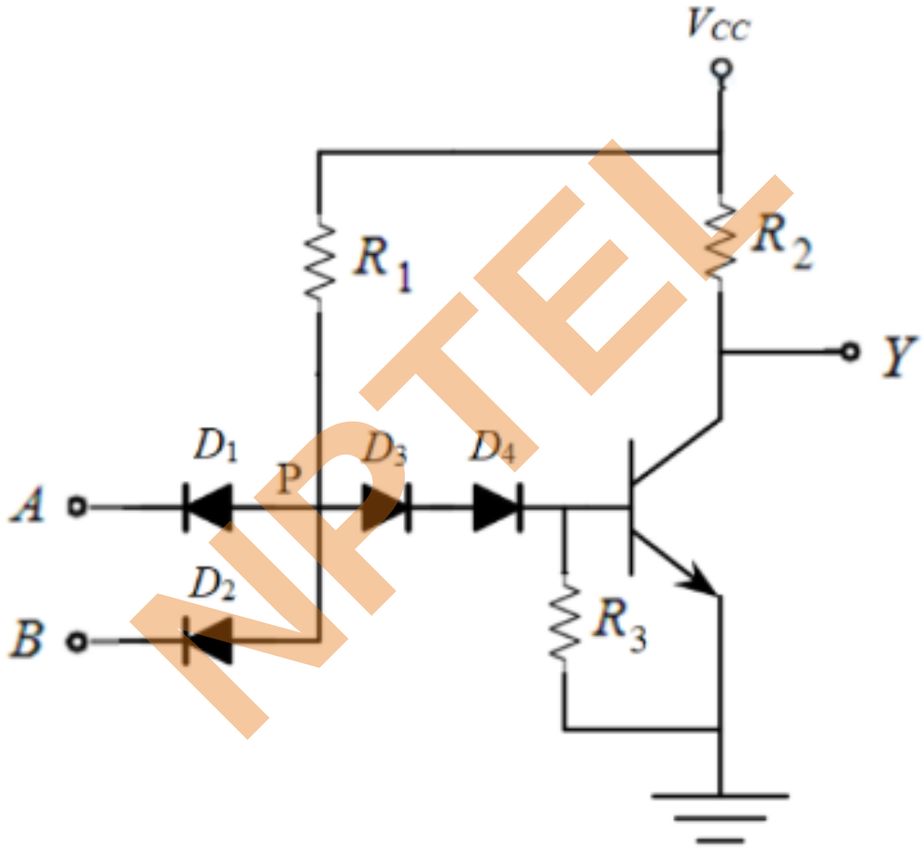

Q 3. For a given logic family, consider $V_{OL} = 0.9V$ and $V_{OH} = 4.5V$. For a given circuit, $V_{IL} = 1.2V$ and $V_{IH} = 3.2V$. Find the noise margins (NM_L and NM_H). Is it functionally better than a circuit with $V_{IL} = 1.5V$ and $V_{IH} = 3V$? (Yes/No)

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a. 0.3, 1.3, Yes

b. 1.3, 0.3, No

c. 0.3, 1.3, No

d. 1.3, 0.3, Yes

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For first circuit

$NM_L = V_{IL} - V_{OL} = 1.2 - 0.9 = 0.3V$

$NM_H = V_{OH} - V_{IH} = 4.5 - 3.2 = 1.3V$

For second circuit

$NM_L = V_{IL} - V_{OL} = 1.5 - 0.9 = 0.6V$

$NM_H = V_{OH} - V_{IH} = 4.5 - 3 = 1.5V$

Q 4. Which of the following statements are FALSE about CMOS logic?

(1) CMOS has very high input resistance and hence draws very low current.

(2) CMOS has high fan-out as compared to TTL.

(3) CMOS is generally faster than TTL.

(4) CMOS has low packing density.

(5) CMOS exhibits low power consumption.

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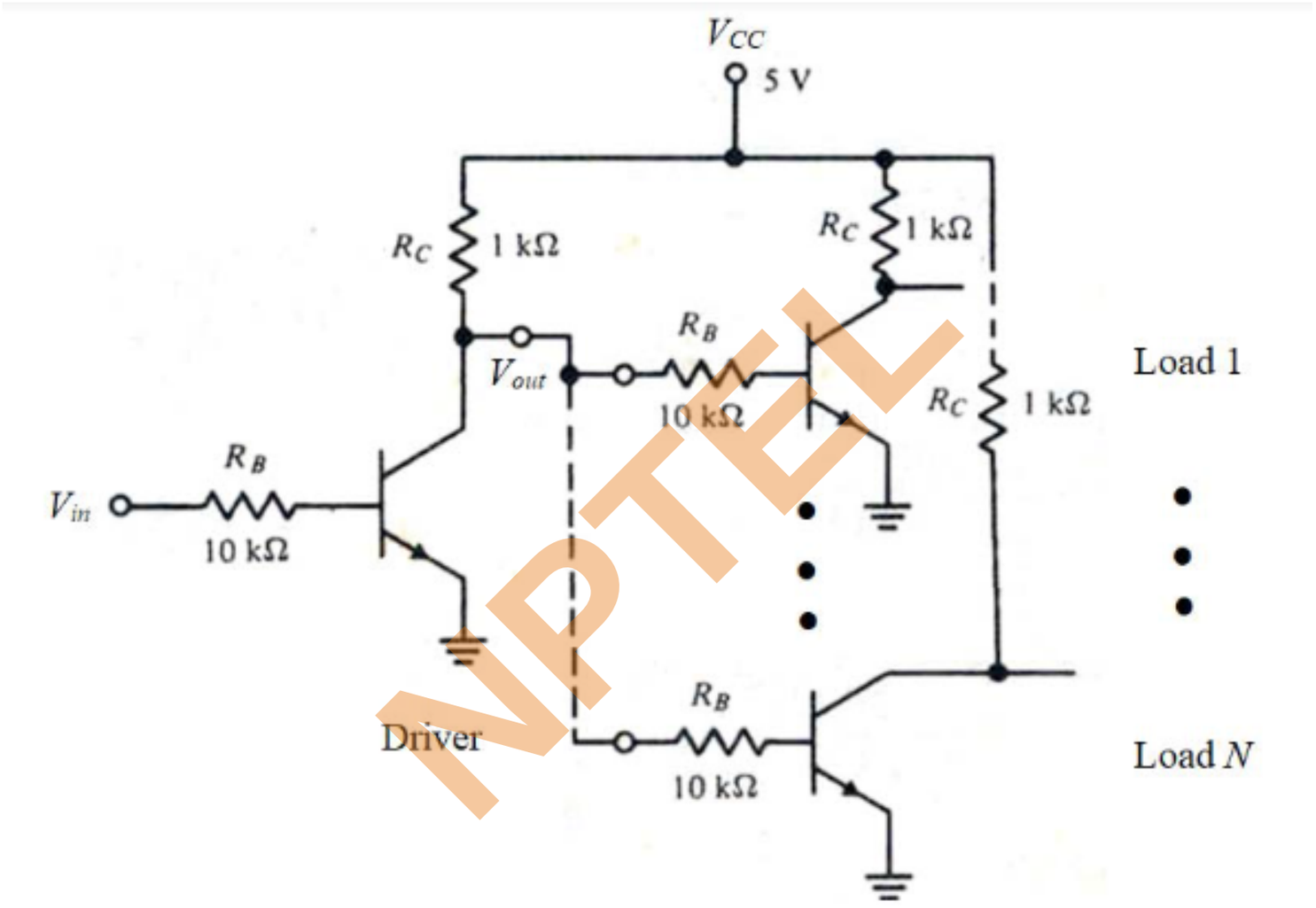
a. (1), (3), (4)

b. (1), (2), (3), (5)

c. (1), (2), (5)

d. (3), (4)

Q 5. In the given circuit, $V_{CE(\text{sat})} = 0.2V, \beta_F = 50, V_{BE(\text{sat})} = 0.7V, V_{IH} = 2V$. Also consider the noise margin high $NM_H = 1V$. What is fanout without and with noise margin?



a. $23, 8$

b. $33, 11$

c. $23, 9$

d. $33, 12$

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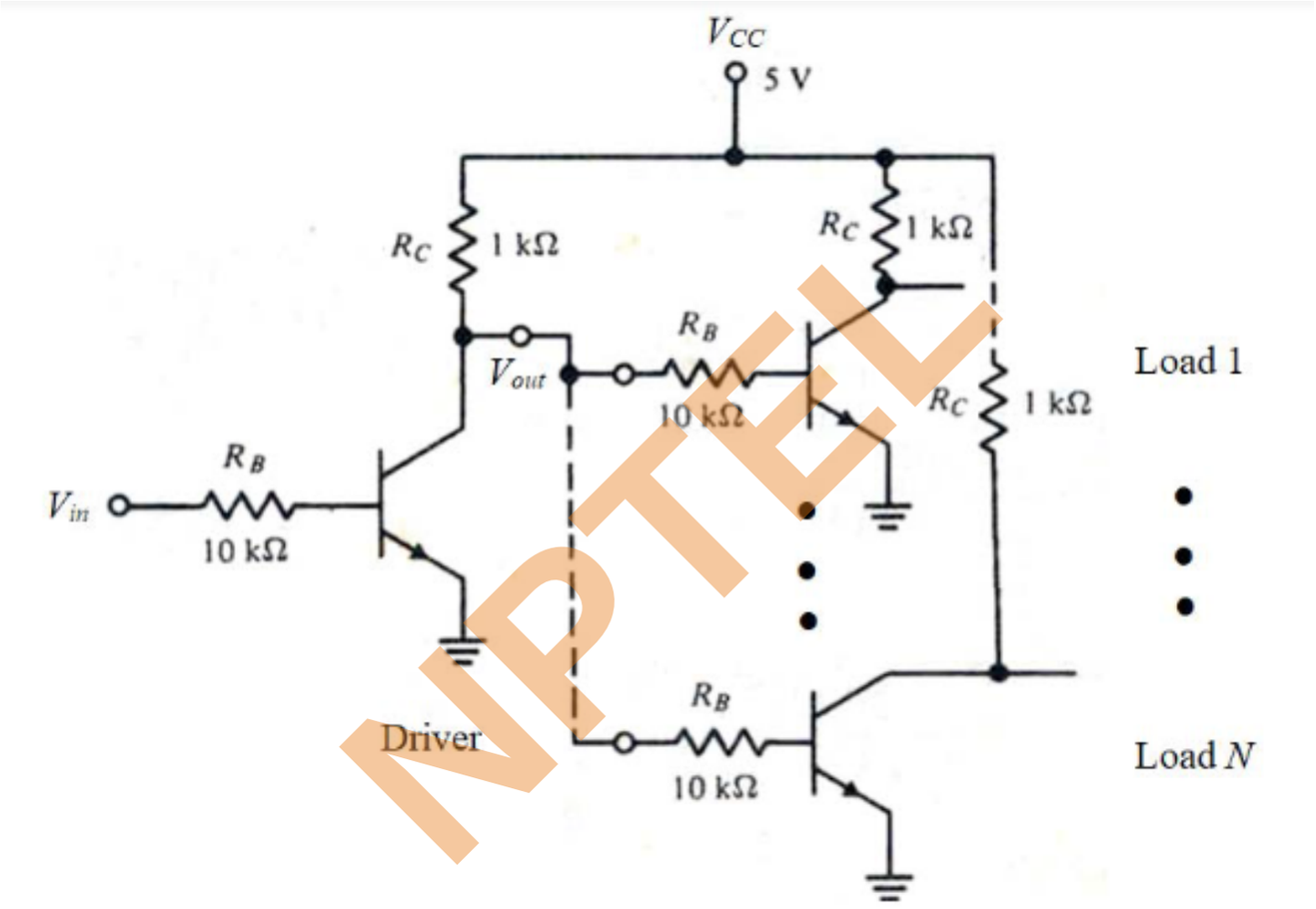


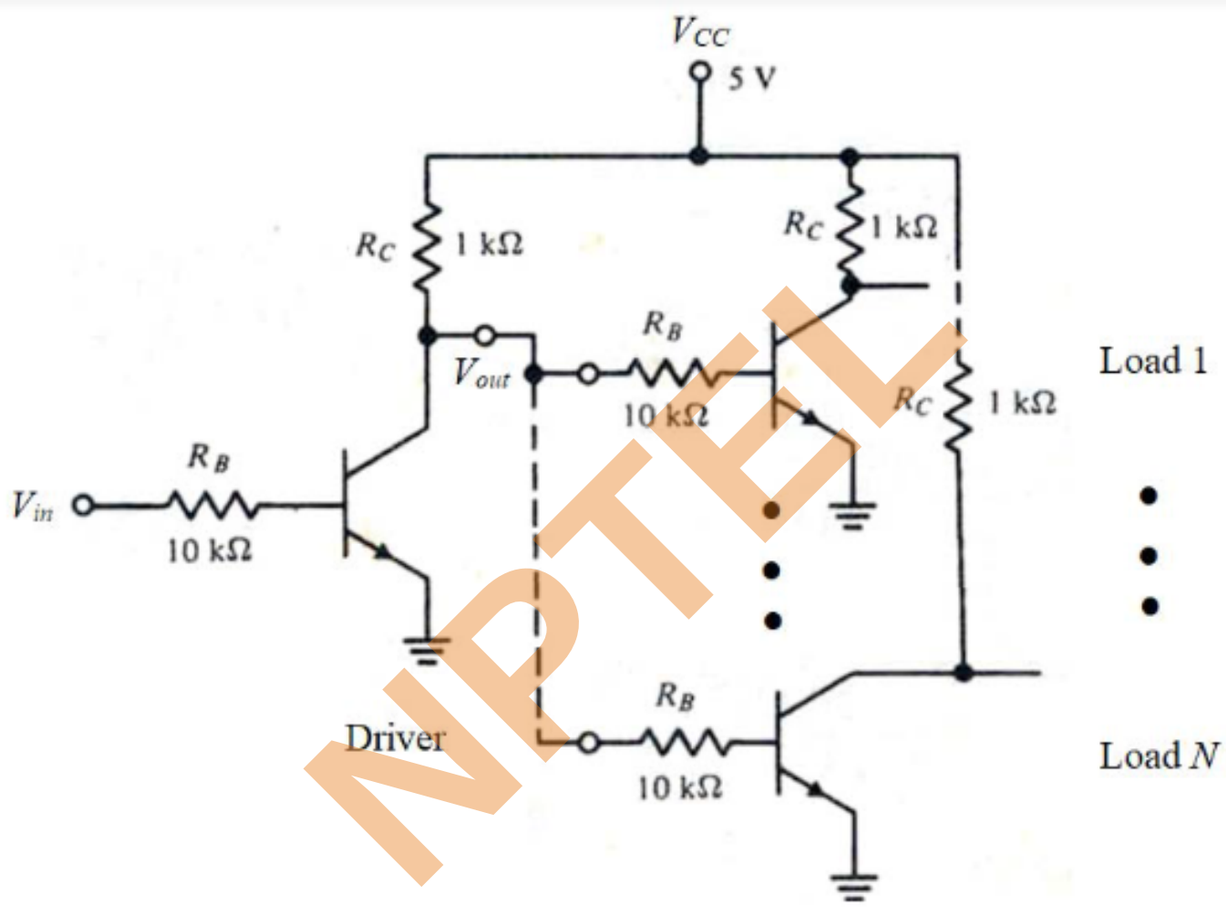
Without noise margin $V_{IH} = 2V$

$I_{C(driver)} = (V_{CC} - V_{out})/R_C = (5-2)/1 = 3mA$

$I_{B(load)} = (V_{out} - V_{BE(sat)})/R_B = (2-0.7)/10 = 0.13mA$

$N = I_{C(driver)}/I_{B(load)} = 3/0.13 = 23.08 \approx 23$

Q 5. In the given circuit, $V_{CE(\text{sat})} = 0.2V, \beta_F = 50, V_{BE(\text{sat})} = 0.7V, V_{IH} = 2V$. Also consider the noise margin high $NM_H = 1V$. What is fanout without and with noise margin?



With noise margin $NM_H = 1V$

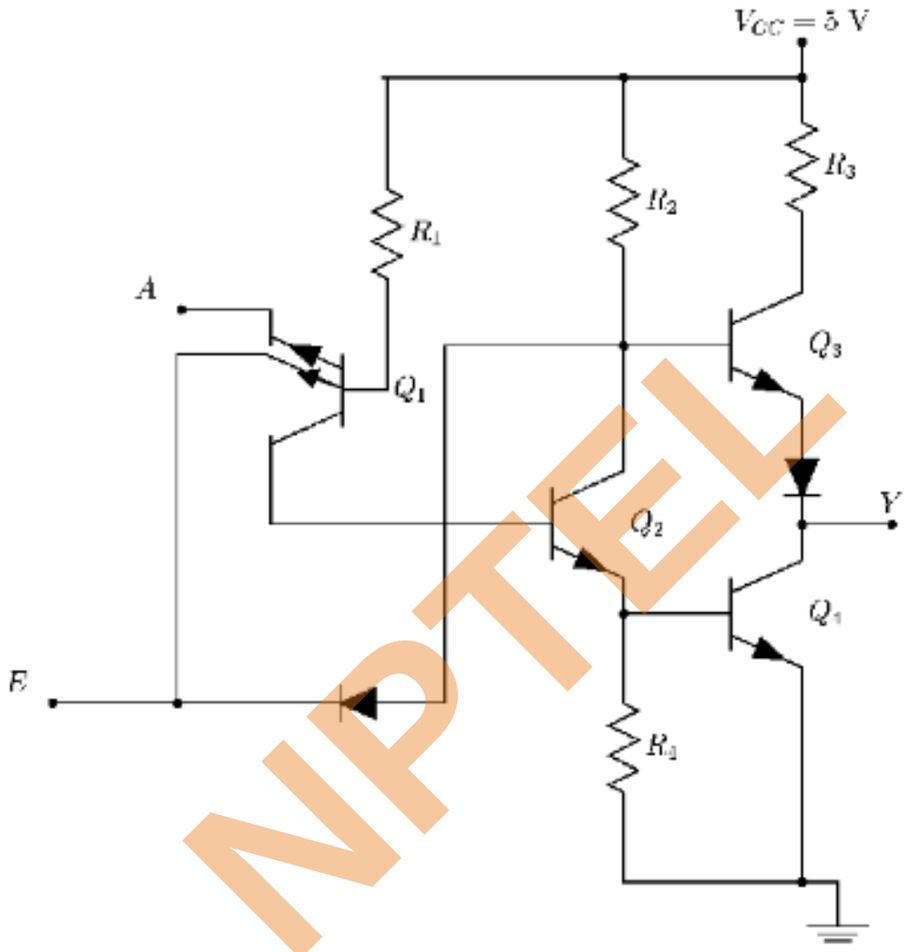
$V_{OH} = V_{IH} + NM_H = 2 + 1 = 3V$

$I_{C(driver)} = (V_{CC} - V_{out})/R_C = (5 - 3)/1 = 2mA$

$I_{B(load)} = (V_{out} - V_{BE(sat)})/R_B = (3 - 0.7)/10 = 0.23mA$

$N = I_{C(driver)}/I_{B(load)} = 2/0.213 = 8.696 \approx 8$

Q 6. Identify the following circuit?



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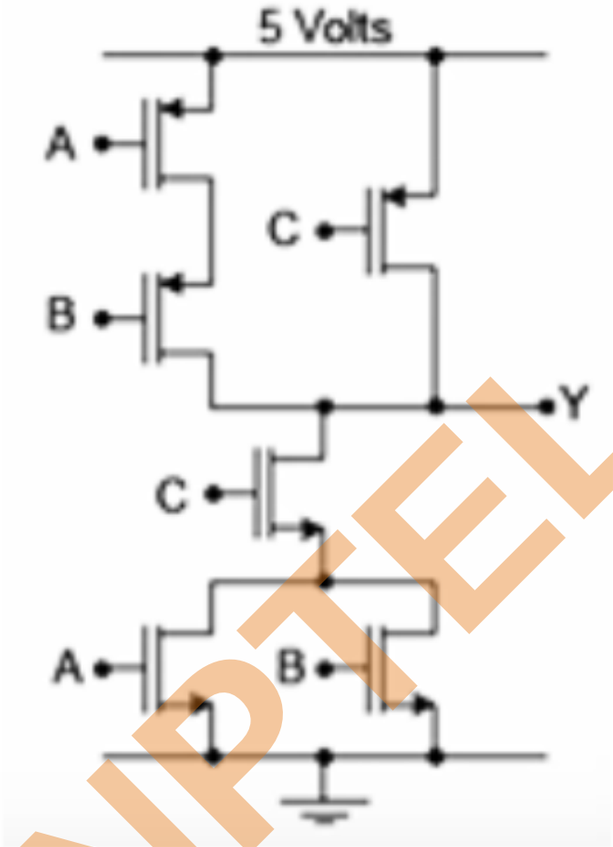
a. Tristate buffer

b. Tristate inverter

c. Open collector logic

d. Totem pole logic

Q 7. Find out the output expression of 'Y' from the circuit given below.



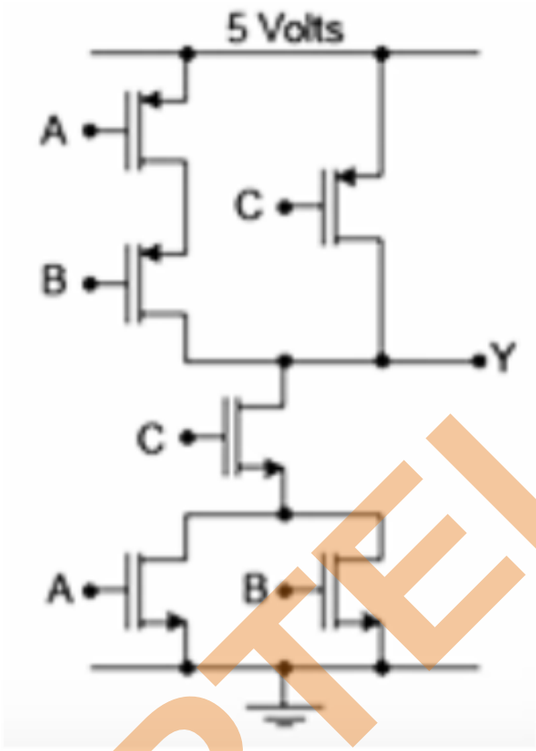
a. $Y = (A + B)C$

b. $Y = \overline{A}\ \overline{B} + \overline{C}$

c. $Y = AB + C$

d. $Y = (\overline{A} + \overline{B})\overline{C}$

Q 7. Find out the output expression of 'Y' from the circuit given below.

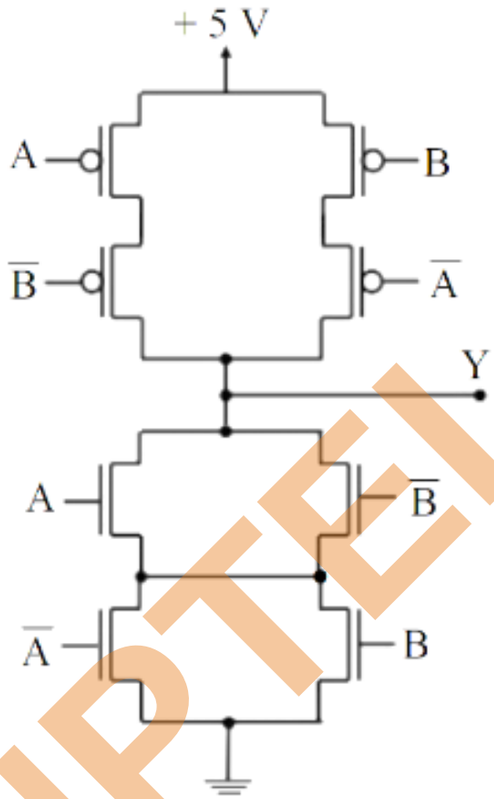


DeMorgan's rule

$$\overline{E+F} = \overline{E}\ \overline{F}, \qquad \overline{EF} = \overline{E} + \overline{F}$$

$$\begin{aligned} Y &= \overline{(A+B)C} \\ &= \overline{(A+B)} + \overline{C} \\ &= \overline{A}\ \overline{B} + \overline{C} \end{aligned}$$

Q 8. The given CMOS circuit implements the logic:



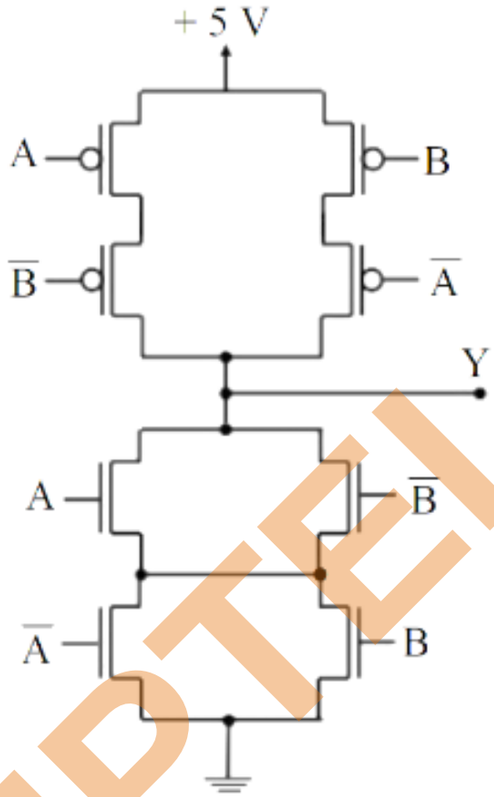
a. $Y = \overline{A}B + A\overline{B}$

b. $Y = \overline{A}\ \overline{B} + AB$

c. $Y = \overline{AB}$

d. $Y = \overline{A + B}$

Q 8. The given CMOS circuit implements the logic:



DeMorgan's rule: $\overline{E+F} = \overline{E}\ \overline{F}, \qquad \overline{EF} = \overline{E} + \overline{F}$

$$
\begin{aligned}
Y &= \overline{(A+\overline{B})(\overline{A}+B)} \\
&= \overline{(A+\overline{B})} + \overline{(\overline{A}+B)} \\
&= \overline{A}\ \overline{\overline{B}} + \overline{\overline{A}}\ \overline{B} = \overline{A}\ B + A\ \overline{B}
\end{aligned}
$$

Thank You