

# **Module 3 : Fabrication Process and Layout Design Rules**

## **Lecture 12 : CMOS Fabrication Technologies**

### **Objectives**

In this course you will learn the following

- Introduction
- Twin Well/Tub Technology
- Silicon on Insulator (SOI)
- N-well/P-well Technology

### **12.1 Introduction**

CMOS fabrication can be accomplished using either of the three technologies:

- N-well/P-well technologies
- Twin well technology
- Silicon On Insulator (SOI)

In this discussion we will focus chiefly on N-well CMOS fabrication technology.

### **12.2 Twin Well Technology**

Using twin well technology, we can optimise NMOS and PMOS transistors separately. This means that transistor parameters such as threshold voltage, body effect and the channel transconductance of both types of transistors can be tuned independently.

n+ or p+ substrate, with a lightly doped epitaxial layer on top, forms the starting material for this technology. The n-well and pwell are formed on this epitaxial layer which forms the actual substrate. The dopant concentrations can be carefully optimized to produce the desired device characteristics because two independent doping steps are performed to create the well regions.

The conventional n-well CMOS process suffers from, among other effects, the problem of unbalanced drain parasitics since the doping density of the well region typically being about one order of magnitude higher than the substrate. This problem is absent in the twin-tub process.

### **12.3 Silicon on Insulator (SOI)**

To improve process characteristics such as speed and latch-up susceptibility, technologists have sought to use an insulating substrate instead of silicon as the substrate material.

Completely isolated NMOS and PMOS transistors can be created virtually side by side on an insulating substrate (eg. sapphire) by using the SOI CMOS technology.

This technology offers advantages in the form of higher integration density (because of the absence of well regions), complete avoidance of the latch-up problem, and lower parasitic capacitances compared to the conventional n-well or twin-tub CMOS processes.

But this technology comes with the disadvantage of higher cost than the standard n-well CMOS process. Yet the improvements of device performance and the absence of latch-up problems can justify its use, especially in deep submicron devices.

## 12.4 N-well Technology

In this discussion we will concentrate on the well established n-well CMOS fabrication technology, which requires that both n-channel and p-channel transistors be built on the same chip substrate. To accommodate this, special regions are created with a semiconductor type opposite to the substrate type. The regions thus formed are called wells or tubs. In an n-type substrate, we can create a p-well or alternatively, an n-well is created in a p-type substrate. We present here a simple n-well CMOS fabrication technology, in which the NMOS transistor is created in the p-type substrate, and the PMOS in the n-well, which is built-in into the p-type substrate.

Historically, fabrication started with p-well technology but now it has been completely shifted to n-well technology. The main reason for this is that, "n-well sheet resistance can be made lower than p-well sheet resistance" (electrons are more mobile than holes).

The simplified process sequence (shown in Figure 12.41) for the fabrication of CMOS integrated circuits on a p-type silicon substrate is as follows:

- N-well regions are created for PMOS transistors, by impurity implantation into the substrate.
- This is followed by the growth of a thick oxide in the regions surround the NMOS and PMOS active regions.
- The thin gate oxide is subsequently grown on the surface through thermal oxidation.
- After this n<sup>+</sup> and p<sup>+</sup> regions (source, drain and channel-stop implants) are created.
- The metallization step (creation of metal interconnects) forms the final step in this process.

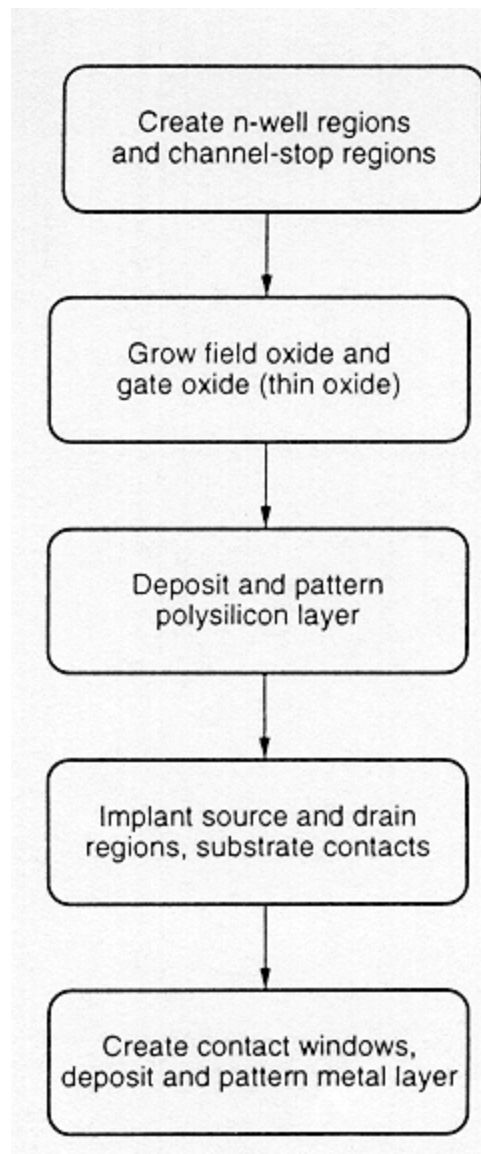
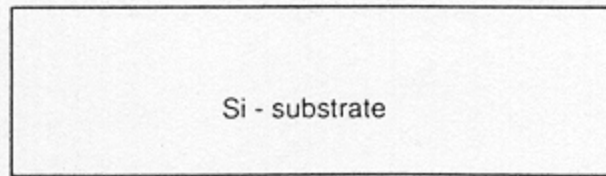


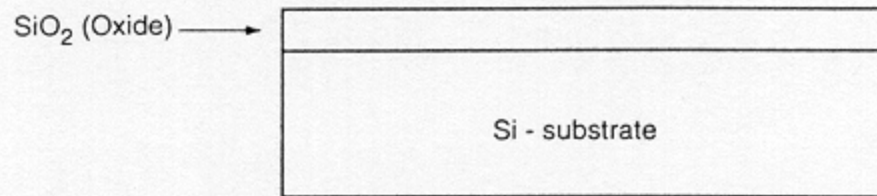
Fig 12.41: Simplified Process Sequence For Fabrication Of CMOS ICs

The integrated circuit may be viewed as a set of patterned layers of doped silicon, polysilicon, metal and insulating silicon dioxide, since each processing step requires that certain areas are defined on chip by appropriate masks. A layer is patterned before the next layer of material is applied on the chip. A process, called lithography, is used to transfer a pattern to a layer. This must be repeated for every layer, using a different mask, since each layer has its own distinct requirements.

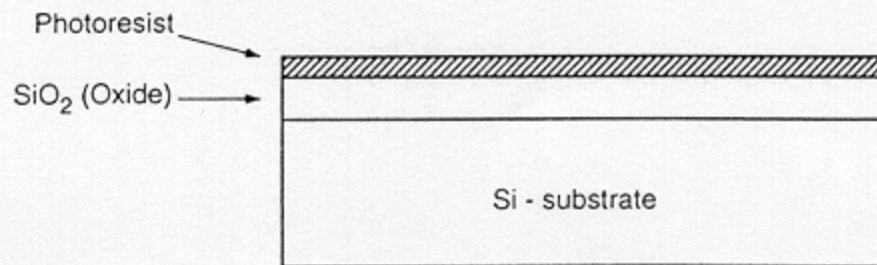
We illustrate the fabrication steps involved in patterning silicon dioxide through optical lithography, using Figure 12.42 which shows the lithographic sequences.



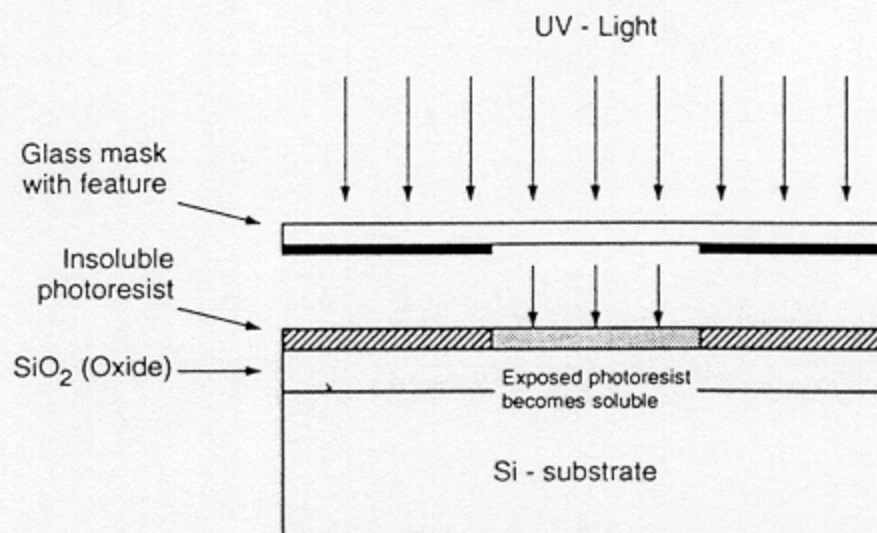
(a)



(b)



(c)



(d)

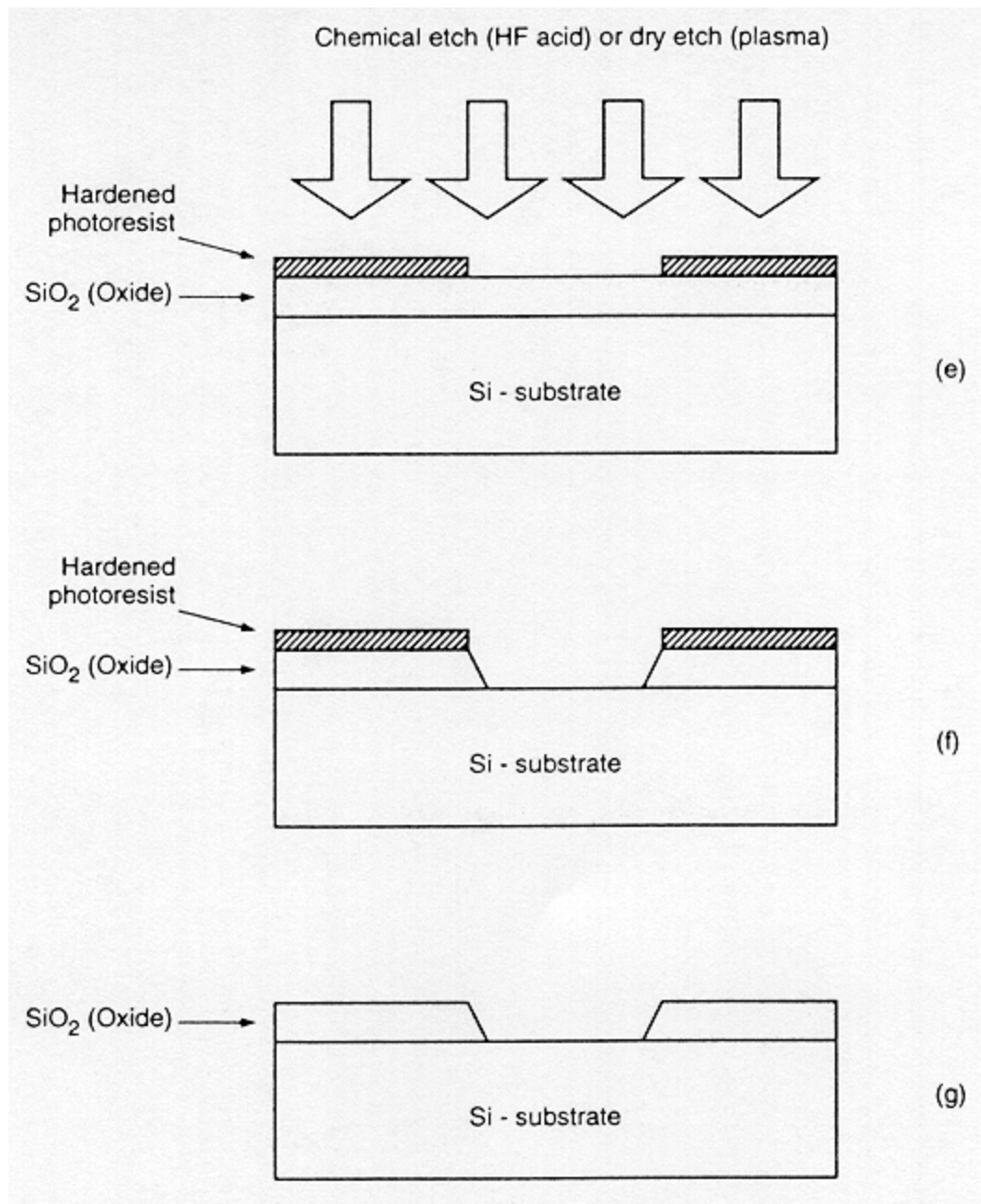


Fig 12.42: Process steps required for patterning of silicon dioxide

First an oxide layer is created on the substrate with thermal oxidation of the silicon surface. This oxide surface is then covered with a layer of photoresist. Photoresist is a light-sensitive, acid-resistant organic polymer which is initially insoluble in the developing solution. On exposure to ultraviolet (UV) light, the exposed areas become soluble which can be etched away by etching solvents. Some areas on the surface are covered with a mask during exposure to selectively expose the photoresist. On exposure to UV light, the masked areas are shielded whereas those areas which are not shielded become soluble.

There are two types of photoresists, positive and negative photoresist. Positive photoresist is initially insoluble, but becomes soluble after exposure to UV light, whereas negative photoresist is initially soluble but becomes insoluble (hardened) after exposure to UV light. The process sequence described uses positive photoresist.

Negative photoresists are more sensitive to light, but their photolithographic resolution is not as high as that of the positive photoresists. Hence, the use of negative photoresists is less common in manufacturing high-density integrated circuits.

The unexposed portions of the photoresist can be removed by a solvent after the UV exposure step. The silicon dioxide regions not covered by the hardened photoresist is etched away by using a chemical solvent (HF acid) or dry etch (plasma etch) process. On completion of this step, we are left with an oxide window which reaches down to the silicon surface. Another solvent is used to strip away the remaining photoresist from the silicon dioxide surface. The patterned silicon dioxide feature is shown in Figure 12.43

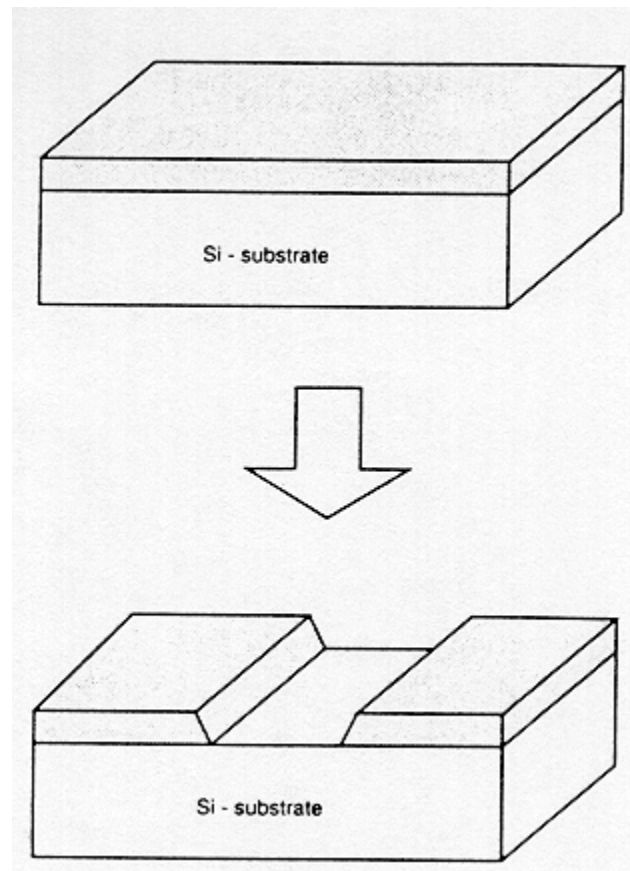


Fig 12.43: The result of single photolithographic patterning sequence on silicon dioxide

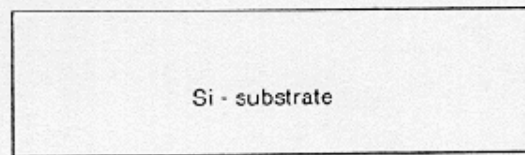
The sequence of process steps illustrated in detail actually accomplishes a single pattern transfer onto the silicon dioxide surface. The fabrication of semiconductor devices requires several such pattern transfers to be performed on silicon dioxide, polysilicon, and metal. The basic patterning process used in all fabrication steps, however, is quite similar to the one described earlier. Also note that for accurate generation of high-density patterns required in submicron devices, electron beam (E-beam) lithography is used instead of optical lithography.

In this section, we will examine the main processing steps involved in fabrication of an n-channel MOS transistor on a p-type silicon substrate.

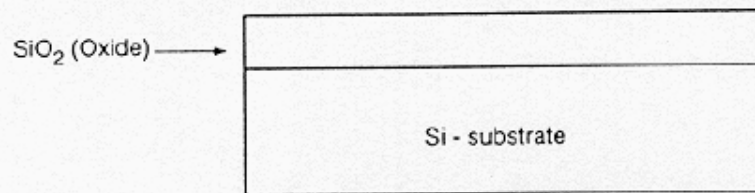
The first step of the process is the oxidation of the silicon substrate (Fig 12.44(a)), which creates a relatively thick silicon dioxide layer on the surface. This oxide layer is called field oxide (Fig. 12.44(b)). The field oxide is then selectively etched to expose the silicon surface on which the transistor will be created (Fig. 12.44(c)). After this the surface is covered with a thin, high-quality oxide layer. This oxide layer will form the gate oxide of the MOS transistor (Fig. 12.44(d)). Then a polysilicon layer is deposited on the thin oxide (Fig 12.44(e)). Polysilicon is used as both a gate electrode material for MOS transistors as well as an interconnect medium in silicon integrated circuits. The resistivity of polysilicon, which is usually high, is reduced by doping it with impurity atoms.

Deposition is followed by patterning and etching of polysilicon layer to form the interconnects and the MOS transistor gates (Fig. 12.44(f)). The thin gate oxide not masked by polysilicon is also etched away exposing the bare silicon surface. The drain and source junctions are to be formed (Fig 12.44(g)). Diffusion or ion implantation is used to dope the entire silicon surface with a high concentration of impurities (in this case donor atoms to produce n-type doping). Fig 12.44(h) shows two n-type regions (source and drain junctions) in the p-type substrate as doping penetrates the exposed areas of the silicon surface. The penetration of impurity doping into the polysilicon reduces its resistivity. The polysilicon gate is patterned before the doping and it precisely defines the location of the channel region and hence, the location of the source and drain regions. Hence this process is called a self-aligning process.

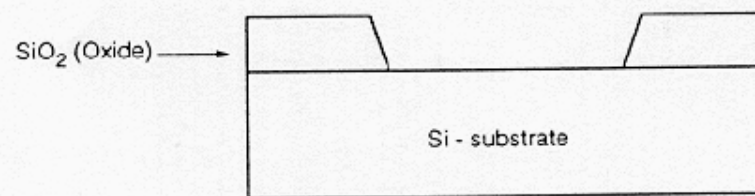
The entire surface is again covered with an insulating layer of silicon dioxide after the source and drain regions are completed (Fig 12.44(i)). Next contact windows for the source and drain are patterned into the oxide layer (Fig. 12.44(j)). Interconnects are formed by evaporating aluminium on the surface (Fig 12.44(k)), which is followed by patterning and etching of the metal layer (Fig 12.44(l)). A second or third layer of metallic interconnect can also be added after adding another oxide layer, cutting (via) holes, depositing and patterning the metal.



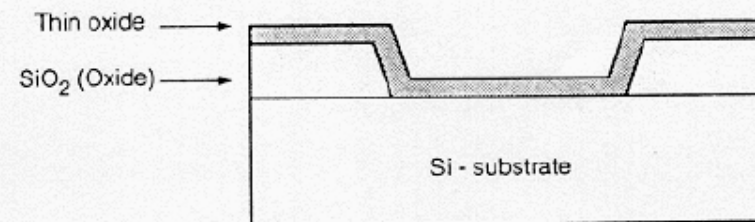
(a)



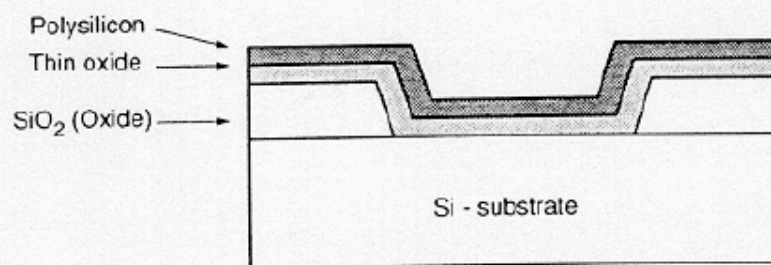
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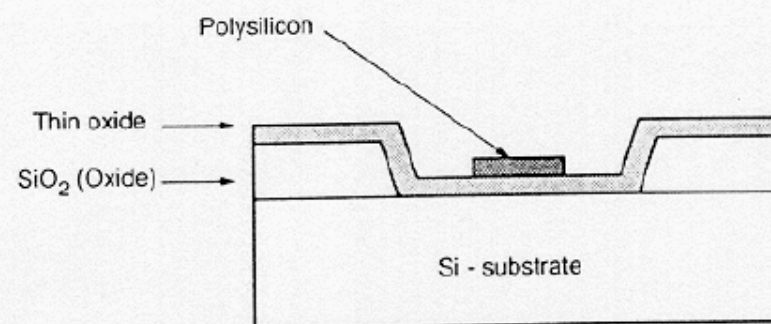
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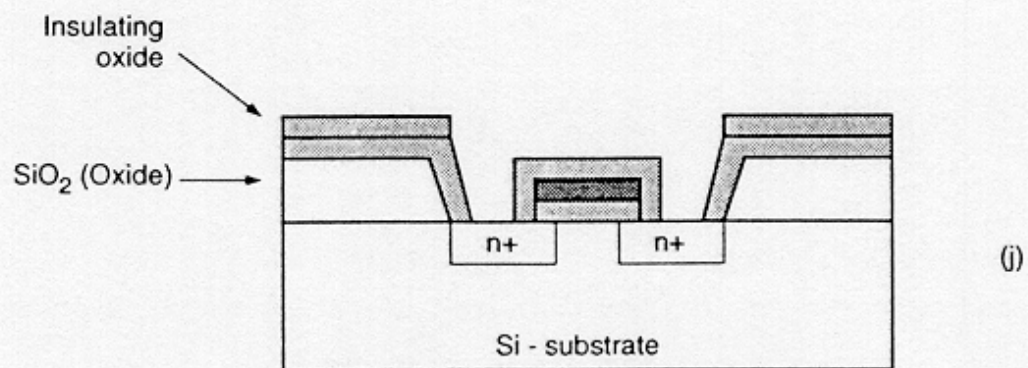
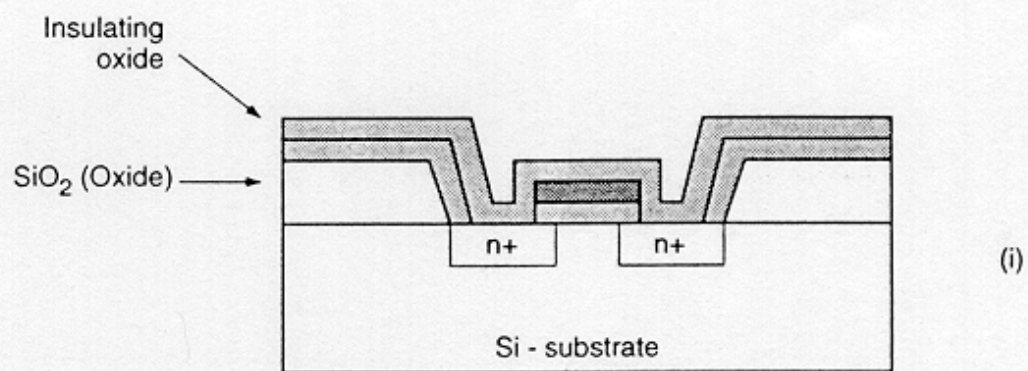
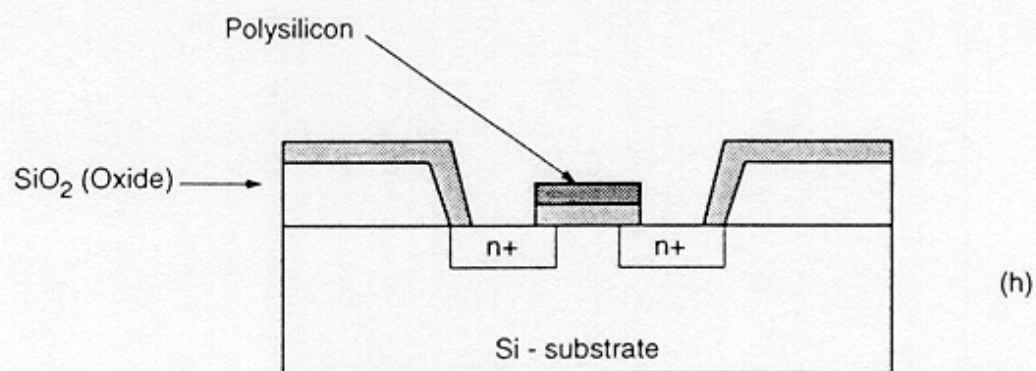
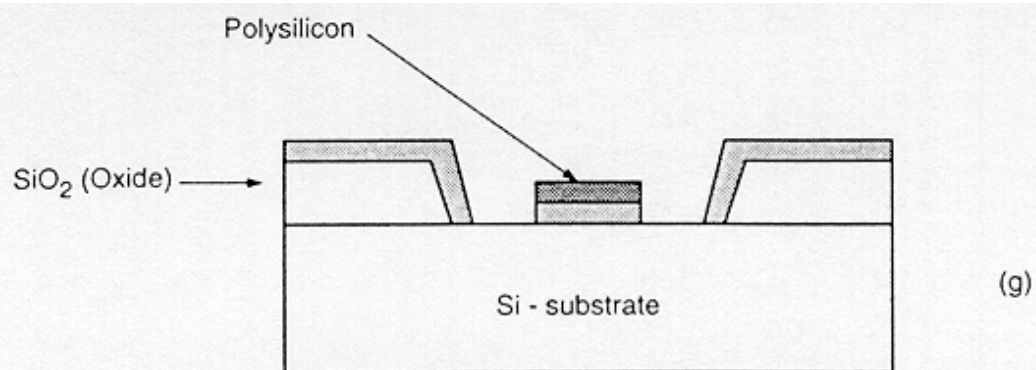


(e)



(f)





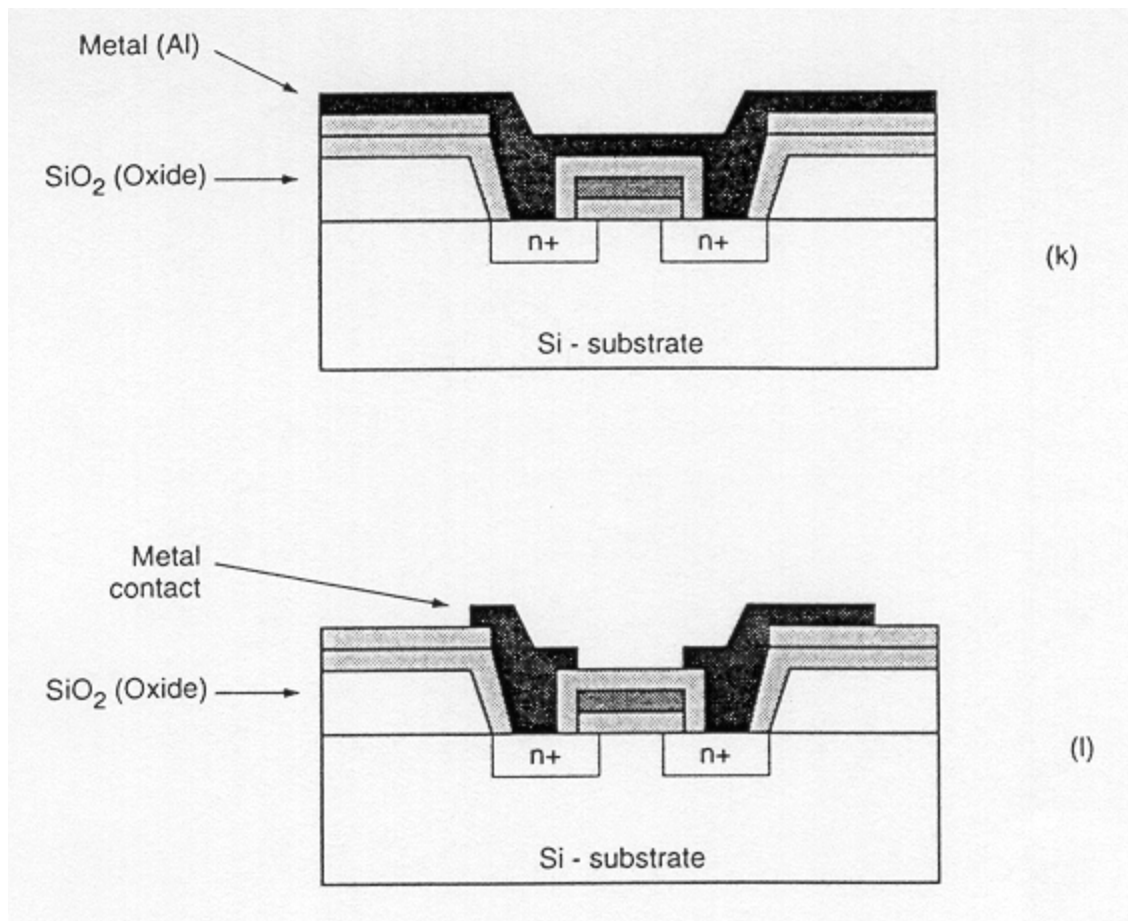
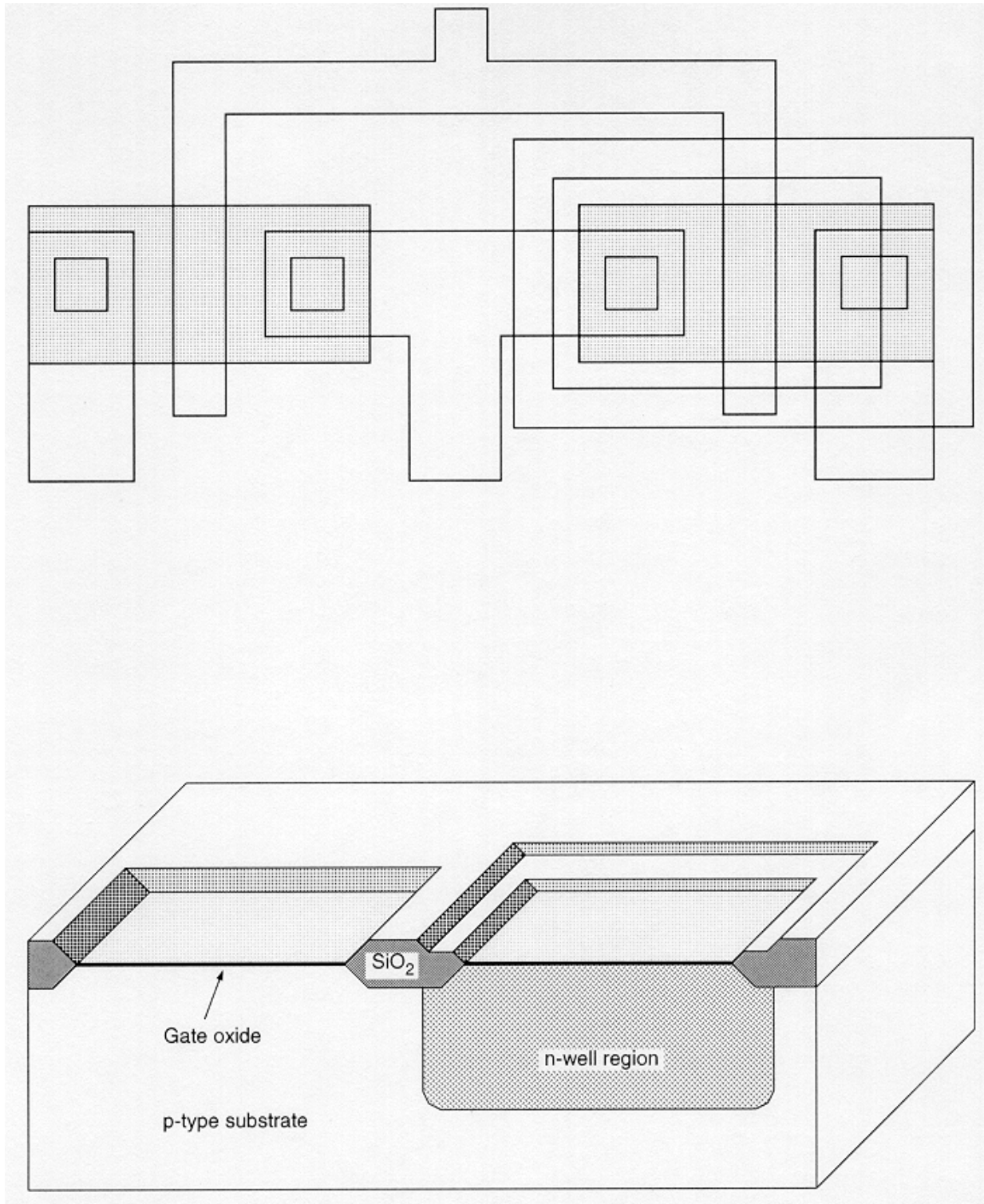


Fig 12.44: Process flow for the fabrication of an n-type MOSFET on p-type silicon

We now return to the generalized fabrication sequence of n-well CMOS integrated circuits. The following figures illustrate some of the important process steps of the fabrication of a CMOS inverter by a top view of the lithographic masks and a cross-sectional view of the relevant areas.

The n-well CMOS process starts with a moderately doped (with impurity concentration typically less than  $10^{15} \text{ cm}^{-3}$ ) p-type silicon substrate. Then, an initial oxide layer is grown on the entire surface. The first lithographic mask defines the n-well region. Donor atoms, usually phosphorus, are implanted through this window in the oxide. Once the n-well is created, the active areas of the nMOS and pMOS transistors can be defined

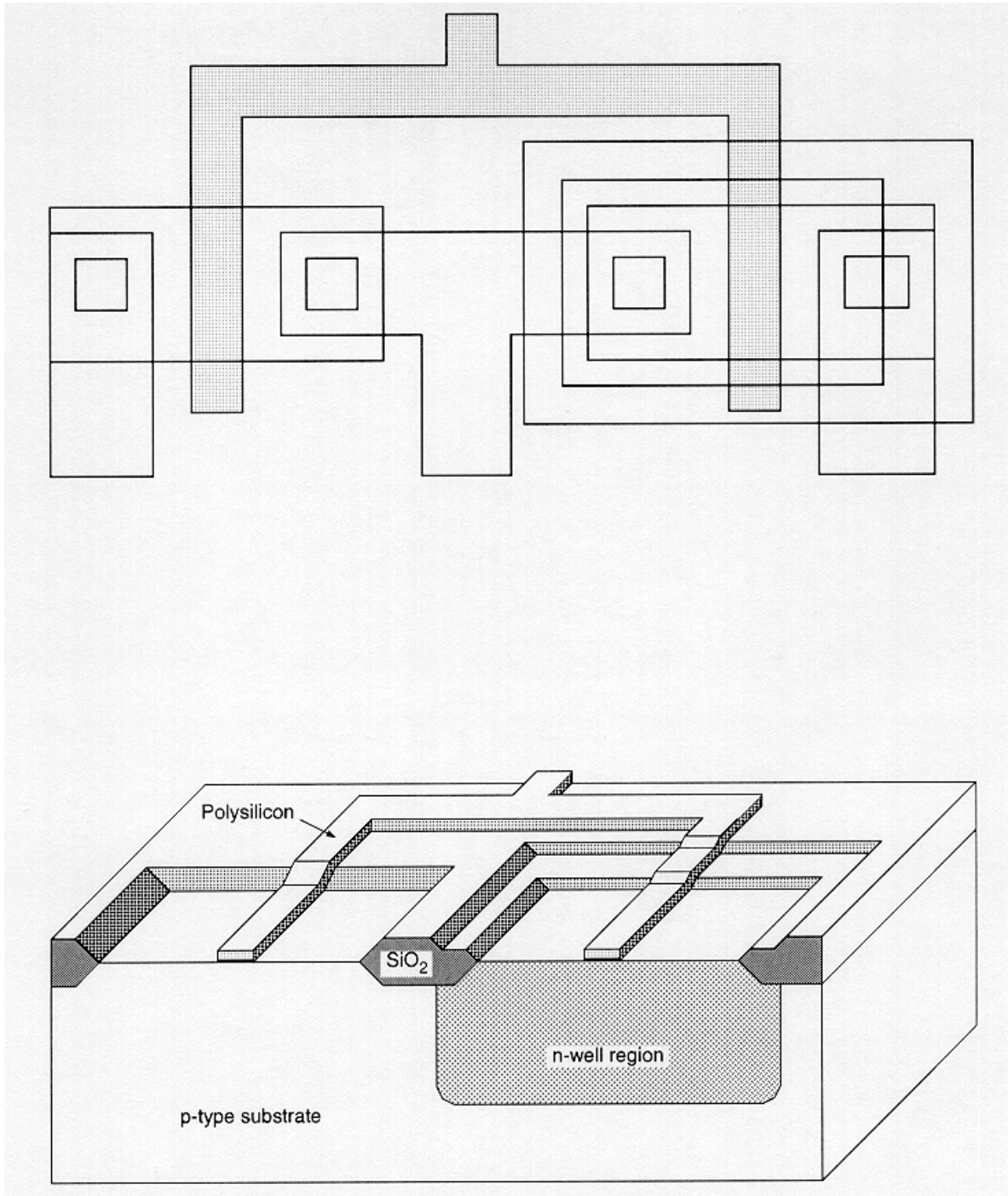


The creation of the n-well region is followed by the growth of a thick field oxide in the areas surrounding the transistor active regions, and a thin gate oxide on top of the active regions. The two most important critical fabrication parameters are the thickness and quality of the gate oxide. These strongly affect the operational characteristics of the MOS transistor, as well as its long-term stability.

Chemical vapor deposition (CVD) is used for deposition of polysilicon layer and patterned by dry (plasma) etching. The resulting polysilicon lines function as the gate electrodes of

the nMOS and the pMOS transistors and their interconnects. The polysilicon gates also act as self-aligned masks for source and drain implantations.

The n+ and p+ regions are implanted into the substrate and into the n-well using a set of two masks. Ohmic contacts to the substrate and to the n-well are also implanted in this process step.

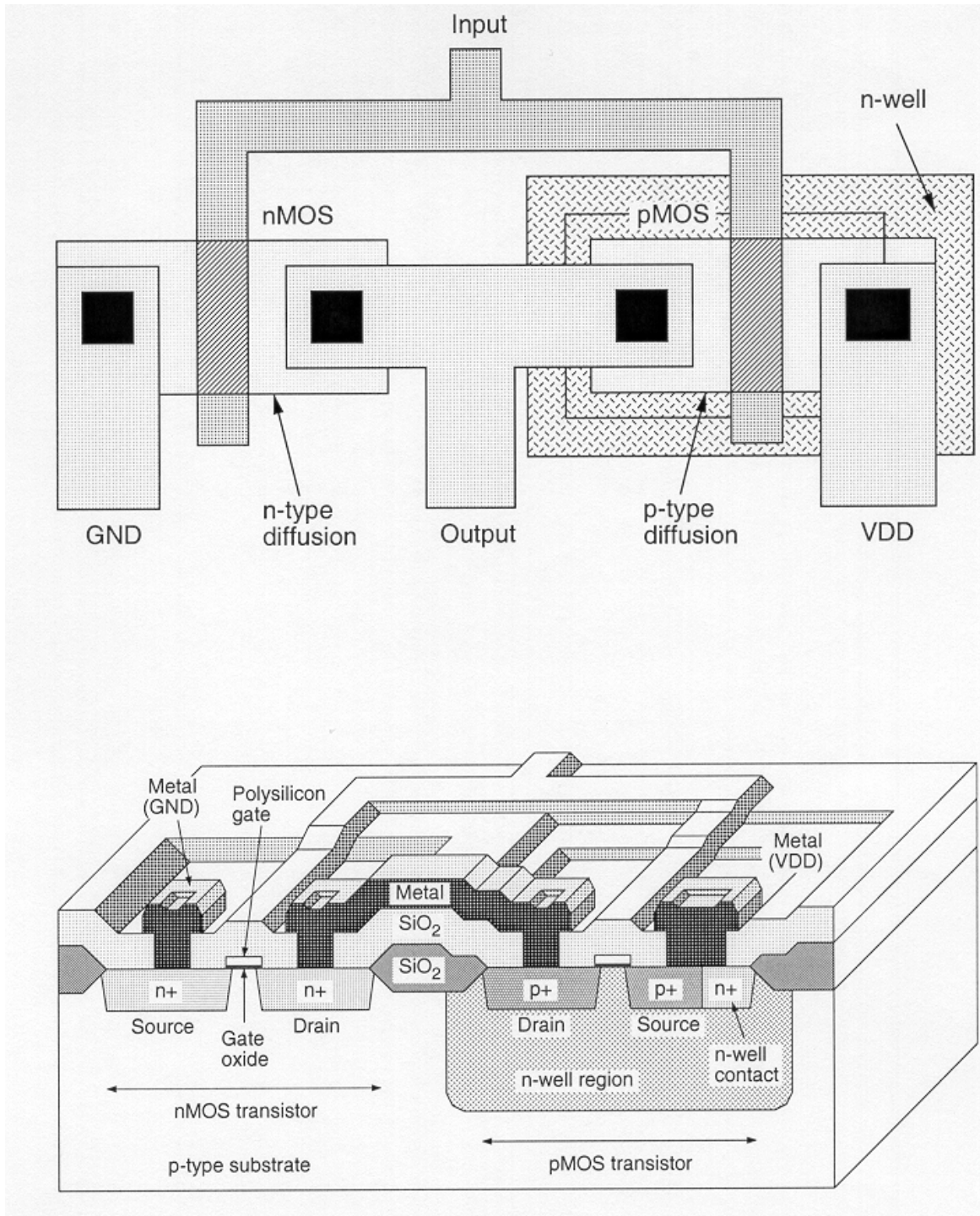


CVD is again used to deposit an insulating silicon dioxide layer over the entire wafer. After this the contacts are defined and etched away exposing the silicon or polysilicon contact windows. These contact windows are essential to complete the circuit interconnections using the metal layer, which is patterned in the next step.

Metal (aluminum) is deposited over the entire chip surface using metal evaporation, and the metal lines are patterned through etching. Since the wafer surface is non-planar, the quality and the integrity of the metal lines created in this step are very critical and are ultimately essential for circuit reliability.

The composite layout and the resulting cross-sectional view of the chip, showing one nMOS and one pMOS transistor (built-in nwell), the polysilicon and metal interconnections. The final step is to deposit the passivation layer (for protection) over the chip, except for wire-bonding pad areas.

This completes the fabrication of the CMOS inverter using n-well technology.





## **Recap**

In this lecture you have learnt the following

- Motivation
- N-well / P-well Technologies
- Silicon on Insulator (SOI)
- Twin well Technology

**Congratulations, you have finished Lecture 12.**