# Module 1 : Introduction to VLSI Design
# Lecture 1 : Motivation of the Course

**Objectives**
In this lecture you will learn the following:
- Motivation of the course
- Course Objectives

## 1.1 Motivation of the course
Why do some circuits work the first time and some circuits take over a year and multiple design iterations to work properly? Why can, for some circuits, the produced quantities easily be ramped up, and for others both circuit and process optimisation is needed. Why are some circuits running red-hot requiring expensive cooling solutions while other circuits, for similar performance, are running from small batteries in hand held gadgets? Why do some companies make money with successful innovations and why do some companies loose hundreds of millions of dollars of revenue just because they did not get their product on market in time.

The answer to these questions is (a lack of) system engineering: analysis and design of a system's relevant electrical parameters. The deep submicron CMOS technologies have moved the bottleneck from device and gate level issues to interconnects and communication (metal wires) bottle necks, where we currently do not have any design automation. This course aims to provide a working knowledge of system electrical issues at chip level related to remove or live with these new bottle-necks (so that the disasters in design can be avoided with proper structures and performance budgeting).

## 1.2 Course Objectives
The course provides for final year undergraduates a solid and fundamental engineering view of digital system operation and how to design systematically well performing digital VLSI systems exceeding consistently, customer expectations and competitor fears. The aim is to teach the critical methods and circuit structures to identify the key 1 % of the circuitry on-chip which dominates the performance, reliability, manufacturability, and the cost of the VLSI circuit. With the current utilisation of the deep submicron CMOS technologies (0.25 micron and below design rules) the major design paradigm shift is associated with the fact that the interconnections (metal Al or Cu wires connecting gates) and the chip communication in general is the main design object instead of active transistors or logic gates. The main design issues defining the make-or-break point in each project is associated with power and signal distribution and bit/symbol communication between functional blocks on-chip and off-chip. In the course we provide a solid framework in understanding:

- Scaling of technology and their impact on interconnects
- Interconnects as design objects
- Noise in digital systems and its impact on system operation
- Power distribution schemes for low noise
- Signal and signalling conventions for on-chip and off-chip communication
- Timing and synchronisation for fundamental operations and signaling

The course objective is to provide the student with a solid understanding of the underlying mechanism and solution techniques to the above key design issues, so that the student, when working as industrial designer, is capable of identifying the key problem points and focus his creative attention and 90% of available resources to right issues for 1% of the circuitry and leave the remaining 99% of circuitry to computer automated tools or unqualified engineers.

**Recap**

In this course you have learnt the following

- Motivation of the course
- Course Objectives