Module 3 : Fabrication Process and Layout Design Rules
Lecture 10 : General Aspects of CMOS Technology

Objectives

In this course you will learn the following

- Gate Material
- Parasitic Capacitances
- Self-aligned silicon gate technology
- Channel Stopper
- Polysilicon deposition
- Oxide Growth
- Active mask or Isolation mask (thin-ox)

10.1 Gate Material

Metals have several advantages when considered as gate electrodes. The use of metal gates would certainly eliminate the problems of dopant penetration through the dielectric and subsequent gate depletion. The use of metals with appropriate work functions for NMOS and PMOS devices would led to transistors with symetrical and tailored threshold voltages. Most refractory metals are good choices for this application primarily due to their high melting points, which allow them to be used at high temperatures necessary for source-drain implant activation. However thermodynamic stability of metal-dielectric interfaces at processing temperatures are major concerns which need to be addressed in addition to more subtle issues of electrical properties, flat band voltage (ultimately threshold voltages) stability and the charge trapping at the interface. The problem with using aluminium is that once deposited, it cannot be subjected to high temperature processes. Copper causes a lot of trap generation when used as a gate material.

10.2 Parasitic Capacitances

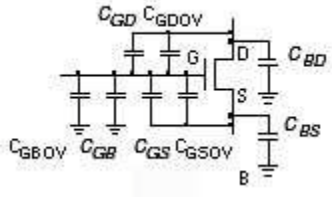

Figure 10.2: Parasitic capacitances in MOSFET

Though a lot of parasitic capacitances exist in a MOSFET as shown in figure 10.2, but those of prime concern to us are the gate to drain capacitance (**Cgd**) and gate to source capacitance (**Cgs**) because they are common to input and output nodes and gate multiplied by gain during circuit operation. Thus they increase the input capacitance drastically and decrease the charging rate.

10.3 Self-aligned Silicon Gate Technology

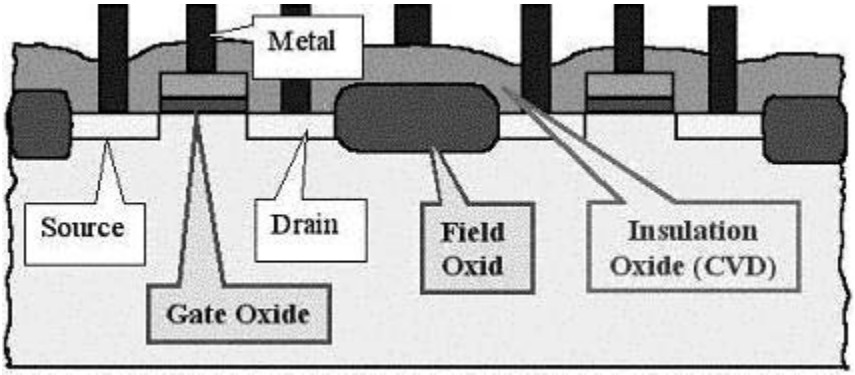

Figure 10.3: Cross sectional view of MOSFET under Selfalgining process

When the metal is used as the gate material, then the source and drain are deposited before the gate and thus to align the gate, mask aligners are used and errors in aligning takes place. In case of polysilicon gate process, the exposed gate oxide (not covered by polysilicon) is etched away and the wafer is subjected to dopant-source or ion-implant which causes source-drain deposition and also these are formed in the regions not covered by polysilicon and thus source and drain donot extend under the gate. This is called self-aligning process.

10.4 Channel Stopper

It is used to prevent the channel formation in the substrate below the field oxide. For example, for a p-substrate, the channel stopper implant would p+ which will increase the magnitude of threshold voltage.

Irregular surfaces can cause "step coverage problems" in which a conductor thins and can even break as it crosses a thick to thin oxide boundary. One of the methods used to remove these irregularities is to pre-etch the silicon in areas where the field oxide is to be grown by around half the final required field oxide thickness. LOCOS (will explain it shortly) oxidation done after this gives the planner field oxide/gate oxide interface.

10.5 Polysilicon Deposition

The sheet resistance of undoped polysilicon is 10^8 ohms/cm and it can be reduced to 30 ohm/cm by heavy doping. The advantage of using polysilicon as gate material is its use as further mask to allow precise definition of source and drain. The polysilicon resistance affects the input resistance of the transistor and thus should be small for improving the RC time constant. For this, higher doping concentration is used.

10.6 Oxide Growth

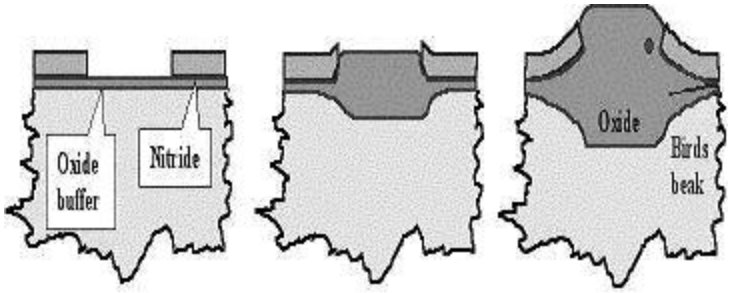

Figure 10.6: Formation of bird's beak in MOSFET

Oxide grown on silicon may result in an uneven surface due to unequal thickness of oxide grown from same thickness of silicon. Stress along the edge of an oxidized area (where silicon has been trenched prior to oxidation to produce a plainer surface) may produce severe damage in the silicon. To relieve this stress, the oxidation temperature must be sufficiently high to allow the stress in the oxide to relieved by viscous flow. In the LOCOS process, the transistor area is masked by **SiO2 / SiN** sandwich and the thick field oxide is then grown. The oxide grows in both the directions vertically and also laterally under the sandwich and results in an encroachment into the gate region called as **bird's beak.**

This reduces the active area of the transistor and specially the width. Some improvements in the LOCOS process produce **Bird's crest** which reduces the encroachments, but it is non-uniform.

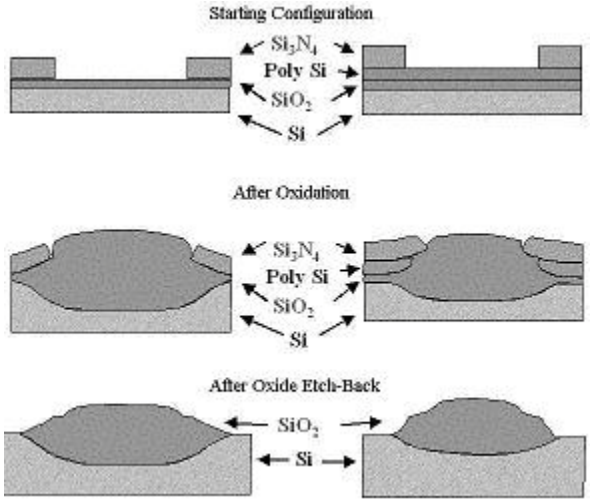

Figure 10.62: Comparison of the LOCOS process
with and without some sacrificial polysilicon

The goal is to oxidize Si only locally, whenever a field oxide is needed. This is necessary for the following reasons:

-- Local oxide penetrates into the **Si,** so the **Si-SiO2**interface is lower than the source-drain regions to be made later. This could not be achieved with oxidizing all of the **Si** and then etching of unwanted oxide.

-- For device performance reasons, this is highly beneficial, if not absolutely necessary.

10.7 Active Mask or Isolation Mask (thin-ox)

It describes the areas where thin oxides are needed to implement the transistor gates and allow implantations to form p/n type diffusions. A thin layer of **SiO_2**is grown and covered with **SiN** and this is used as mask. The **bird's bead** must be taken into account while designing thin-ox.

Recap

In this lecture you have learnt the following

- Gate Material
- Parasitic Capacitances
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Congratulations, you have finished Lecture 10.