Module 4 : Propagation Delays in MOS
Lecture 19 : Analyzing Delay for various Logic Circuits

Objectives

In this lecture you will learn the following

- Ratioed Logic
- Pass Transistor Logic
- Dynamic Logic Circuits

19.1 Ratioed Logic

Instead of combination of active pull down and pull up networks such a gate consists of an NMOS pull down network that realizes the logic function and a simple load device. For an inverter PDN is single NMOS transistor.

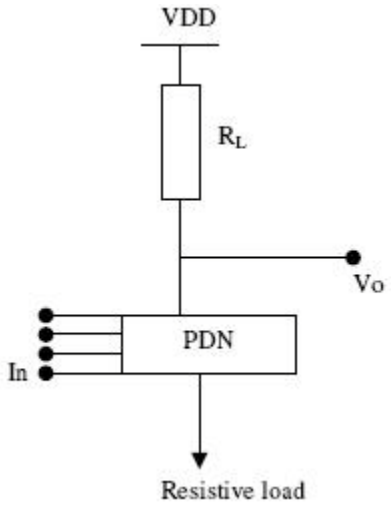


Fig 19.1: Ratioed Logic Circuit

The load can be a passive device, such as a resistor or an active element as a transistor. Let us assume that both PDN and load can be represented as linearized resistors. The operation is as follows: For a low input signal the pull down network is off and the output is high by the load. When the input goes high the driver transistor turns on, and the resulting output voltage is determined by the resistive division between the impedances of pull down and load network:

$$V_{OL} = R_D V_{DD} / (R_D + R_L)$$

where R_D = pulldown n/w resistance, R_L = load resistance.

To keep the low noise margin high it is important to chose $R_L >> R_D$. This style of logic therefore called ratioed, because a careful **PDN** scaling of impedances (or transistor sizes) is required to obtain a workable gate. This is in contrast to the ratioless logic style

as complementary CMOS, where the low and high level don't depend upon transistor sizes. As a satisfactory level we keep **RL>=4RD**. To achieve this, $(W/L)_D/(W/L)_L > 4$.

19.2 Pass Transistor Logic

The fundamental building block of nMOS dynamic logic circuit, consisting of an nMOS pass transistor is shown in figure 19.21.

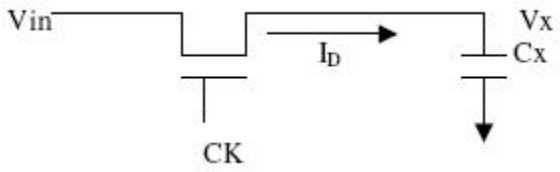


Fig 19.21: Pass Transistor Logic Circuit

The pass transistor MP is driven by the periodic clock signal and acts as an access switch to either charge up or down the parasitic capacitance, **C**x, depending on the input signal **V**in. Thus there are 2 possible operations when the clock signal is active are the logic "**1**" transfer(charging up the capacitance **C**x to logic high level) and the logic "**0**" transfer(charging down the capacitance **C**x to a logic low level). In either case, the output of the depletion load of the nMOS inverter obviously assumes a logic low or high level, depending on the voltage **V**x. The pass transistor MP provides the only current path to the intermediate capacitive node X. when clock signal becomes inactive **(clk=0)** the pass transistor ceases to conduct and the charge is stored in the parasitic capacitor **C**x continues to determine the output level of the inverter. Logic "1" Transfer: Assume that the **V**x **= 0** initially. A logic "**1**"level is applied to the input terminal which corresponds to **V**in=**V**OH**=V**DD. Now the clock signal at the gate of the pass transistor goes from **0** to **V**DD at **t=0**. It can be seen that the pass transistor starts to conduct and operate in saturation throughout this cycle since VDS=VGS. Consequently **V**DS**>** **V**GS**V**tn.

Analysis: The pass transistor operating in saturation region starts to charge up the capacitor **C**x, thus:

$$C_x(dV_x/dt) = (k_n/2)(V_{DD} - V_x - V_{tn})^2 \Rightarrow \int_0^t dt = (2C_x/k_n)\int_0^{V_x} dV_x/(V_{DD} - V_x - V_{tn})^2$$

$$\text{So,} \quad t = (2C_x/k_n)[1/(V_{DD} - V_x - V_{tn}) - 1/(V_{DD} - V_{tn})]$$

The previous equation for **Vx(t)** can be solved as-

$$V_x(t) = (V_{DD} - V_{tn})\frac{(k_n/2C_x)(V_{DD} - V_{tn})t}{1 + (k_n/2C_x)(V_{DD} - V_{tn})t}$$

The variation of the node voltage **Vx(t)**is plotted as a function of time in fig. 19.22. The voltage rises from its initial value of **0** and reaches **Vmax =VDD-Vtn** after a large time. The pass transistor will turn off when **V**x = **V**max. Since **Vgs= Vtn**. Therefore **Vx** can never attain **VDD** during logic **1** transfer. Thus we can use buffering to overcome this problem.

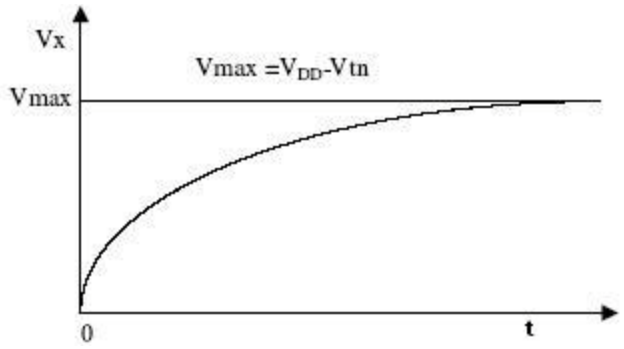


Fig 19.22: Node Voltage Vx vs t

Logic "0" Transfer: Assume that the ***Vx=1***
Initially. A logic"**0**" level is applied to the input terminal which corresponds to ***Vin=1***. Now the clock signal at the gate of the pass transistor goes from **0** to **VDD** at **t=0**. It can be seen that the pass transistor starts to conduct and operate in linear mode throughout this cycle and the drain current flows in the opposite direction to that of charge up.

Analysis: We can write –

$$-C_x(dV_x/dt) = (k_n/2)[(V_{DD} - V_{tn})V_x - V_x^2] \Rightarrow \int_0^t dt = -(C_x/k_n)\int_0^{V_x} dV_x/[(V_{DD} - V_{tn})V_x - V_x^2]$$

So, $$t = (C_x/k_n)\ln[2((V_{DD} - V_{tn}) - V_x)/V_x]$$

The above equation for **Vx(t)** can be solved as –

$$V_x(t) = \frac{2(V_{DD} - V_{tn})}{1 + e^{(k_n/C_x)t}}$$

Plot of **Vx(t)** is shown in figure 19.23.

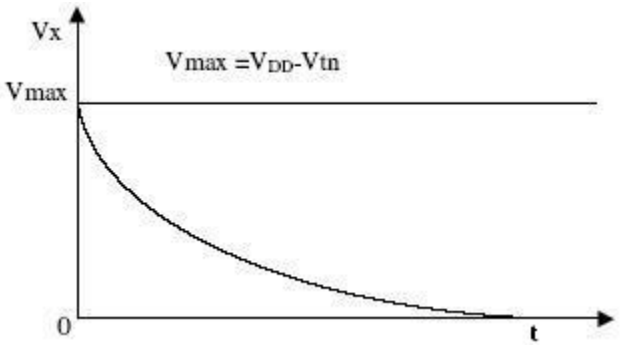


Fig 19.22: Node Voltage Vx vs t

19.3 Dynamic Logic Circuits

In case of static CMOS for a fan-in of **N**, **2N** transistors are required. In order to reduce this, various other design logics were used like pseudo-NMOS logic and pass transistor logic. However the static power consumption in these cases increased. An alternative to

these design logics is **Dynamic logic**, which reduces the number of transistors at the same time keeps a check on the static power consumption.

Principle: A block diagram of a dynamic logic circuit is as shown in fig 19.31. This uses NMOS block to implement its logic

The operation of this circuit can be explained in two modes.

1. Precharge
2. Evaluation

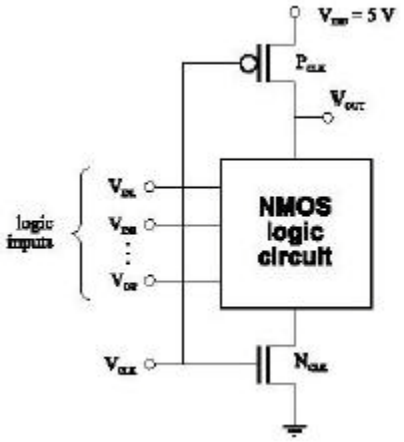
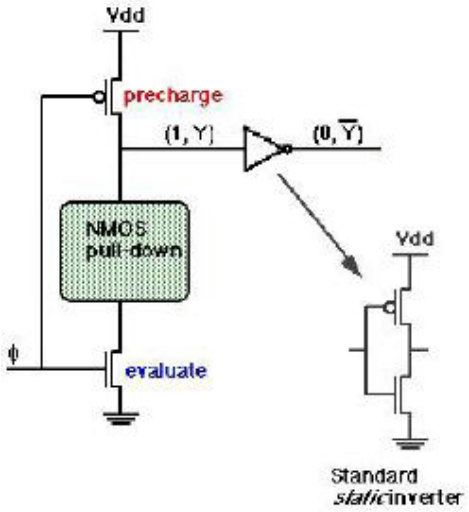


Fig 19.31: Dynamic CMOS Block Diagram

In the precharge mode, the **CLK** input is at logic **0**. This forces the output to logic **1**, charging the load capacitance to **VDD**. Since the NMOS transistor **M1** is off the pulldown path is disabled. There is no static consumption in this case as there is no direct path between supply and ground.

In the evaluation mode, the **CLK** input is at logic **1**. Now the output depends on the PDN block. If there exists a path through PDN to ground (i.e. the PDN network is **ON**), the capacitor **CL** will discharge else it remains at logic **1**.As there exists only one path between the output node and a supply rail, which can only be ground, the load capacitor can discharge only once and if this happens, it cannot charge until the next precharge operation. Hence the inputs to the gate can make at most one transition during evaluation



19.32: DOMINO CMOS Block Diagram

Advantages of dynamic logic circuits:

1. As can be seen, the number of transistors required here are **N+2** as compared to **2N** in the Static CMOS circuits.
2. This circuit is still a ratioless circuit as in Static case. Hence, progressive sizing and ordering of the transistors in the PDN block is important.
3. As can be seen, the static power loss is negligible.

Disadvantages of dynamic logic circuits:

1. The penalty paid in such circuits is that the clock must run everywhere to each such block as shown in the diagram.
2. The major problem in such circuits is that the output node is at Vdd till the end of the precharge mode. Now if the **CLK** in the next block arrives earlier compared to the **CLK** in this block, or the PDN network in this block takes a longer time to evaluate its output, then the next block will start to evaluate using this erroneous value

The second part of the disadvantage can be eliminated by using **DOMINO CMOS** circuits which are as shown below.
As can be seen the output at the end of precharge is inverted by the inverter to logic 0. Thus the next block will not be evaluated till this output has been evaluated. As an ending point, it must be noted that this also has a disadvantage that since at each stage the output is inverted, the logic must be changed to accommodate this.

Recap

In this lecture you have learnt the following

- Ratioed Logic
- Pass Transistor Logic
- Dynamic Logic Circuits

Congratulations, you have finished Lecture 19.