Module 6 : Semiconductor Memories
Lecture 30 : SRAM and DRAM Peripherals

Objectives

In this lecture you will learn the following

- Introduction
- SRAM and its Peripherals
- DRAM and its Peripherals

30.1 Introduction

Even though a lot of the concepts here have been discussed earlier, they are repeated for convenience.
Broadly memories can be classified into

- RAM (Random Access Memory)
- Serial Memory

A RAM is one in which the time required for accessing the information and retrieving the information is independent of the physical location of the information. In contrast, in a Serial memory, the data is available only in the same form as it was stored previously.

The following diagram shows the organization of a Memory

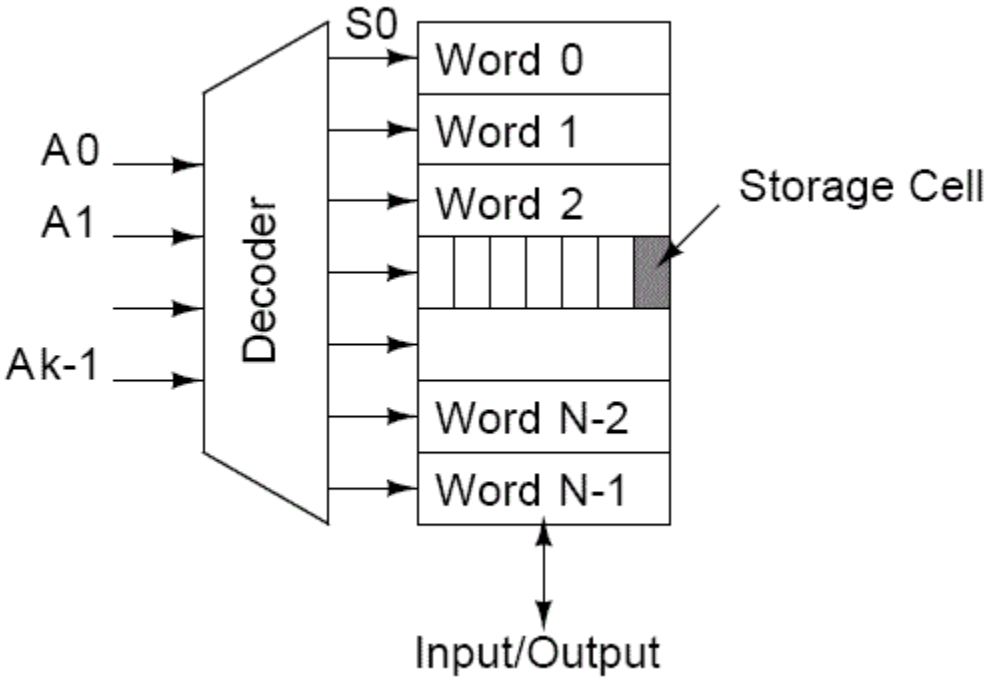

Fig 30.11: Organization of Memory

This memory consists of two address decoders viz. Row and Column decoders to select a particular bit in the memory. If there are **M** rows and **N** columns, then the number of

bits that can be accessed are 2^{M+N}. Either a **read** operation or a **write** operation can be done on any selected bit by the use of control signals.

RAMs are once again classified into two types:

- SRAM (Static RAM)
- DRAM (Dynamic RAM)

30.2 SRAM and Its Peripherals

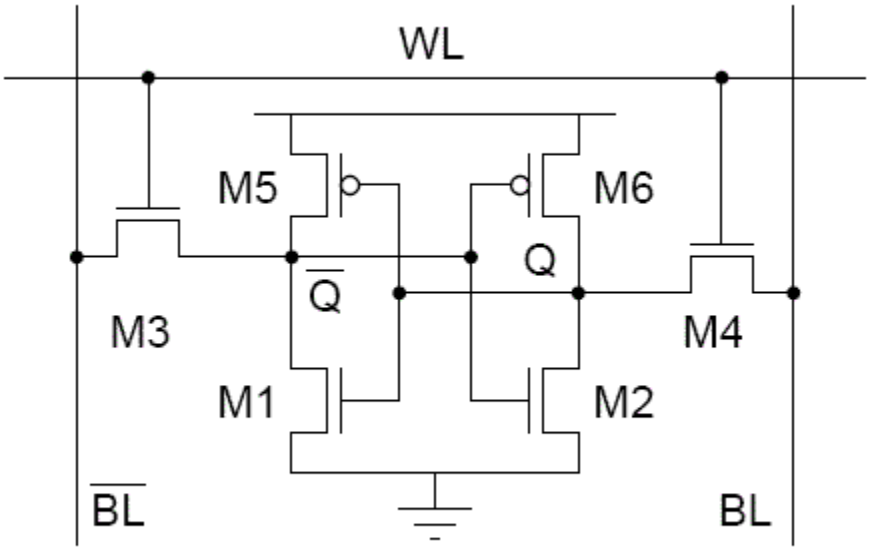

Fig 30.21: SRAM Cell

Figure 30.21 shows a standard **6** transistor SRAM cell. The signal designed as **WL** is the **WORDLINE** used to read or write into the cell. BL and $\overline{BL}$ are the data to be written into the cell.

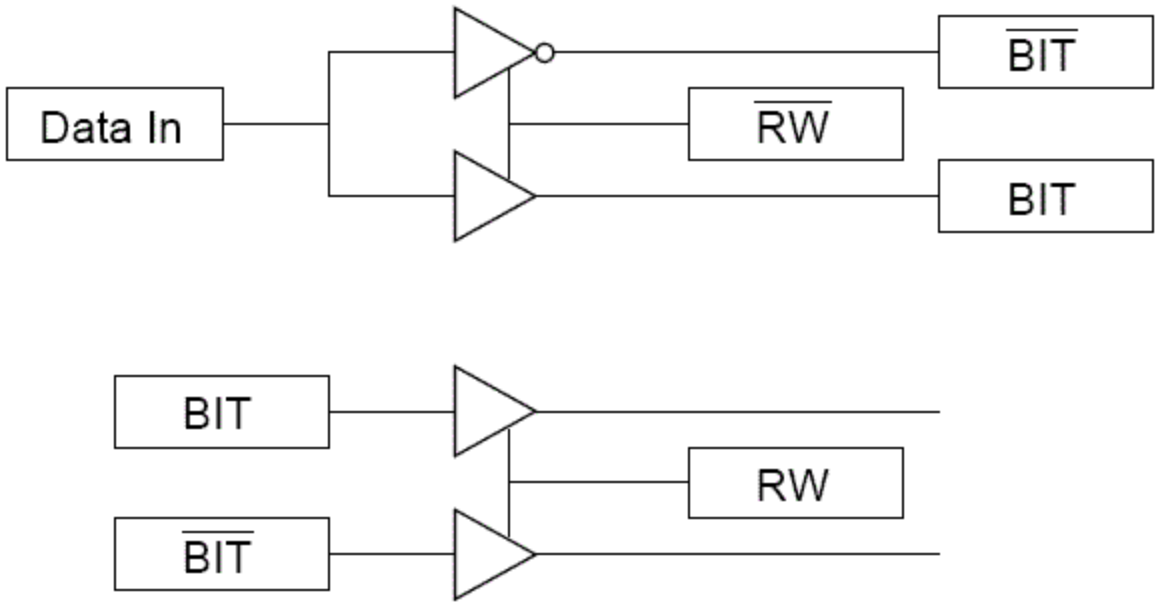

Fig 30.22: Circuit for reading and writing data into cell

The circuits shown in the previous page are used to write and read the data to and from the cell. When a read operation is to be performed, RW signal is made HIGH and $\overline{RW}$ at the same time is made LOW. As a result the data present on the BIT and $\overline{BIT}$ lines are transferred to the input of the sense amplifier (Sense amplifier operation will be discussed shortly). The sense amplifier then senses the data and gives the output.

During the write operation**,** RW is made LOW and $\overline{RW}$ is made HIGH. Thus the $DATA$ and $\overline{DATA}$ will be written onto the BIT and $\overline{BIT}$ lines respectively.

However the read and write operation on a particular cell takes place only if the cell is enabled by the corresponding row(Word) and column(Digit) lines. It is important to remember that before every read operation, the BIT and $\overline{BIT}$ are precharged to a voltage (usually VDD/2). During read operation, one of the two BIT (BIT or $\overline{BIT}$) lines discharges slightly whereas the other line charges to a voltage slightly greater than its precharged value. This difference in these voltages is detected by the sense amplifier to produce and output voltage, which corresponds to the stored value in the cell which is read. Care should be taken in sizing the transistors to ensure that the data stored in the cell does not change its value.

30.3 Sense Amplifier

The circuit shown in Figure 30.31 is the sense amplifier used to read data from the cell. As soon as the **SE** signal goes HIGH the amplifier senses the difference between the BIT and $\overline{BIT}$ voltages and produces an output voltage appropriately. The access time of the memory, which is defined as the time between the initiation of the read operation and the appearance of the output, mainly depends on the performance of the sense amplifier. So the design of the sense amplifier forms the main criteria for the design of memories. The one that is shown here is a simple sense amplifier.

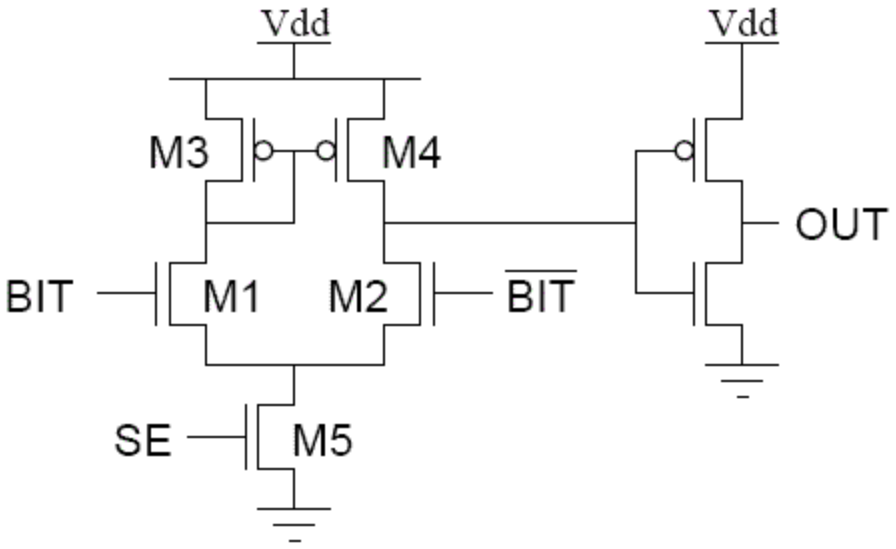

Fig 30.31: Differential Sense Amplifier

Figure 30.31 shows the block diagram of a memory cell with all the peripherals

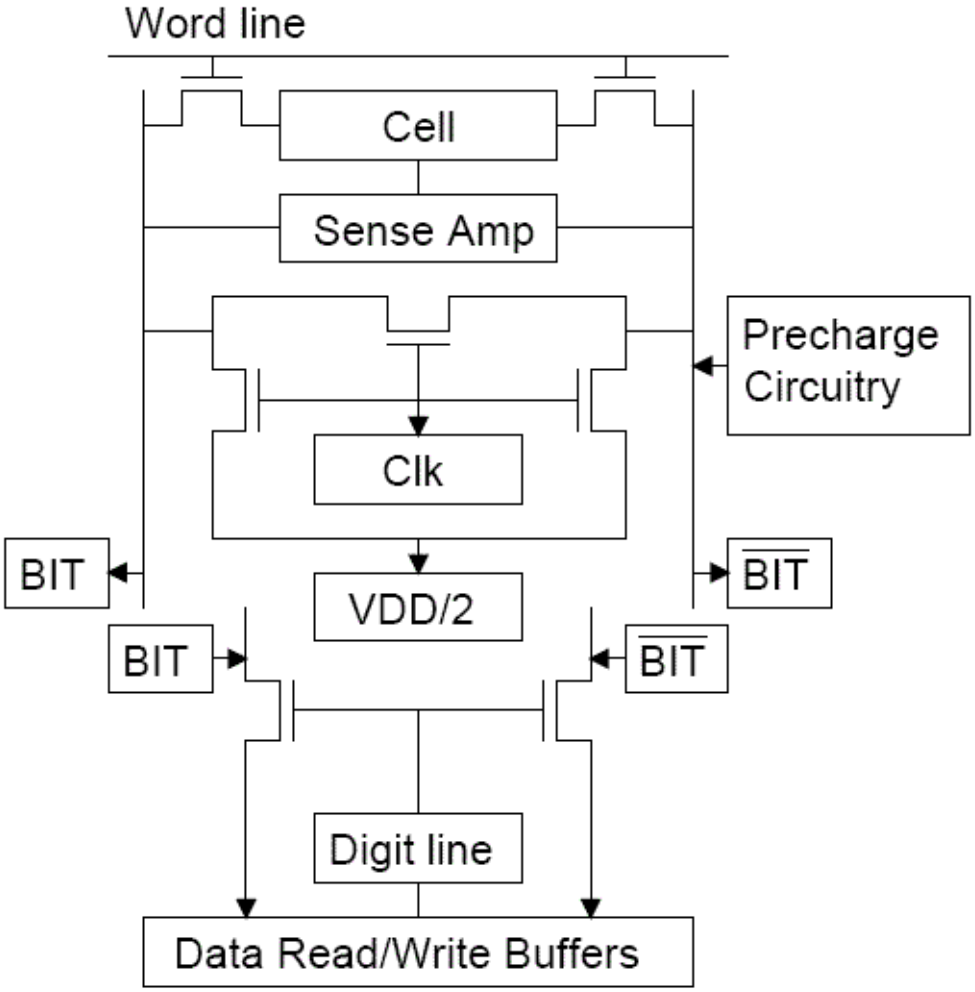

Fig 30.32: Block Diagram Of A Memory Cell With All Its Peripherals

30.4 Another Type of Sensing

Figure 30.41 illustrates the SRAM sensing scheme.

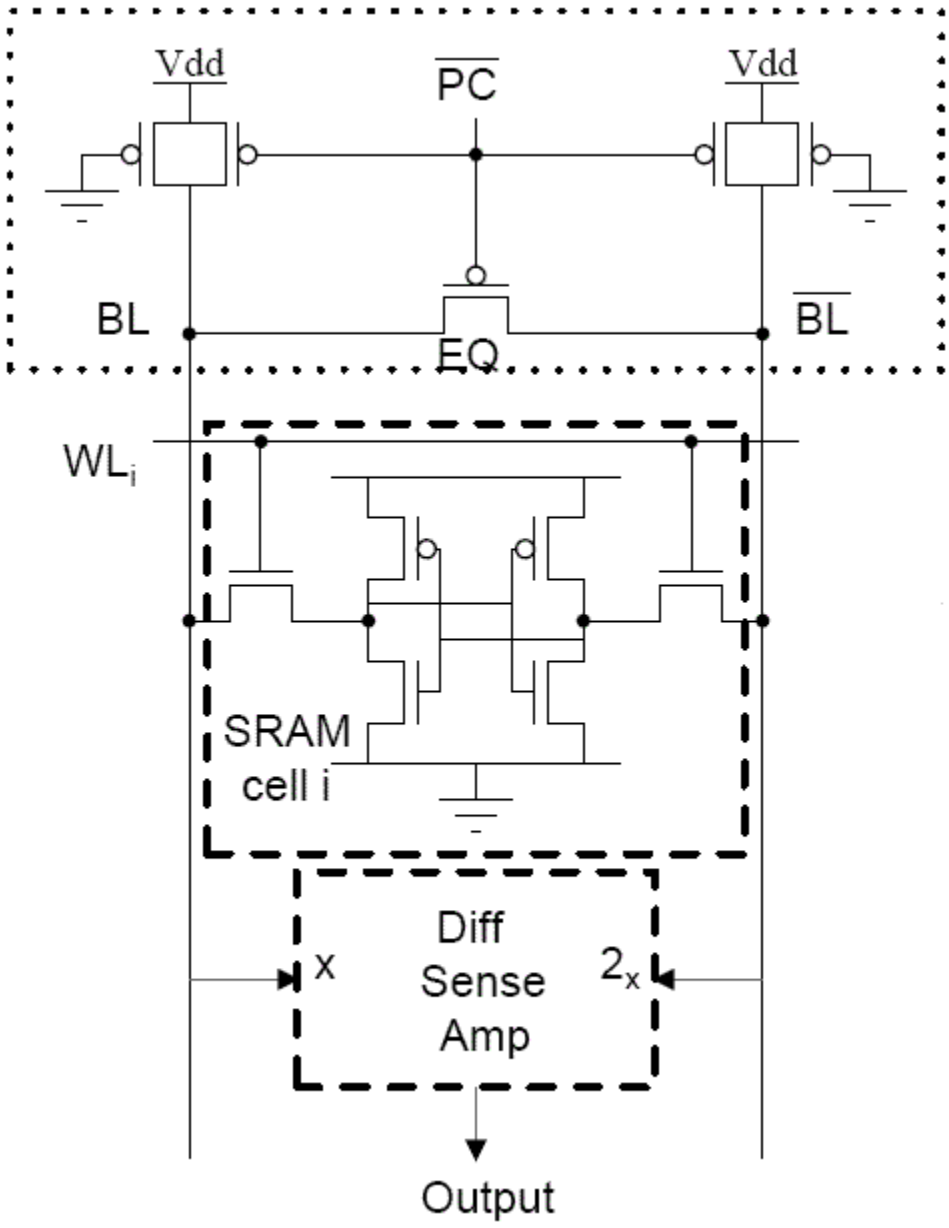

Fig 30.41: SRAM Sensing Scheme

In the above figure, $\overline{PC}$ is the signal used to precharge the BIT and $\overline{BIT}$ lines before every read operation. The transistor labelled **EQ** is the equalization transistor to ensure equal voltages on BIT and $\overline{BIT}$ lines after precharge. **SE** is the sense enable signal used to sense the voltage difference between the BIT and $\overline{BIT}$ lines.

As mentioned earlier, the access time of the memory mainly depends on the performance of the sense amplifier. In contrast with the simple sense amplifier shown

earlier, Figure 30.42 shows an amplifier which is somewhat complicated to improve the performance.

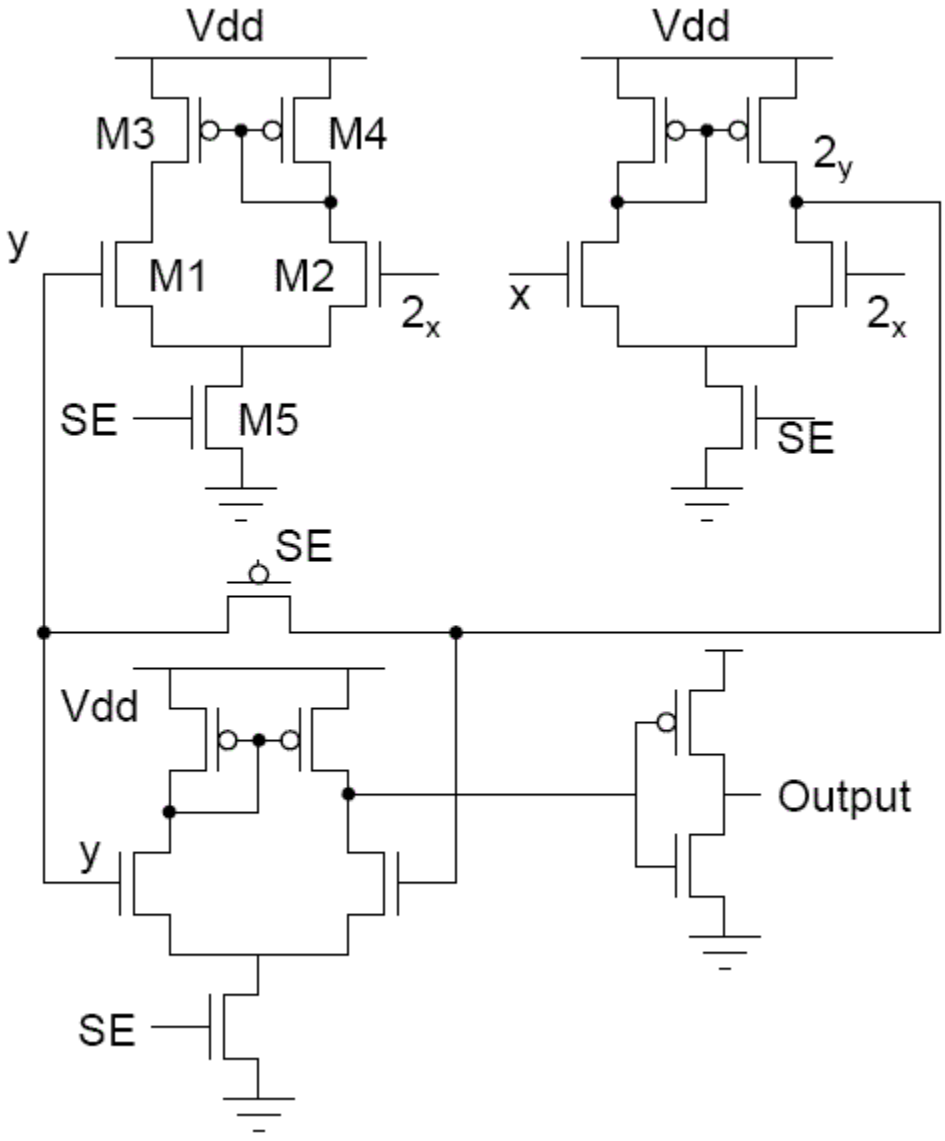

Fig 30.42: Two Stage Differential Amplifier

30.5 DRAM and Its Peripherals

The circuit shown in Figure 30.51 is the simple DRAM circuit. Charge sharing takes place between the two capacitors during read and write operations in the following manner. During the write cycle, $\mathbf{C_S}$ is charged or discharged by asserting **WL** and **BL**. During the read cycle, charge redistribution takes place between the bit line and the storage capacitance.

$$\Delta V = V_B - V_{PR} = V_{BL} - V_{PR} \frac{C_s}{C_S + C_B} \quad \textbf{(Eq 30.1)}$$

Voltage swing is small; typically around 250mV.
Figure 30.52 shows a simple 3-transistor DRAM cell.

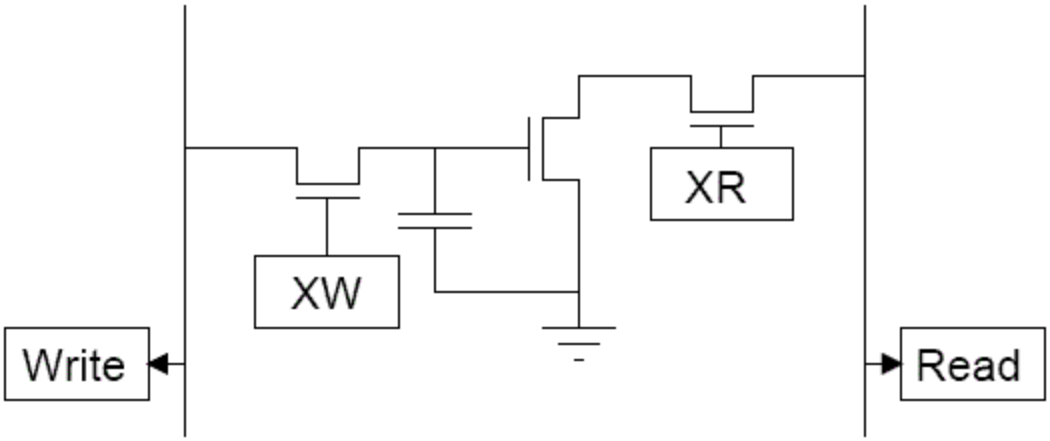

Fig 30.52: 3-Transistor DRAM Cell

Figure 30.53 shows a very simple address decoder. These address decoders are compulsory in case of main memories. But the cache memories avoid the usage of address decoders. Many other possible architectures are available for address decoding.

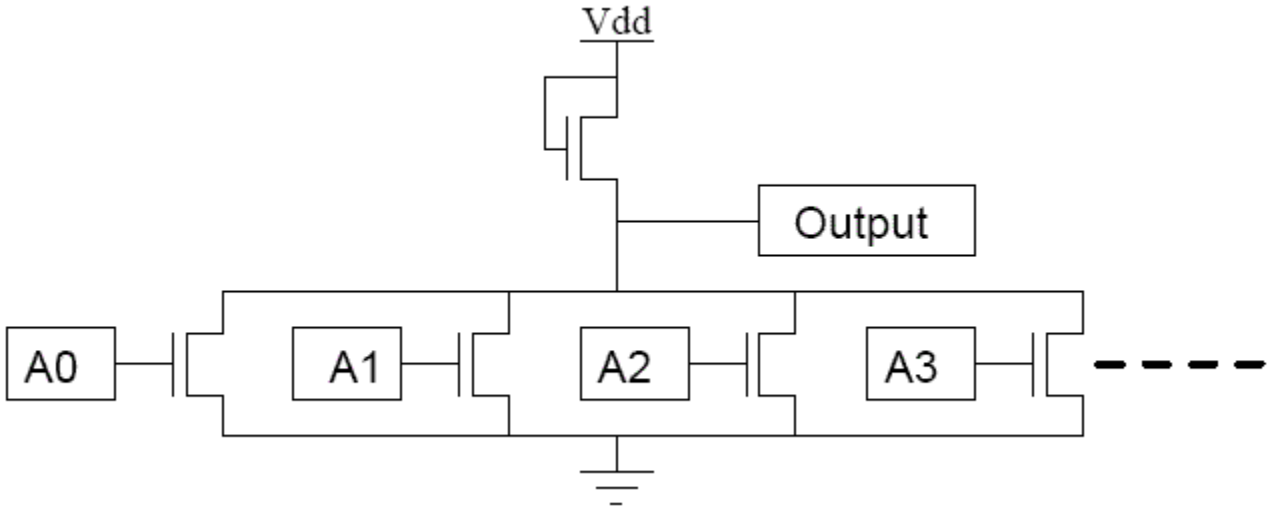

Fig 30.53: A Simple Address Decoder

Recap

In this lecture you have learnt the following

- Introduction
- SRAM and its Peripherals
- DRAM and its Peripherals

Congratulations, you have finished Lecture 30.