Module 3 : Fabrication Process and Layout Design Rules
Lecture 9 : Introduction to Fabrication Process

Objectives

In this course you will learn the following

- Motivation
- Photolithography
- Fabrication Process

9.1 Motivation

In the previous module, we did a detailed study about the MOSFET. VLSI circuits are very complex circuits i.e we cannot make circuits by interconnecting few single MOSFET transistors. A VLSI circuit consists of millions to billions of transistors. For this purpose, we use **Photolithography** which is a method/technology to create the circuit patterns on a silicon wafer surface and the process is called **Fabrication.**

In this lecture, we will study in detail photolithography, how it is done and what sort of materials are used for this purpose.

9.2 Photolithography

Photolithography is the method that sets the surface dimensions (horizontal) of various parts of devices and circuits. Its goal is two fold. **First goal** is to create in and on the wafer surface a pattern whose dimensions are as close to the device requirements as possible. This is known as **resolution of images** on the wafer and the pattern dimensions are known as **feature or image sizes** of the circuit. **Second goal** is the correct placement called **alignment** or **registration** of the circuit patterns on the wafer. The entire circuit patterns must be correctly placed on the wafer surface because misaligned mask layers can cause the entire circuit to fail.

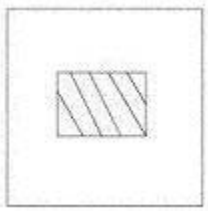


Figure 9.1: Clear Field mask

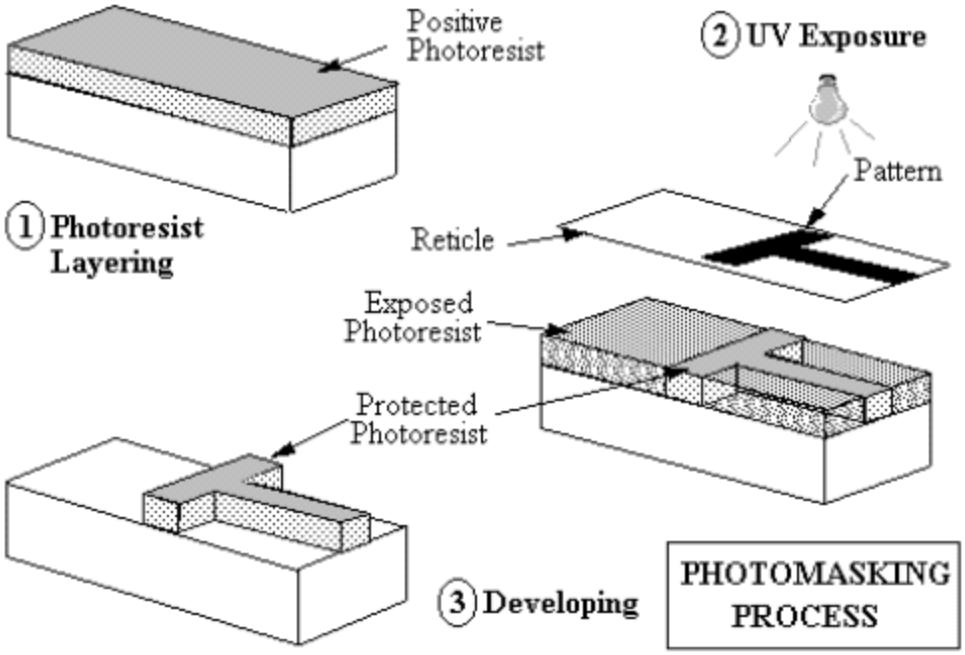
Figure 9.2: Dark Field mask

In order to create patterns on the wafer, the required pattern is first formed in the **reticles** or **photomasks**. The pattern on reticle or mask is then transfered into a layer of **photoresist**. Photoresist is a light sensitive material similar to the coating on a regular photographic film. Exposure to light causes changes in its structure and properties. If the exposure to light causes photoresist to change from a soluble to insoluble one, it is known as **negative acting**and the chemical change is called **polymerization.** Similarly, if exposure to light causes it change from relatively non-soluble to much more soluble, it is known as **positive acting** and the term describing it is called as **photosolubilisation.** The exposure radiation is generally **UV** and **E-beam.** Removing the soluble portions with chemical solvents called **developers** leaves a pattern on the photoresist depending upon the type of mask used. A mask whose pattern exists in the opaque regions is called **clear field mask**. The pattern could also be coded in reverse, and such masks are known as **dark field masks**.

The result obtained from the photomasking process from different combinations of mask and resist polarities is shown in the following table:

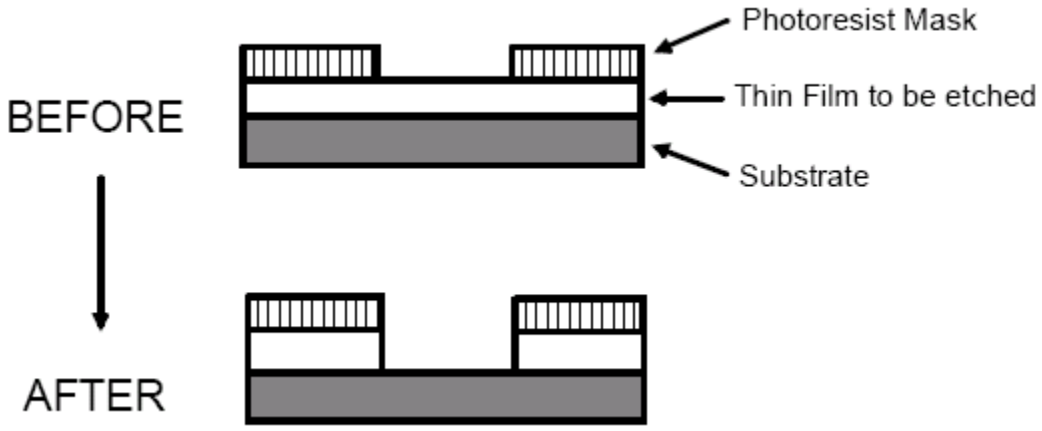
	Photoresist Polarity	
	Negative	Positive
Clear Field	Hole	Island
Dark Field	Island	Hole

The second transfer takes place from the photoresist layer into the wafer surface layer. The transfer occurs when etchants remove the portion of the wafer's top layer that is not covered by the photoresist. The chemistry of the photoresists is such that they do not dissolve in the chemical etching solutions; they are **etch resistant**; hence the name **photoresists**.The etchant generally used to remove silicon dioxide is hydrogen fluoride (**HF**).



The choice of mask and resist polarity is a function of the level of dimensional control and defect protection required to make the circuit work. For example, sharp lines are not obtainable with negative photoresists while etchants are difficult to handle with positive photoresists.

After the pattern has been taken on resist, the thin layer needs to be etched. Etching process is used to etch into a specific layer the circuit pattern that has been defined during the photomasking process. For example, aluminium connections are obtained after etching of the aluminium layer.



9.3 Fabrication Process

Why polysilicon gate?

The most significant aspect of using polysilicon as the gate electrode is its ability to be used as a further mask to allow precise definition of source and drain regions. This is achieved with minimum gate to source/drain overlap, which leads to lower overlap capacitances and improved circuit performance.

Procedure:

1. A thick layer of oxide is grown on the wafer surface which is known as **field oxide (FOX)**. It is much thicker than the gate oxide. It acts as shield which protects the underlying substrate from impurities when other processes are being carried out on the wafer. Besides, it also aids in preventing conduction between unrelated transistor source/drains. In fact, the thick FOX can act as a gate oxide for a parasitic MOS transistor. The threshold voltage of this transistor is much higher than that of a regular transistor due to thick field oxide. The high threshold voltage is further ensured by introducing **channel-stop** diffusion underneath the field oxide, which raises the impurity concentration in the substrate in the areas where transistors are not required.

2. A window is opened in the field oxide corresponding to the area where the transistor is to be made. A thin highly controlled layer of oxide is deposited where active transistors are desired. This is called **gate oxide** or **thinox.** A thick layer of silicon dioxide is required elsewhere to isolate the individual transistors.

3. The thin gate oxide is etched to open windows for the source and drain diffusions. Ion implantation or diffusion is used for the doping. The former tends to produce shallower junctions which are compatible with fine dimension processes. As the diffusion process occurs in all directions, the deeper a diffusion is the more it spreads laterally. This lateral spread determines the overlap between gate and source/drain regions.

4. Next, a gate delineation mask is used to determine the gate area. There has to be minimum overlap between gate and source/drain regions. This is referred to as **self-aligned** process because source and drain do not extend under the gate. Polysilicon is then deposited over the oxide.

5. The complete structure is then covered with silicon dioxide and contact holes are etched using contact window mask down to the surface to be contacted. These allow metal to contact diffusion or polysilicon regions.

6. Metallization is then applied to the surface using interconnect mask and selectively etched to produce circuit interconnections.

7. As a final step, the wafer is passivated and openings to the bond pads are etched to allow for wire bonding. Passivation protects the silicon surface against the ingress of contaminants than can modify circuit behavior.

Recap

In this lecture you have learnt the following

- Motivation
- Photolithography
- Fabrication Process

Congratulations, you have finished Lecture 9.