

## Module 2 : MOSFET

### Lecture 8 : Short Channel Effects

#### Objectives

In this course you will learn the following

- Motivation
- Mobility degradation
- Subthreshold current
- Threshold voltage variation
- Drain induced barrier lowering (DIBL)
- Drain punch through
- Hot carrier effect
- Surface states and interface trapped charge

#### 8.1 Motivation

As seen in the last lecture as channel length is reduced, departures from long channel behaviour may occur. These departures, which are called **Short Channel Effects**, arise as results of a two-dimensional potential distribution and high electric fields in the channel region.

For a given channel doping concentration, as the channel length is reduced, the depletion layer widths of source and drain junctions become comparable to channel length. The potential distribution in the channel now depends on both the transverse field  **$E_x$** (controlled by the gate voltage and back-surface bias) and the longitudinal field  **$E_y$** (controlled by the drain bias). In other words, the potential distribution becomes two dimensional, and the gradual channel approximation (i.e.  **$E_x \gg E_y$** ) is no longer valid. This two dimensional potential results in the degradation of the threshold behaviour, dependence of threshold voltage on the channel length & biasing voltages and failure of the current saturation due to punch through effect.

In further sections, we will study various effects due to short channel length in MOSFET.

#### 8.2 Mobility Degradation

Mobility is important because the current in MOSFET depends upon mobility of charge carriers(holes and electrons).

We can describe this mobility degradation by two effects:

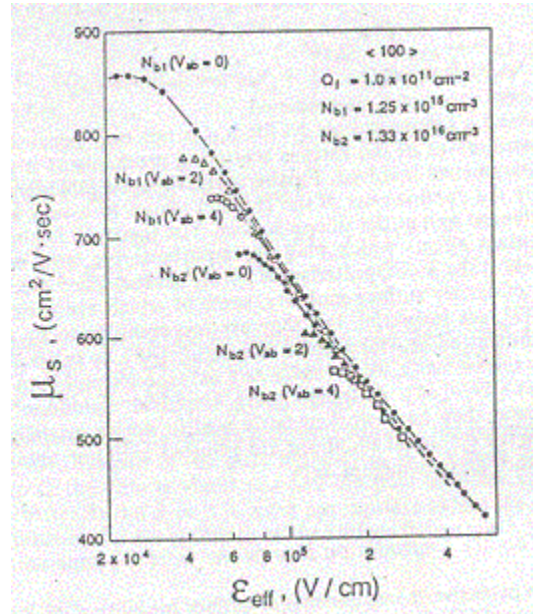


Figure 8.2: Mobility degradation graph

- i. **Lateral Field Effect:** In case of short channels, as the lateral field is increased, the channel mobility becomes field-dependent and eventually velocity saturation occurs (which was referred to in the previous lecture). This results in current saturation.
- ii. **Vertical Field Effect:** As the vertical electric field also increases on shrinking the channel lengths, it results in scattering of carriers near the surface. Hence the surface mobility reduces (Also explained by the mobility dependence equation given below).

$$\mu_s = \frac{\mu_{s0}}{1 + \left(\frac{E_{eff}}{E_{cr}}\right)^\alpha} \quad \text{where,}$$

$E_{eff}$  is the effective vertical electric field and

$E_{cr}$  is the critical electric field.

Thus for short channels, we can see (in the figure 8.2) the mobility degradation which occurs due to velocity saturation and scattering of carriers.

### 8.3 Subthreshold Current

An effect that is exacerbated by short channel designs is the subthreshold current which arises from the fact that some electrons are induced in the channel even before strong inversion is established. For the low electron concentration (typically of subthreshold regime), we expect diffusion current (proportional to carrier gradients) to dominate over drift currents (proportional to carrier concentrations). For very short channel lengths,

such carrier diffusion from source to drain can make it impossible to turn off the device below threshold. The subthreshold current is made worse by the DIBL effect (will be explained in later sections) which increases the injection of electrons from the source.

## 8.4 Threshold Voltage variation with Channel Length

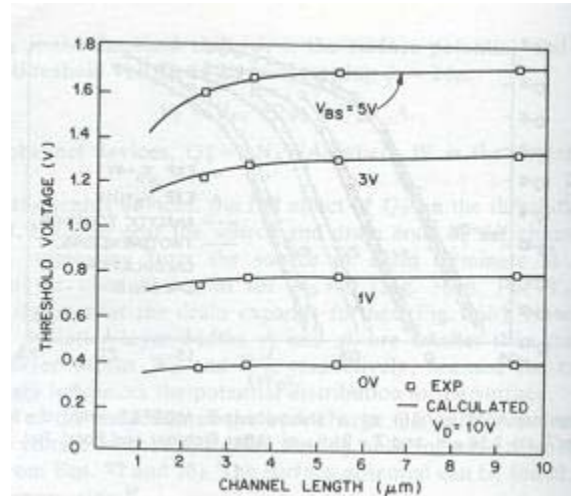


Figure 8.41: Dependence of  $V_T$  on  $L$  for MOSFET

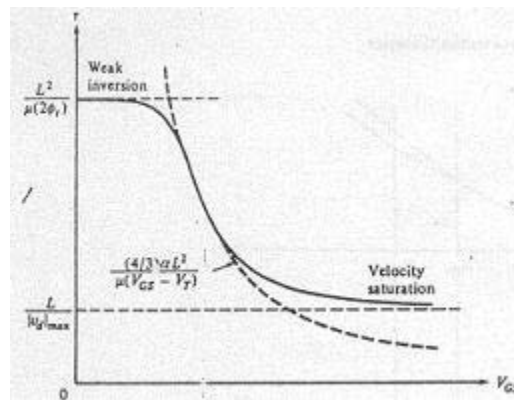


Figure 8.42:  $I_{DS}$  Vs  $V_{GS}$  for short channel

In case of long channel MOSFETs, gate has control over the channel and supports most of the charge. As we go to short channel lengths as seen in the graph above, the threshold voltage begins to decrease as the charge in the depletion region is now supported by the drain and the source also. Thus the gate needs to support less charge in this region and as a result,  $V_T$  falls down. This phenomenon is known as **charge sharing effect**.

Now since  $I_{DS}$  is proportional to  $(V_{GS} - V_T)$ , therefore as  $V_T$  begins to fall in case of short channels,  $I_{DS}$  starts increasing resulting in larger drain currents. Also when  $V_{GS}$  is zero and the MOSFET is in the cut off mode, since  $V_T$  is small,  $(V_{GS} - V_T)$  will be a small negative value and will result in leakage current which further multiplied by the drain voltage will result in leakage power. In case of long channel MOSFETs,  $V_T$  is large enough and  $(V_{GS} - V_T)$  is a comparatively larger negative value, in cut off mode leakage power is very small.

**Transit Time:** As seen in previous lecture, the short channel results in **velocity saturation** over part of the channel. So the argument used to derive the transit time for long channel MOSFET is no longer valid for short channel MOSFETs. We note that the transit time will be larger if electrons were moving at maximum speed all over the channel. Thus,

$$\text{transit time} > \frac{L}{|V_d|_{\max}}$$

Figure 8.42 shows that the transit time of a device operating in the 'flat' part of **IDS-VGS** characteristics curve which concludes that transit time cannot be decreased by increasing further **VGS**.

**Quantum Mechanical Increase Effect:** Another effect of quantum mechanics that also increases with scaling, is a shift in the surface potential required for strong inversion. This effect arises from so called "energy quantization" of confined particles which precludes electrons and holes from existing at zero energy in the conduction or valence bands. It is a direct consequence of the coupled **Poisson-Schrodinger equation** solution. This surface potential shift manifests itself as an increase in **|VT|** which for the long devices is given by –

$$|\Delta V_T| = |\Delta \psi_s| + \gamma(\sqrt{\phi_0 + \Delta \psi_s} - \sqrt{\phi_0})$$

Above equation tells that **|VT|** increases as devices are scaled down.

## 8.5 Drain Induced Barrier Lowering (DIBL)

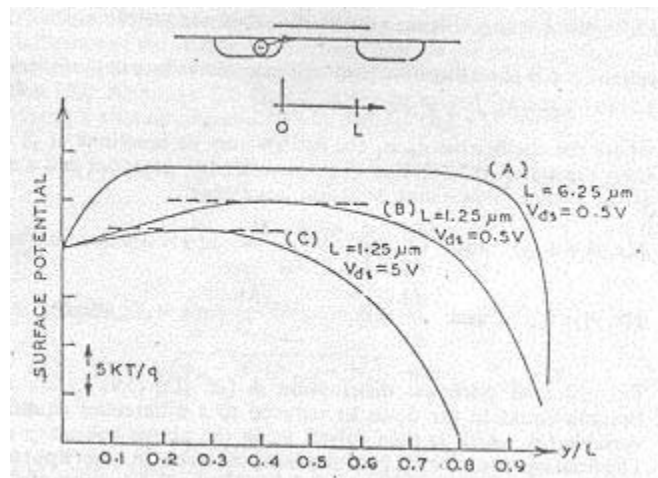


Figure 8.5: Surface potential graph with constant gate voltage ( $V_{DS}$  and  $L$  are varied)

The source and drain depletion regions can intrude into the channel even without bias, as these junctions are brought closer together in short channel devices. This effect is called charge sharing (as mentioned earlier) since the source and drain in effect take part of the channel charge, which would otherwise be controlled by the gate. As the

drain depletion region continues to increase with the bias, it can actually interact with the source to channel junction and hence lowers the potential barrier. This problem is known as **Drain Induced Barrier Lowering (DIBL)**. When the source junction barrier is reduced, electrons are easily injected into the channel and the gate voltage has no longer any control over the drain current.

In DIBL case,

$$X_{D(\text{source})} + X_{D(\text{drain})} < L$$

For figure 8.5, we can observe that under extreme conditions of encroaching source and drain depletion regions, the two curves can meet.

## 8.6 Drain Punch Through

When the drain is at high enough voltage with respect to the source, the depletion region around the drain may extend to the source, causing current to flow irrespective of gate voltage (i.e. even if gate voltage is zero). This is known as **Drain Punch Through** condition and the punch through voltage **VPT** given by:

$$V_{PT} = \frac{qN_a L^2}{2\epsilon_s}$$

So when channel length **L** decreases (i.e. short channel length case), **punch through voltage** rapidly decreases.

## 8.7 Hot Carrier Effect

Electric fields tend to be increased at smaller geometries, since device voltages are difficult to scale to arbitrarily small values. As a result, various hot carrier effects appear in short channel devices. The field in the reversed biased drain junction can lead to impact ionization and carrier multiplication. The resulting holes contribute to substrate current and some may move to the source, where they lower source barrier and result in electron injected from source into p-region. In fact n-p-n transistor can result within source channel drain configuration and prevent gate control of the current.

Another hot electron effect is the transport of the energetic electrons over (or tunneling through) the barrier into the oxide. Such electrons become trapped in the oxide, where they change the threshold voltage and I-V characteristics of the device. Hot electron effects can be reduced by reducing the doping in the source and drain regions, so that the junction fields are smaller. However lightly doped source and drain regions are incompatible with small geometry devices because of contact resistances and other similar problems. A compromise design of MOSFET, called **Lightly Doped Drain (LDD)**, using two doping levels with heavy doping over most of the source and drain areas with light doping in a region adjacent to the channel. The LDD structure decreases the field between drain and channel regions, thereby reduces injection into the oxide, impact ionization and other hot electron effects.

## 8.8 Surface States and Interface Trapped Charge

At Si-SiO<sub>2</sub> interface, the lattice of bulk silicon and all the properties associated with its periodicity terminate. As a result, localized states with energy in the forbidden energy gap of silicon are introduced at or very near to the Si-SiO<sub>2</sub> interface. Interface trapped charges are electrons or holes trapped in these states. The probability of occupation of a surface state by an electron or by a hole is determined by the surface state energy relative to the Fermi level. An electron in conduction band can contribute readily to electrical conduction current while an interface trapped electron does not, except hopping among the surface states. Thus by trapping electrons and holes, surface states can reduce conduction current in MOSFETs.

Surface states can also act as localized generation-recombination centers and lead to leakage currents.

## 8.9 Conclusion

Because short channel effects complicate device operation and degrade device performance, these effects should be eliminated or minimized, so that a physical short channel device can preserve the electrical long channel behaviour.

## Recap

In this lecture you have learnt the following

- Motivation
- Mobility degradation
- Subthreshold current
- Threshold voltage variation
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**Congratulations, you have finished Lecture 8.**