Module 6 : Semiconductor Memories
Lecture 32 : Few special Examples of Memories

Objectives

In this lecture you will learn the following

- Non-Volatile READ-WRITE Memory
- The Floating Gate Transistor
- Erasable Programmable Read Only Memory (EPROM)
- Electrically Erasable Programmable Read Only Memory (E2PROM)

32.1 Non-Volatile Read-Write Memory

The architecture of Non-Volatile Read-Write (NVRW) Memory is virtually identical to the ROM structure. The memory core consists of an array of transistors placed on the wordline/bitline grid. Selectively disabling or enabling some of the devices programs the memory. In a ROM, this is accomplished by mask-level alterations. In a NVRW memory, a modified transistor that permits its threshold to be altered electrically is used. This modified threshold is retained indefinitely (or atleast for the lifetime, typically of the order of 10 yrs) even when the supply is turned off. To reprogram the memory, the programmed values must be erased, after which a new programming round must be started. The method of erasing is the main differentiating factor between the various classes of reprogrammable nonvolatile memories. The programming of the memory is typically an order of magnitude slower than the reading operation.

32.2 Floating Gate Transistor

Over the years, various attempts have been made to create a device with electrically alterable characteristics and enough reliability to support a multitude of write cycles. For example, the MNOS (**M**etal **N**itride **O**xide **S**emiconductor) transistor held promise, but has been unsuccessful until now. In this device, threshold-modifying electrons are trapped in a $\mathbf{Si_3N_4}$ layer deposited on the top of the gate $\mathbf{SiO_2}$. A more accepted solution is offered by the floating gate transistor shown in Figure 32.21, which forms the core of virtually every NVRW memory built today.

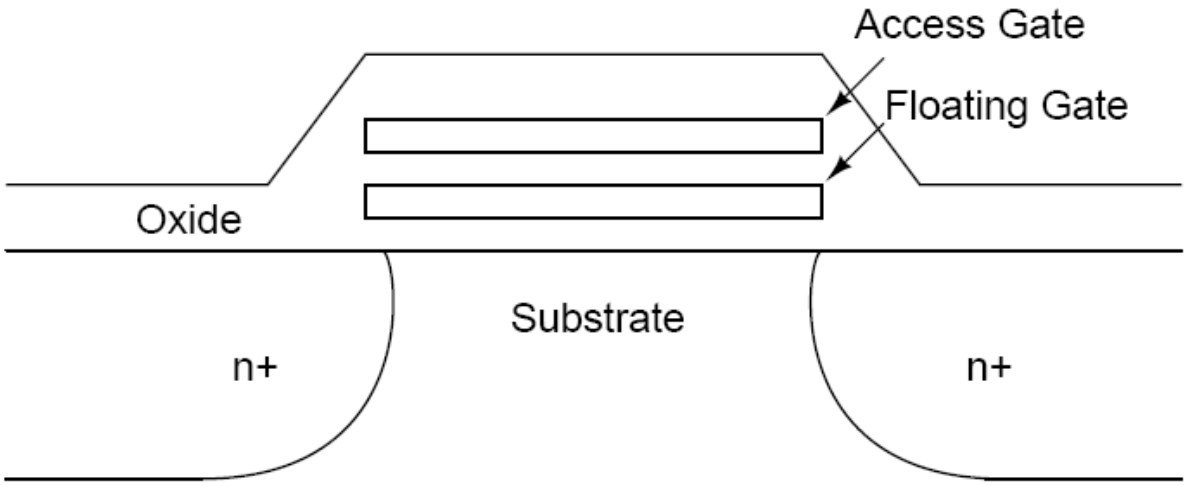

Fig 32.21: FAMOS Structure

The structure is similar to traditional MOS device, except that an extra polysilicon strip is inserted between the gate and channel. This strip is not connected to anything and is called as **Floating gate**. The most obvious impact of inserting this extra gate is to double the gate oxide thickness $\mathbf{t_{ox}}$, which results in a reduced device transconductance as well as increased threshold voltage. Both these properties are not particularly desirable.

This device has property that its threshold voltage is programmable. Applying a high voltage (about 10V) between the source and drain terminals creates a high electric field and causes **avalanche injection** to occur. Electrons acquire sufficient energy to become **'HOT'** and traverse through the first oxide insulator, so that they get trapped on the floating gate. This phenomenon can occur with oxide as thick as 100nm, which makes it relatively easy to fabricate the device. In reference to the programming mechanism, the floating gate transistor is often called Floating Gate Avalanche Injection MOS (FAMOS).

The trapping of electrons on the floating gate effectively drops the voltage on that gate. This process is self-limiting and the negative charge accumulated on the floating gate reduces the electrical field over the oxide so that ultimately it becomes incapable of accelerating more hot electrons. Removing the voltage leaves the induced negative charge in place, and results in a negative voltage on the intermediate gate. From the device point of view, this translates into an effective increase in threshold voltage. To turn on the device, a higher voltage is needed to overcome the effect of the induced negative charge. Typically, the resulting threshold voltage is around 7V; thus a 5V gate-to-source voltage is not sufficient to turn on the transistor, and the device is effectively disabled.
Since the floating gate is surrounded by $\mathbf{SiO_2}$, which is an excellent insulator, the trapped charge can be stored for many years, even when the supply voltage is removed, creating the nonvolatile storage mechanism. One of the major concerns of the floating gate approach is the need for high programming voltages. By tailoring the impurity profiles, technologists have been able to reduce the required voltage from the original 25V to approximately 12.5V in today's memories.

32.3 Erasable Programmable Read Only Memory (EPROM)

An EPROM is erased by shining ultraviolet light on the cells through a transparent window in the package. The UV radiation renders the oxide slightly conductive by direct generation of electron-hole pair in the material. The erasure process is slow and can take from seconds to several minutes, depending on the intensity of the UV source. Programming takes several (5-10) microseconds/word. Another problem with the process is limited endurance, that is, the number of erase/program cycles is generally limited to maximum of 1000, mainly as a result of UV erase procedure. Reliability is also an issue. The device threshold might vary with repeated programming cycles. Most EPROM memories therefore contain on-chip circuitry to control the value of thresholds to within a specified range during programming. Finally, the injection always entails a large channel current, as high as 0.5mA at a control gate voltage of 12.5V. This causes high power dissipation during programming. The EPROM cell is extremely simple and dense, making it possible to fabricate large memories at a low cost. EPROMs were therefore attractive in applications that do not require regular programming. Due to cost and reliability issues, EPROMs have fallen out of favor and have been replaced by Flash Memories.

32.4 Electrically Erasable Programmable Read Only Memory (EEPROM)

The major disadvantage of the EPROM approach is that erasure procedure has to occur **"off system"**. This means the memory must be removed from the board and placed in the EPROM programmer for programming. The EEPROM approach avoids this labor intensive and annoying procedure by using another mechanism to inject or remove charges from the floating gate viz. tunneling. A modified floating gate device called the FLOTOX (Floating Gate Tunnel Oxide) transistor is used as a programmable device that supports an electrical erasure procedure. A cross section of the FLOTOX structure is shown in Figure 32.41.

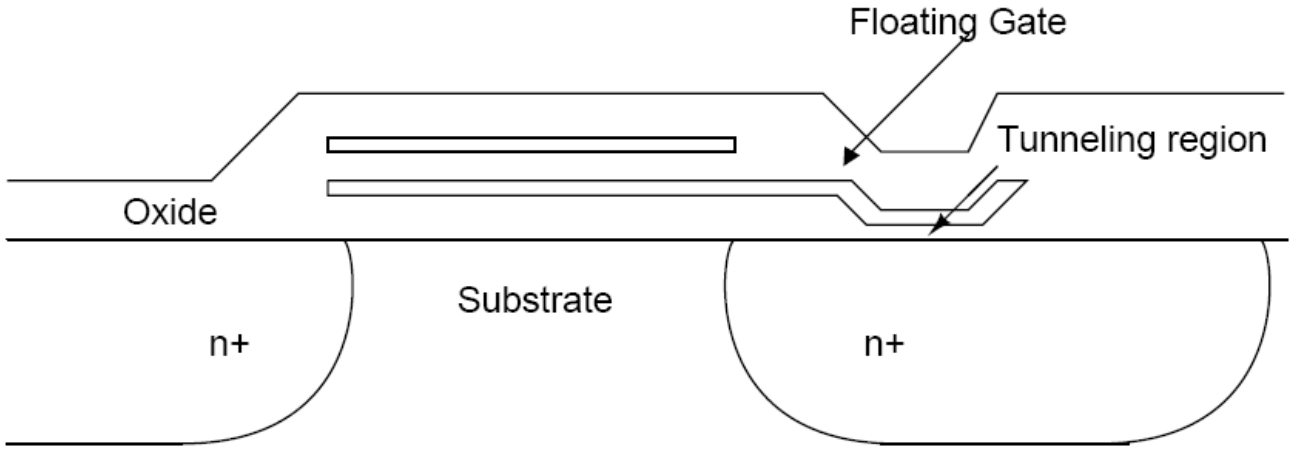

Fig 32.41: FLOTOX Structure

It resembles the FAMOS device, except that a portion of the dielectric separating the floating gate from the channel and drain is reduced in thickness to about 10nm or less.

When a voltage of approximately 10V is applied over the thin insulator, electrons can move to and from the floating gate through tunneling.

The main advantage of this programming approach is that it is reversible; that is, erasing is simply achieved by reversing the voltage applied during the writing process. Injecting electrons onto the floating gate raises the threshold, while the reverse operation lowers it. This bidirectionality, however, introduces a threshold control problem: removing too much charge from the floating gate results in a depletion device that cannot be turned off by the standard wordline signals. Notice that the resulting threshold voltage depends on initial charge on the gate, as well as the applied programming voltages. It is a strong function of the oxide thickness, which is subject to non-neglible variations over the die. To remedy this problem, an extra transistor connected in series with the floating gate transistor is added to the EEPROM cell. This transistor acts as the access device during the read operation, while the FLOTOX transistor performs the storage function. This is in contrast to the EPROM cell, where the FAMOS transistor acts as both the programming and access device.

The EEPROM cell with its two transistors is larger than its EPROM counterpart. This area penalty is further aggravated by the fact that the FLOTOX device is intrinsically larger than the FAMOS transistor due to the extra area of the tunneling oxide. Additionally, fabrication of very thin oxide is a challenging and costly manufacturing step. Thus EEPROM components pack less bits for more cost than EPROMs. On the positive side EEPROM offer high versatility. They also tend to last longer, as they can support upto 100,000 erase/write cycles. Repeated programming causes a drift in the threshold voltage due to permanently trapped charges in the **SiO_2**.This finally leads to malfunction or the inability to reprogram the device.

Recap

In this lecture you have learnt the following

- Non-Volatile READ-WRITE Memory
- The Floating Gate Transistor
- Erasable Programmable Read Only Memory (EPROM)
- Electrically Erasable Programmable Read Only Memory (E2PROM)

Congratulations, you have finished Lecture 32.