

# Module 3 : Fabrication Process and Layout Design Rules

## Lecture 13 : Layout Design Rules

### Objectives

In this course you will learn the following

- Motivation
- Types of Design Rules
- Layer Representations
- Stick Diagrams

### 13.1 Motivation

In VLSI design, as processes become more and more complex, need for the designer to understand the intricacies of the fabrication process and interpret the relations between the different photo masks is really trouble some. Therefore, a set of layout rules, also called **design rules**, has been defined. They act as an interface or communication link between the circuit designer and the process engineer during the manufacturing phase. The objective associated with layout rules is to obtain a circuit with optimum yield (functional circuits versus non-functional circuits) in as small as area possible without compromising reliability of the circuit. In addition, Design rules can be conservative or aggressive, depending on whether yield or performance is desired. Generally, they are a compromise between the two. Manufacturing processes have their inherent limitations in accuracy. So the need of design rules arises due to manufacturing problems like –

- Photo resist shrinkage, tearing.
- Variations in material deposition, temperature and oxide thickness.
- Impurities.
- Variations across a wafer.

These lead to various problems like :

- **Transistor problems:**  
Variations in threshold voltage: This may occur due to variations in oxide thickness, ion-implantation and poly layer.  
Changes in source/drain diffusion overlap.  
Variations in substrate.
- **Wiring problems:**  
Diffusion: There is variation in doping which results in variations in resistance, capacitance.  
Poly, metal: Variations in height, width resulting in variations in resistance, capacitance.  
Shorts and opens.
- **Oxide problems:**  
Variations in height.  
Lack of planarity.

- **Via problems:**

- Via may not be cut all the way through.
  - Undersize via has too much resistance.
  - Via may be too large and create short.

To reduce these problems, the design rules specify to the designer certain geometric constraints on the layout artwork so that the patterns on the processed wafers will preserve the topology and geometry of the designs. This consists of minimum-width and minimum-spacing constraints and requirements between objects on the same or different layers. Apart from following a definite set of rules, design rules also come by experience.

## 13.2 Types of Design Rules

The design rules primary address two issues:

1. The geometrical reproduction of features that can be reproduced by the maskmaking and lithographical process ,and
2. The interaction between different layers.

There are primarily two approaches in describing the design rules.

1. Linear scaling is possible only over a limited range of dimensions.
2. Scalable design rules are conservative .This results in over dimensioned and less dense design.
3. This rule is not used in real life.

### 1. Scalable Design Rules (e.g. SCMOS, $\lambda$ -based design rules):

In this approach, all rules are defined in terms of a single parameter  $\lambda$ . The rules are so chosen that a design can be easily ported over a cross section of industrial process ,making the layout portable .Scaling can be easily done by simply changing the value of.

The key disadvantages of this approach are:

### 2. Absolute Design Rules (e.g. $\mu$ -based design rules ) :

In this approach, the design rules are expressed in absolute dimensions (e.g.  $0.75\mu\text{m}$ ) and therefore can exploit the features of a given process to a maximum degree. Here, scaling and porting is more demanding, and has to be performed either manually or using CAD tools .Also, these rules tend to be more complex especially for deep submicron.

The fundamental unity in the definition of a set of design rules is the minimum line width .It stands for the minimum mask dimension that can be safely transferred to the semiconductor material .Even for the same minimum dimension, design rules tend to differ from company to company, and from process to process. Now, CAD tools allow designs to migrate between compatible processes.



















### 13.3 Layer Representations

With increase of complexity in the CMOS processes, the visualization of all the mask levels that are used in the actual fabrication process becomes inhibited. The layer concept translates these masks to a set of conceptual layout levels that are easier to visualize by the circuit designer. From the designer's viewpoint, all CMOS designs have the following entities:

- Two different substrates and/or wells: which are p-type for NMOS and n-type for PMOS.
- Diffusion regions (p+ and n+): which defines the area where transistors can be formed. These regions are also called **active areas**. Diffusion of an inverse type is needed to implement contacts to the well or to substrate. These are called **select regions**.
- Transistor gate electrodes : Polysilicon layer
- Metal interconnect layers
- Interlayer contacts and via layers.

The layers for typical CMOS processes are represented in various figures in terms of:

- A color scheme (Mead-Conway colors).
- Other color schemes designed to differentiate CMOS structures.
- Varying stipple patterns
- Varying line styles

Layer Description	Representation				
metal	 m1	 m2	 m3	 m4	 m5
well	 nw				
polysilicon	 poly				
contacts & vias	 ct	 v12,v23,v34,v45	 nwc	 pwc	
active area and FETs	 ndif	 pdif	 nfct	 pfct	
select	 nplus	 pplus	 prb		

13.31 Mead Conway Color coding for layers.

An example of layer representations for CMOS inverter using above design rules is shown below-

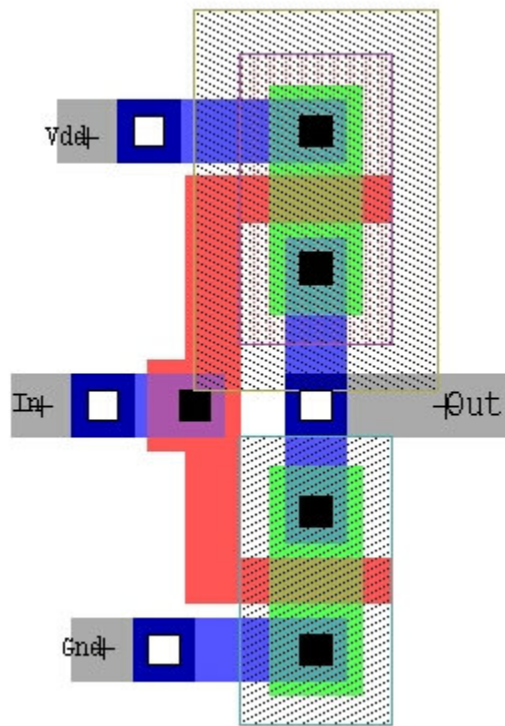


Figure 13.32 :CMOS Inverter Layout Figure

### 13.4 Stick Diagrams

Another popular method of symbolic design is "**Sticks**" layout. In this, the designer draws a freehand sketch of a layout, using colored lines to represent the various process layers such as diffusion, metal and polysilicon. Where polysilicon crosses diffusion, transistors are created and where metal wires join diffusion or polysilicon, contacts are formed.

This notation indicates only the relative positioning of the various design components. The absolute coordinates of these elements are determined automatically by the editor using a compactor. The compactor translates the design rules into a set of constraints on the component positions, and solve a constrained optimization problem that attempts to minimize the area or cost function.

The advantage of this symbolic approach is that the designer does not have to worry about design rules, because the compactor ensures that the final layout is physically correct. The disadvantage of the symbolic approach is that the outcome of the compaction phase is often unpredictable. The resulting layout can be less dense than what is obtained with the manual approach. In addition, it does not show exact placement, transistor sizes, wire lengths, wire widths, tub boundaries.

For example, stick diagram for CMOS Inverter is shown below.

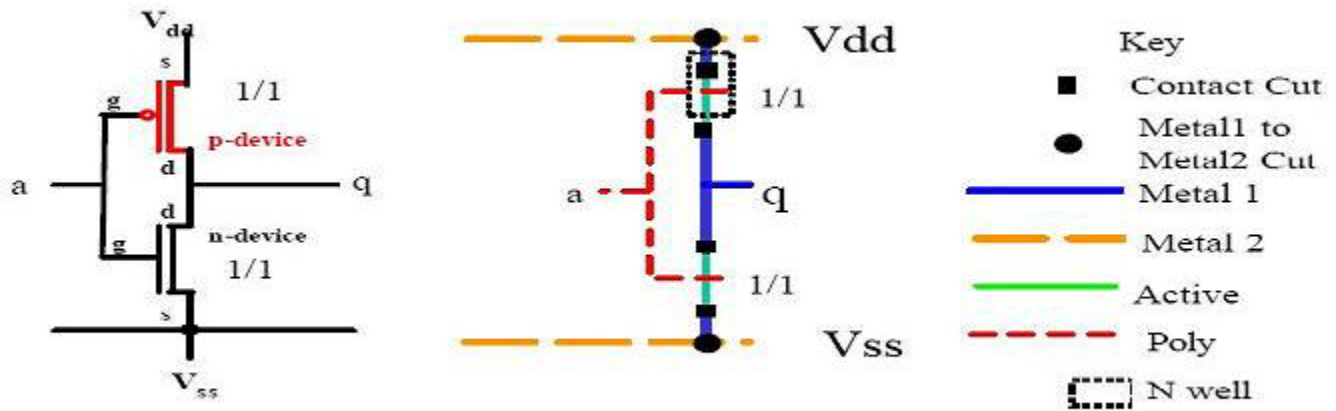


Figure 13.41: Stick Diagram of a CMOS Inverter

## Recap

In this lecture you have learnt the following

- Motivation
- Types of Design Rules
- Layer Representations
- Stick Diagrams

**Congratulations, you have finished Lecture 13.**