Module 2 : MOSFET
Lecture 4 : MOS Capacitor

Objectives

In this course you will learn the following

- MOS as Capacitor
- Modes of operation
- Capacitance calculation of MOS capacitor

4.1 MOS as Capacitor

Refering to fig. 4.1, we can see there is an oxide layer below the Gate terminal. Since oxide is a very good insulator, it contributes to an oxide capacitance in the circuit.

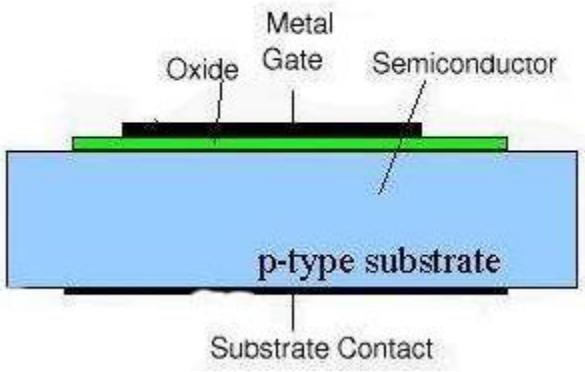


Fig 4.1: Cross-section view of MOS Capacitor

Normally, the capacitance value of a capacitor doesn't change with values of voltage applied across its terminals. However, this is not the case with MOS capacitor. We find that the capacitance of MOS capacitor changes its value with the variation in Gate voltage. This is because application of gate voltage results in band bending in silicon substrate and hence variation in charge concentration at **Si-SiO2** interface.

4.2 Modes of operation

Depending upon the value of gate voltage applied, the MOS capacitor works in three modes :

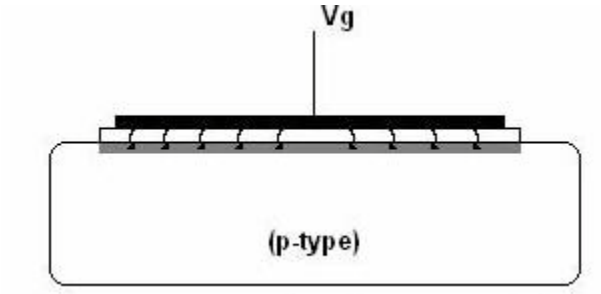


Fig 4.2a: Accumulation mode (grey layer - strong hole concentration)

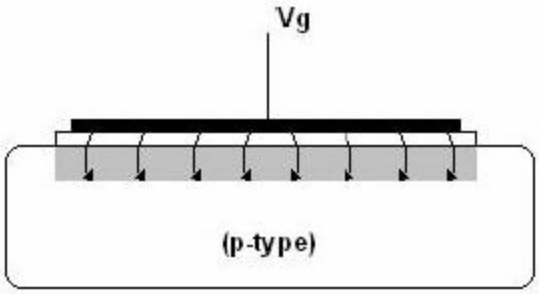


Fig 4.2b: Depletion Mode (light grey layer – depletion region)

1. **Accumulation:** In this mode, there is accumulation of holes (assuming n-MOSFET) at the Si-SiO2 interface. All the field lines emanating from the gate terminate on this layer giving an effective dielectric thickness as the oxide thickness (shown in Fig. 4.2a). In this mode, Vg <0

2. **Depletion:** As we move from negative to positive gate voltages the holes at the interface are repelled and pushed back into the bulk leaving a depleted layer. This layer counters the positive charge on the gate and keeps increasing till the gate voltage is below threshold voltage. As shown in Fig. 4.2b we see a larger effective dielectric length and hence a lower capacitance.

3. **Strong Inversion:**When Vg crosses threshold voltage, the increase in depletion region width stops and charge on layer is countered by mobile electrons at Si-SiO2 interface. This is called inversion because the mobile charges are opposite to the type of charges found in substrate. In this case the inversion layer is formed by the electrons. Field lines hence terminate on this layer thereby reducing the effective dielectric thickness as shown in Fig. 4.2c)

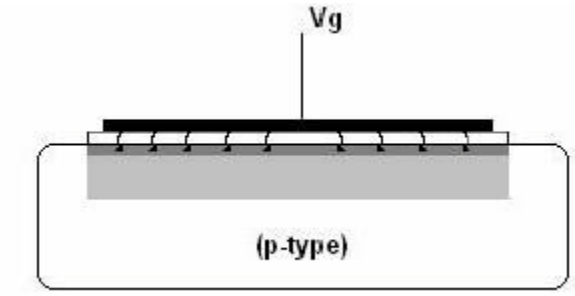
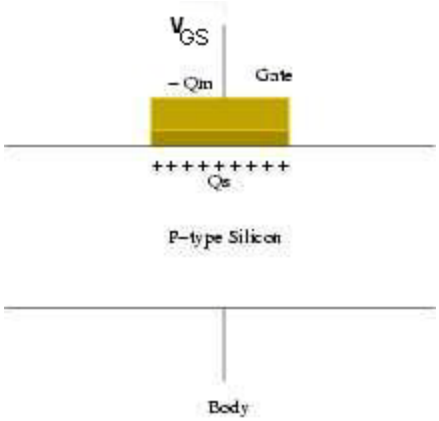


Fig 4.2c: Strong Inversion mode
(grey layer - strongelectron concentration, light grey - depletion region)

4.3 Capacitace calculation of MOS Capacitor

In the last chapter, we gave you an introduction of MOS as capacitor. In this chapter, we will see how MOS works as a capacitor with derivation of some related equations.



By Gauss's Law: $\sum Q = 0$

$\Rightarrow Q_s = -Q_m$

Also by thermal equilibrium:

$p.n = n_i^2$

where **p** and **n** are hole and electron concentrations of substrate and is hole or electron concentration of the corresponding intrinsic seminconductor.

We see that if we keep making more and more -ve, the charges **Qs** and **Qm** keep increasing. Thus, it is acting like a good parallel plate capacitor. Its capacitance can be given as-

$$C = C_{ox} = \frac{\in_{ox}}{t_{ox}}$$

Fig 4.3: Gate and Depeletion charge of MOS Capacitor

For +ve bias voltage on gate, increasing V_{GS} will increase **Qm** and **Qs.**

Using the depletion approximation, we can write depletion width x_d as a function of φ_s as

$$x_d = \sqrt{\frac{2 \in_s \varphi_s}{qN_a}}$$

where N_a is the substrate acceptor density, $\in_s$ is dielectric constant of substrate and φ_s is the surface potential at substrate.

The depletion region grows with increased voltage across the capacitor until strong inversion is reached. After that, further increase in the voltage results in inversion rather than more depletion. Thus the maximum depletion width is:

$$x_{dmax} = \sqrt{\frac{2 \in_s (2\varphi_F)}{qN_a}}$$

Also,

$$Q_D = -qN_a x_d$$

Therefore at

$$x_d = x_{dmax}, \; Q_D = -qN_a x_{dmax} \text{ (const.)}$$

But by Gauss's law, electrons must compensate for increasing **Qs**.
So,

$$Q_s = -(Q_i + Q_D)$$

where charge **Qi** is due to electrons in the inversion layer.

Earlier due to low electric field, the electron-hole pairs formed below the oxide interface recombine. However, once the electric field increases, the electron-hole pairs formed are not able to recombine. So the free electron concentration increases.

By Kirchoff's law, V_{GS} is given by: $V_{GS} = \varphi_s + V_{ox}$

We assume here that $Q_{ox} = 0$ and $\varphi_m = \varphi_s$.

Since, $Q_{ox} = 0$, we have: $\in_{ox} E_{ox} = \in_S E_s$

$$\Rightarrow E_s = \frac{\in_{ox} V_{ox}}{\in_s t_{ox}} = \frac{C_{ox}}{\in_s} V_{ox}$$

$$Q_s = -\in_s E_s = -C_{ox} V_{ox}$$

$$\Rightarrow V_{ox} = -\frac{Q_s}{C_{ox}}$$

Thus we have, $V_{GS} = \varphi_s - \frac{Q_s}{C_{ox}}$

$$\Rightarrow C_{ox} = \frac{Q_s}{\varphi_s - V_{GS}}$$

Recap

In this lecture you have learnt the following

- MOS as Capacitor
- Modes of operation
- Capacitance calculation of MOS capacitor

Congratulations, you have finished Lecture 4.