Module 4 : Propagation Delays in MOS
Lecture 16 : Propagation Delay Calculation of CMOS Inverter

Objectives

In this lecture you will learn the following

- Few Definitions
- Quick Estimates
- Rise and Fall times Calculation

16.1 Few Definitions

Before calculating the propagation delay of CMOS Inverter, we will define some basic terms-

- **Switching speed -** limited by time taken to charge and discharge, **C**L.
- **Rise time, tr:** waveform to rise from 10% to 90% of its steady state value
- **Fall time tf:** 90% to 10% of steady state value
- **Delay time, t*d*:** time difference between input transition (50%) and 50% output level

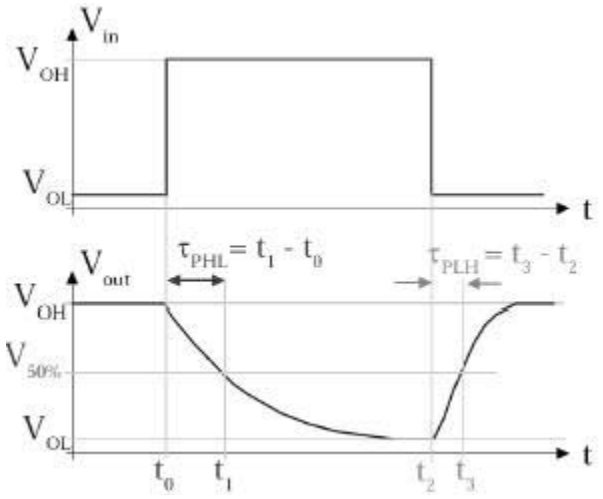

Fig 16.1: Propagation delay graph

The propagation delay **tp** of a gate defines how quickly it responds to a change at its inputs, it expresses the delay experienced by a signal when passing through a gate. It is measured between the 50% transition points of the input and output waveforms as shown in the figure 16.1 for an inverting gate. The τ_{pHL} defines the response time of the gate for a low to high output transition, while τ_{pHL} refers to a high to low transition. The propagation delay τ_p as the average of the two

$$\tau_p = (\tau_{pLH} + \tau_{pHL})/2$$

16.2 Quick Estimates:

We will give an example of how to calculate quick estimate. From fig 16.22, we can write following equations.

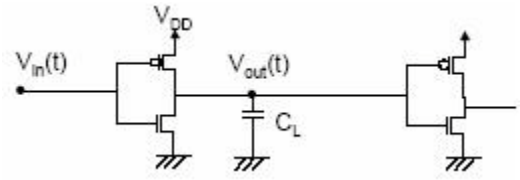

Fig 16.21: Example CMOS Inverter Circuit

$$V_{50\%} = V_{OL} + \frac{V_{OH} - V_{OL}}{2} = \frac{V_{OH} + V_{OL}}{2}$$
$$V_{90\%} = V_{OL} + 0.9(V_{OH} - V_{OL})$$
$$V_{10\%} = V_{OL} + 0.1(V_{OH} - V_{OL})$$

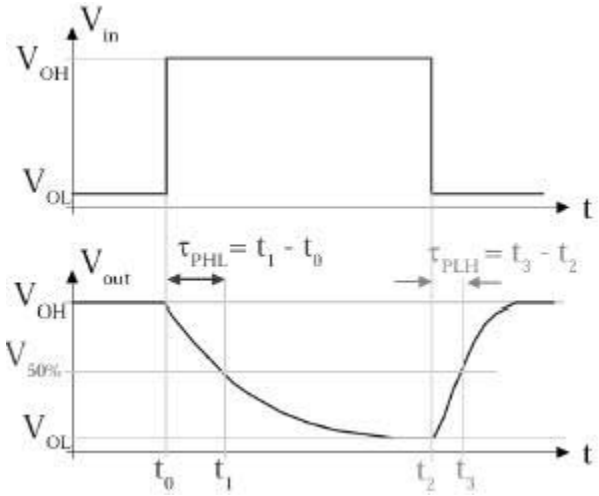

Fig. 16.22 : Propagation Delay of above MOS circuit

From figure 16.21, when Vin = 0 the capacitor CL charges through the PMOS, and when Vin = 5 the capacitor discharges through the N-MOS. The capacitor current is –

$$C_L \frac{dV}{dt} = i_{dsn} = |i_{dsp}|$$

From this the delay times can be derived as

$$\int dt = \int \frac{C_L}{i_{ds}} dV$$

The expressions for the propagation delays as denoted in the figure (16.22) can be easily seen to be

$$\tau_{PHL} = \frac{C_{Load}\Delta V_{HL}}{I_{avg,HL}} = \frac{C_{Load}(V_{OH} - V_{50\%})}{I_{avg,HL}} \quad \& \quad \tau_{PLH} = \frac{C_{Load}\Delta V_{LH}}{I_{avg,LH}} = \frac{C_{Load}(V_{50\%} - V_{OL})}{I_{avg,HL}}$$

where $I_{avg,HL}$ & $I_{avg,LH}$ are defined as -

$$I_{avg,HL} = \frac{1}{2}[i_C(V_{in} = V_{OH}, V_{out} = V_{OH}) + i_C(V_{in} = V_{OH}, V_{out} = V_{50\%})]$$

$$I_{avg,LH} = \frac{1}{2}[i_C(V_{in} = V_{OL}, V_{out} = V_{OL}) + i_C(V_{in} = V_{OL}, V_{out} = V_{50\%})]$$

16.3 Rise and Fall Times

Figure 16.21 shows the familiar CMOS inverter with a capacity load **CL** that represents the load capacitance (input of next gates, output of this gate and routing). Of interest is the voltage waveform **Vout(t)** when the input is driven by a step waveform, **Vin(t)** as shown in figure 16.22.

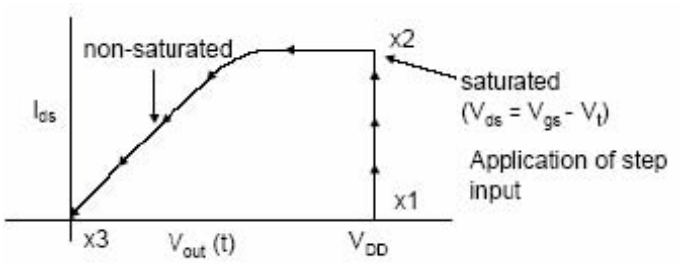

Fig 16.31: trjectory of n-transistor operating point

Figure 16.31 shows the trajectory of the n-transistor operating point as the input voltage, **Vin(t)**, changes from **0V** to **VDD**. Initially, the end-device is cutt-off and the load capacitor is charged to **VDD**. This illustrated by **X1** on the characteristic curve. Application of a step voltage (**VGS = VDD**) at the input of the inverter changes the operating point to **X2**. From there onwards the trajectory moves on the **VGS= VDD** characteristic curve towards point **X3** at the origin.

Thus it is evident that the fall time consists of two intervals:

1. **t**f1=period during which the capacitor voltage, **Vout**, drops from **0.9VDD** to (**VDD**−**Vtn**)
2. **t**f2=period during which the capacitor voltage, **Vout**, drops from **(VDD−Vtn)** to **0.1VDD.**

The equivalent circuits that illustrate the above behavior are show in figure (16.32 & 16.33).

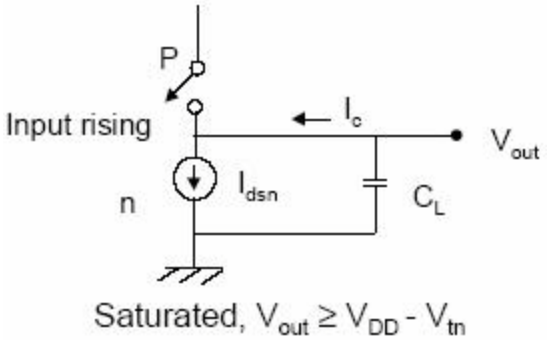

Figure 16.32: Equivalent circuit for showing behav. of **t**f1

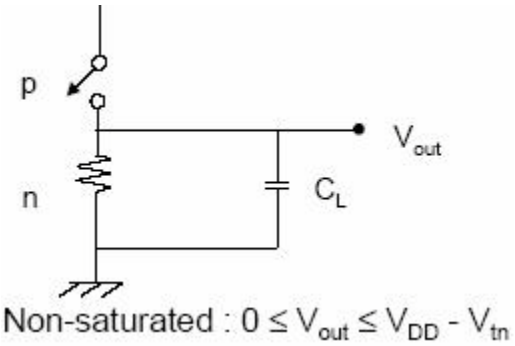

Figure 16.33: Equivalent circuit for showing behav. of **t**f2

As we saw in last section, the delay periods can be derived using the general equation

$$\int dt = \int \frac{C_L}{i_{ds}} dV$$

from figure (16.32) while in saturation,

$$I_{dsn(sat)} = \frac{\beta_n}{2}(V_{in} - V_{tn})^2$$

Integrating from t **=** t**1**, corresponding to **Vout=0.9 VDD**, to t **=** t**2** corresponding to **V**out**=(*V*DD-*V*tn) results in,**

$$t_{f1} = \frac{2C_L}{\beta_n (V_{DD} - V_{tn})^2} \int_{V_{DD}-V_{tn}}^{0.9V_{DD}} dV_{out}$$
$$= \frac{2C_L (V_{DD} - 0.1V_{tn})}{\beta_n (V_{DD} - V_{tn})^2}$$

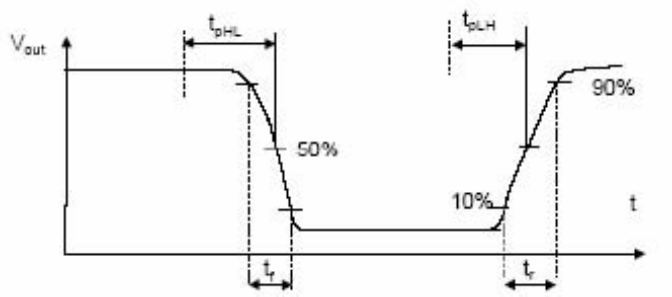

Fig 16.34: Rise and Fall time graph

When the n-device begins to operate in the linear region, the discharge current is no longer constant. The time **tf1** taken to discharge the capacitor voltage from **(*V*DD-*V*tn)** to ***0.1V*DD** can be obtained as before. In linear region,

$$I_{dsn(\text{linear})} = -\beta_n[(V_{DD} - V_{tn})V_{out} - V_{out}^2/2]$$

$$t_{f2} = \frac{C_L}{\beta_n(V_{DD} - V_{tn})^2}\int_{V_{DD}-V_{tn}}^{0.1V_{DD}} \frac{dV_{out}}{\frac{V_{out}^2}{2(V_{DD} - V_{tn})} - V_{out}} = \frac{C_L}{\beta_n(V_{DD} - V_{tn})}\ln\left(\frac{19V_{DD} - 20V_{tn}}{V_{DD}}\right)$$

$$= \frac{C_L}{\beta_n V_{DD}(1 - n)}\ln(19 - 20n) \qquad \text{where } n = \frac{V_{tn}}{V_{DD}}$$

Thus the complete term for the fall time is,

$$t_f = t_{f1} + t_{f2} = \frac{2C_L}{\beta_n V_{DD}(1 - n)}\left[\frac{(n - 0.1)}{(1 - n)} + \frac{1}{2}\ln(19 - 20n)\right]$$

The fall time tf can be approximated as,

$$t_f \approx k_n \frac{C_L}{\beta_n V_{DD}} \qquad k_n = 3 \sim 4 \text{ for } V_{DD} = 3 \sim 5V \text{ and } V_{tn} = 0.5 \sim 1V$$

From this expression we can see that the delay is directly proportional to the load capacitance. Thus to achieve high speed circuits one has to minimize the load capacitance seen by a gate. Secondly it is inversely proportion to the supply voltage i.e. as the supply voltage is raised the delay time is reduced. Finally, the delay is proportional to the **βn** of the driving transistor so increasing the width of a transistor decreases the delay.

Due to the symmetry of the CMOS circuit the rise time can be similarly obtained as; For equally sized **n** and **p** transistors (where **βn=2βp**) **tf**=t**r**

Thus the fall time is faster than the rise time primarily due to different carrier mobilites associated with the p and n devices thus if we want t**f**=t**r** we need to make **βn**/**βp** =**1**. This implies that the channel width for the **p**-device must be increased to approximately 2 to 3 times that of the **n**-device.

The propagation delays if calculated as indicated before turn out to be,

$$\tau_{PLH} = \frac{C_L}{k_P(V_{DD} - |V_{T0p}|)}\left[\frac{2|V_{T0p}|}{(V_{DD} - |V_{T0p}|)} + \ln\left(\frac{4((V_{DD} - |V_{T0p}|))}{V_{DD}} - 1\right)\right]$$

$$\tau_{PHL} = \frac{C_L}{k_n(V_{DD} - V_{T0n})}\left[\frac{2V_{T0n}}{(V_{DD} - V_{T0n})} + \ln\left(\frac{4((V_{DD} - V_{T0n}))}{V_{DD}} - 1\right)\right]$$

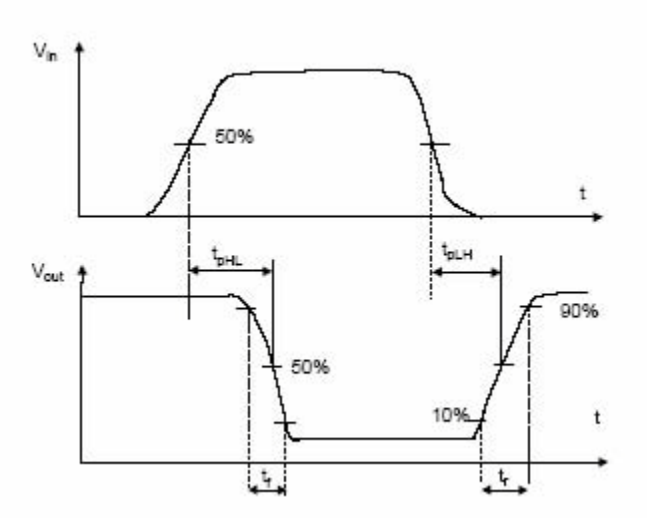

Figure 16.35: Rise and Fall time graph of Output w.r.t Input

If we consider the rise time and fall time of the input signal as well, as shown in the fig 16.35 we have,

$$\tau_{PLH(\text{actual})} = \sqrt{(\tau_{PLH})^2 + (t_f/2)^2}$$
$$\tau_{PHL(\text{actual})} = \sqrt{(\tau_{PHL})^2 + (t_r/2)^2}$$

These are the rms values for the propagation delays.

Recap

In this lecture you have learnt the following

- Few Definitions
- Quick Estimates
- Rise and Fall times Calculation

Congratulations, you have finished Lecture 16.