Module 1 : Introduction to VLSI Design
Lecture 2 : System approach to VLSI Design

Objectives

In this lecture you will learn the following:

- What is System?
- Design Abstraction Levels
- Delay and Interconnect Issues in physical circuits

2.1 What is System?

2.1.1 Definition of System

A system is something which gives an output when it is provided with an input (see figure 1).

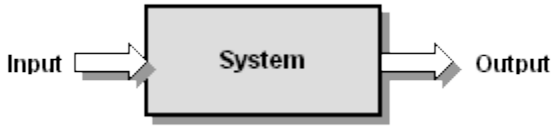

Figure 1. A simple System

2.1.2 System-On-Chip (SoC)

As the name suggests, its basically means shrinking the whole system onto a single chip.The most important feature of the chip is that its functionality should be comparable to that of the original system. It improves quality, productivity and performance.

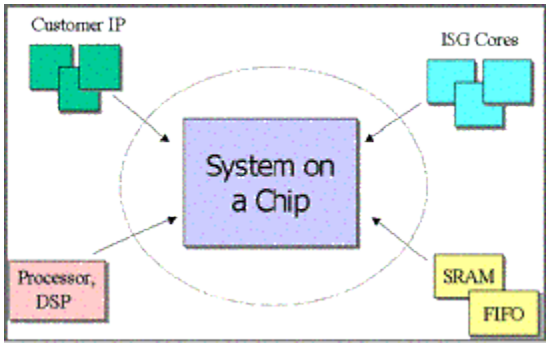

Figure 2. An SoC example

2.2 Design Abstraction levels

Every system should be decomposed into *three* fundamental domains:

1. Behavioral Domain
2. Structural Domain
3. Physical Domain

In every domain, there are diffirent layers or levels of hierarchy. The following Onion Diagram will give a better understanding of this -

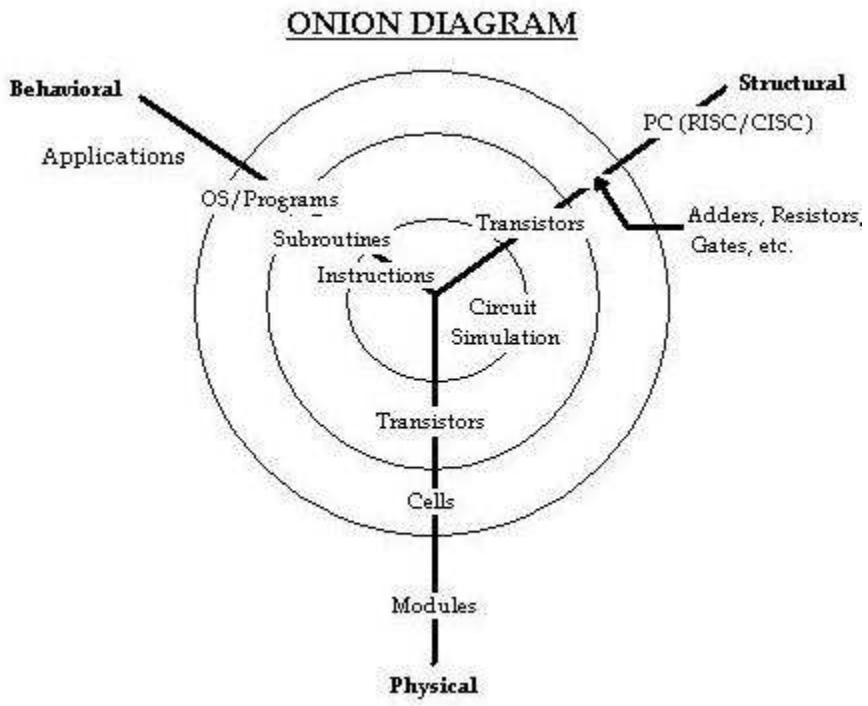

Figure 3. Onion Diagram

We can design the system at various layers, which are called design abstraction levels:

1. Architechture
2. Algorithm
3. Modules (or Functions)
4. Logic
5. Switch
6. Circuit
7. Device

In this course, we are only dealing with Logic, Switch and Circuit levels.

Representation examples

Behavioral Representation

```
If(d > 0) d = d + a
else    d = d + b
```

Structural Representation

```
module add(c0, s, a, b, c);
  input a, b, c;
  output s, c0;
  sum s1 (s, a, b, c);
  carry c1 (c0, a, b, c)
end module
```

2.3 Delay and Interconnect Issues in physical circuits

It must be noted that when the adder described (in the above structural Representation) is realized physically, the output may not arrive at the instant the input is given i.e. if the input is given at time t=0, output can be obtained at time t=t1>0, where values of t1 may range from picoseconds to milliseconds, but never zero.

Figure 4: Delay in system output

These delays may occur in the devices used to realize the system. However, today the major concern of designers are are the interconnecting wires which connect the various devices. They are the major bottleneck in the speed of the systems today. They occur due to parasitic resistances and capacitances present in the circuits designed.

A detailed discussion on Circuit Interconnects will be done in later lectures.

Recap

In this lecture you have learnt the following

- What is System?
- Design Abstraction Levels
- Delay and Interconnect Issues in physical circuits

Congratulations, you have finished Lecture 2.