Module 4 : Propagation Delays in MOS
Lecture 23 : Logical Effort of Multistage Logic Networks

Objectives

In this lecture you will learn the following

- Logical Effort of Multistage Logic Networks
- Minimizing Delay along a Path
- Few Examples

23.1 Logical Effort of Multistage Logic Networks

The logical effort along a path compounds by multiplying the logical effort of all the logic gates along the path. We denote it by the letter '**G**'. Hence,

$$G = \prod_i g_i \qquad \text{(where } g_i \text{ is the logical effort of single gate)}$$

The electrical effort along a path through the network is simply the ratio of the capacitance that loads the logic gate in the path to input capacitance of the first gate in the path. We denote it by the letter '**H**'.

$$H = C_{out}/C_{in} \qquad \text{where } C_{out} \text{ and } C_{in} \text{ refer to the output and input capacitances of the path as whole}$$

When fanout occurs within a logic network, some of the available drive current is directed along the path we are analyzing, and some are directed off that path. Branching effort (**b**) at the output of a logic gate is defined as

$$b = \frac{C_{on\text{-}path} + C_{off\text{-}path}}{C_{on\text{-}path}}$$

Where $C_{on\text{-}path}$ is the load capacitance along the path and $C_{off\text{-}path}$ is the capacitance of connections that lead off the path. If there is no branching in the path the branching effort is unity.

Branching effort along the entire path '**B**' is the product of branching effort at each of the stages along the $B = \prod_i b_i$ path.-

Path effort (**F**) is defined as- $F = G * B * H$

The path branching and electrical effort are related to the electrical effort of each stage as-

$$B * H = (C_{out}/C_{in}) \prod_i b_i = \prod_i h_i$$

The path delay **D** is the sum of the delays of each of the stages of logic in the path.

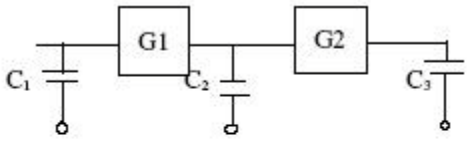
$$D = \sum_i d_i = D_F + P$$

where $\mathbf{D_F}$ is path effort delay and **P** is path parasitic delay which are given as –

$$D_F = \sum_i g_i * h_i \quad \text{and} \quad P = \sum_i p_i$$

23.2 Minimizing Delay along a Path

Consider two path stages as in figure 23.21.



Input capacitance:	C1	C2
Logical effort :	g1	g2
Parasitic delay :	p1	p2

Fig 23.21: An Example Circuit equating

The total delay of the above circuit is given by

$$D = (g_1 * h_1 + p_1) + (g_2 * h_2 + p_2)$$
$$\text{as } h_1 = C_2/C_1 \text{ and } h_2 = C_3/C_2$$
$$\text{So, } H = h_1 * h_2 = c_3/c_1$$

Substituting $h_2 = H/h_1$ in equation for **D** we get,

$$D = (g_1 * h_1 + p_1) + (g_2 * H/h_1 + p_2)$$

To minimize **D**, we take the partial derivative of **D** with respect to it to zero we get, $g_1 * h_1 = g_2 * h_2$

i.e. the product of logical effort and electrical effort of each stage should be equal to get minimum delay. This is independent of scale of circuit and of the parasitic delay. The delay in the two stages will differ only if the parasitic delays are different.

We can generalise this result for **N** stages as-

$$B * H = \prod_i h_i = h_1 * h_2 * \ldots\ldots * h_n \quad \text{and} \quad G = \prod_i g_i = g_1 * g_2 * \ldots\ldots * g_n.$$
$$\text{So, } F = G * B * H = (g_1 * h_1) * (g_2 * h_2) * \ldots\ldots * (g_n * h_n)$$

Hence, $F_{opt} = (gh)^n = (\hat{f})^n$, $\hat{f} = F^{1/N} = g_i * h_i$ and $D = N * F^{1/N} + P$, $h_i = F^{1/N}/g_i$

So,

$$C_{in,i} = \frac{g_i * C_{out,i}}{\hat{f}}$$

Example of Minimizing delay: Consider the path from A to B involving three two input NAND gates as in fig 23.22. The input capacitance of first gate is **C** and the load capacitance is also **C** . Find the least delay in this path and how should the transistors be sized to achieve least delay?

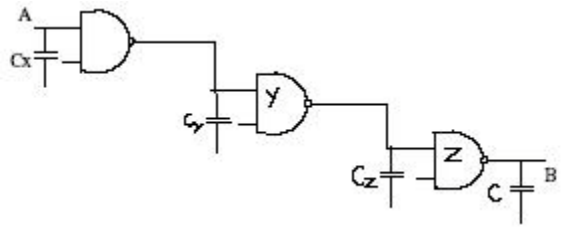


Fig 23.22: Example Circuit

Solution:
Logical effort of a two input NAND gate is **g = 4/3**
so **G = (4/3)*3 = 64/27 = 2.37 .**
B = 1 (as there is no branching) , **H = Cout / Cin = 1**
Path Effort **F = 64/27*1*1 = 64/27**

if each stage has same parasitic delay then **P = p1+ p2+p3 =6 pinv** (as all are two input), then $\hat{D} = NF^{1/N} + P = 3 * (4/3)3/3 + 6 = 10$

As, $C_{in,i} = g_i * C_{out,i} / \hat{f}$

So, **Cz = g3 * C/ (4/3) = C, Cy = g2 * C/ (4/3) = C**.

Now if **Cout = 8C,** then

$H = 8C/C = 8, \quad F = G * B * H = (4/3) * 1 * 8 = 18.96,$

$C_y = (8C) * (4/3)/(8/3) = 4C, \quad C_z = (4C) * (4/3)/(8/3) = 2C$ and

$\hat{D} = NF^{1/N} + P = 3 * (18.96) * 1/3 + 6 = 14$

$As\ Y = 8, \quad N = \frac{\ln 8}{\ln 2} = \frac{2.08}{0.693} = 3$

23.3 Reduction of Delay

For the minimum delay of the circuit we optimize the number of stages. Let total number of stages be N = n1 + n2

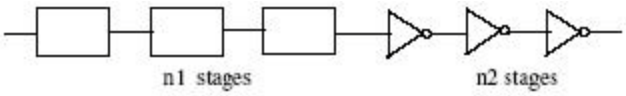


Fig 23.31: Example Circuit

$$\hat{D} = NF^{1/N} + \sum_{i=1}^{n1} p_i + n_2 p_{inv}$$

$$\Rightarrow \partial D / \partial N = -F^{1/N} \ln(F^{1/N}) + F^{1/N} + p_{inv} = 0$$

Let $\rho = F^{1/N}$, So $p_{inv} + \rho(1 - \ln \rho) = 0$

But the number of stages for minimum delay may not be the integer, so it is not feasible to implement it. So we realise the circuit by either taking the number of stages greatest integer of the obtained value or the one more then the greatest integer whatever gives us the minimun delay.

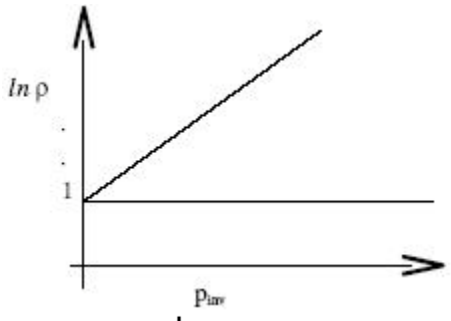


Fig 23.32: $\ln \rho$ *vs* p_{inv} *graph*

We will study about in more details in next chapter.

Recap

In this lecture you have learnt the following

- Logical Effort of Multistage Logic Networks
- Minimizing Delay along a Path
- Few Examples

Congratulations, you have finished Lecture 23.