IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

MICROELECTRONICS: DEVICES AND CIRCUITS

CLOCKING STRATEGIES FOR SEQUENTIAL DESIGN

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Outline

- Introduction
- Synchronous Design technique
- Clock Skew
- Clock jitter
- Impact of Clock Skew and Clock Jitter
- Sources of Skew and Jitter
- Design Techniques to Reduce of Skew and Jitter
- Clock Distribution
- Advantages of Synchronous Design
- Recapitulation

Introduction

- All sequential circuits have a well-defined switching events.
- The systemic switching ensure the circuit to be functional correctly.

Synchronous approach

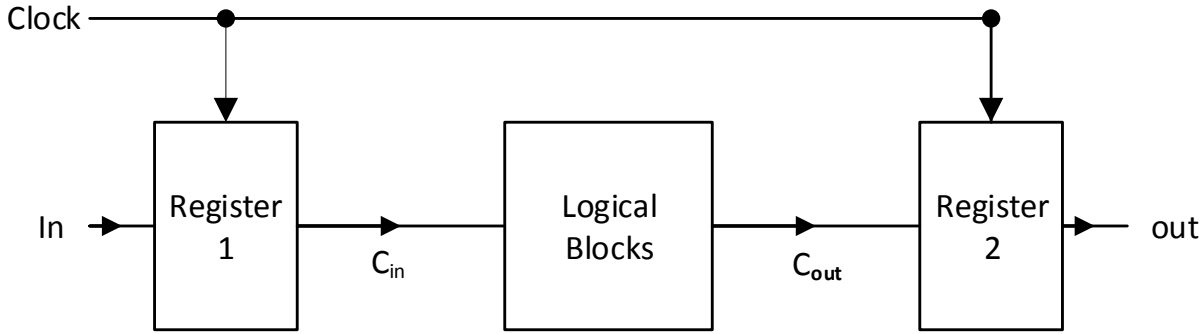
- All the circuit elements will be simultaneously updated with the global clock.
- Functionality ensure by the constraints of clock generation and proper distribution.

Asynchronous approach

- No global distributed clock is required.
- How ever these protocol results in increased complexity.

Synchronous Design technique - Introduction

- A synchronous signal is one that has the exact same frequency as local clock, and maintains a fixed phase offset with respect to the local clock.
- In such a timing methodology, the signal is “synchronized”.
- With the clock, data can be sampled directly without any uncertainty.
- Most straight forward type of interconnect.

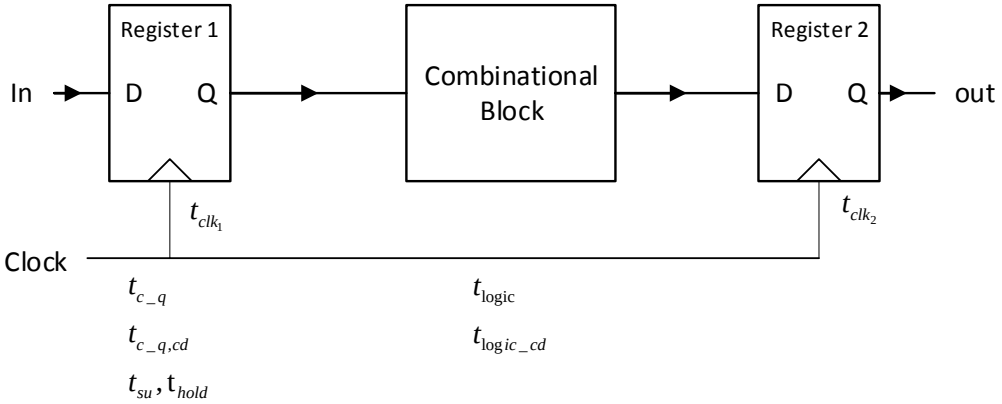


Synchronous interconnect methodology

Synchronous Timing Basics

A positive edge triggered system is assumed. Where –

- $t_{c_q,cd}$ = contamination or minimum delay of the register
- t_{c_q} = maximum delay of the register
- t_{su} = Setup time
- t_{hold} = hold time
- $t_{\log ic,cd}$ = Contamination delay of combinational block
- $t_{\log ic}$ = Maximum delay of the combinational block
- t_{clk_1} , t_{clk_2} = Positions of the rising edges of the clocks CLK_1 and CLK_2.



Pipelined datapath circuit and timing parameters

Under ideal conditions (t_{clk1} = t_{clk2}), the worst case propagation delays determine the minimum clock period required for this sequential circuit.

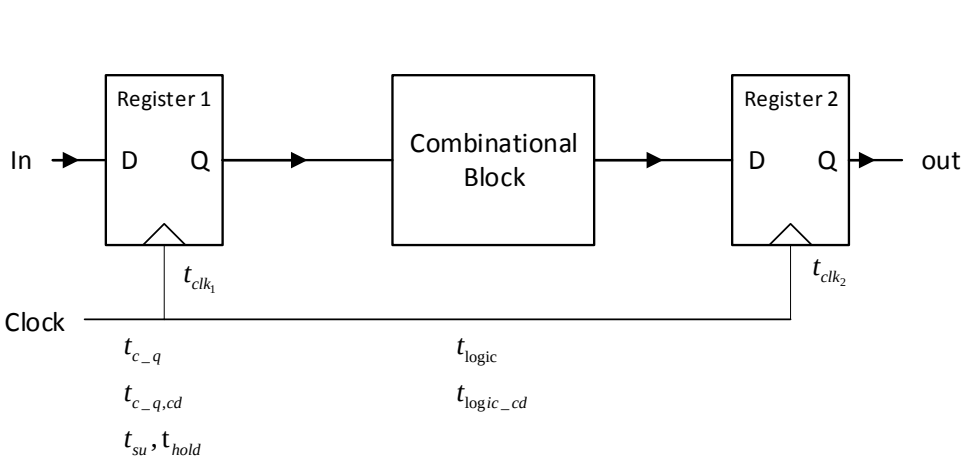
$$T > t_{c_q} + t_{\log ic} + t_{su}$$

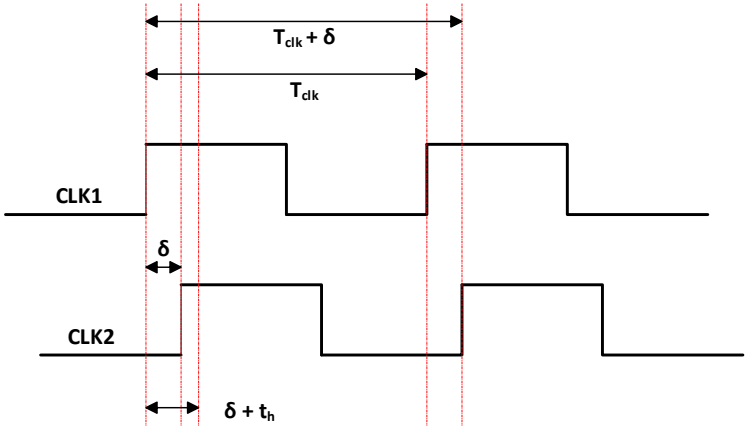
$$t_{hold} < t_{c_q,cd} + t_{\log ic,cd}$$

Clock Skew

- Because of process and environmental variations, the clock signal can have spatial and temporal variations.
- The spatial variation in arrival time of a clock transition on an integrated circuit is commonly referred to as **clock skew.**
- The clock skew between two points i and j on a IC is given by $\delta (i,j) = t_i - t_j$, where, t_i and t_j are the position of the rising edge of the clock with respect to a reference.
- The clock skew can be positive or negative depending upon the routing direction and position of the clock source.
- Clock skew is caused by static path-length mismatches in the clock load and by definition skew is constant from cycle to cycle.

Positive Clock Skew

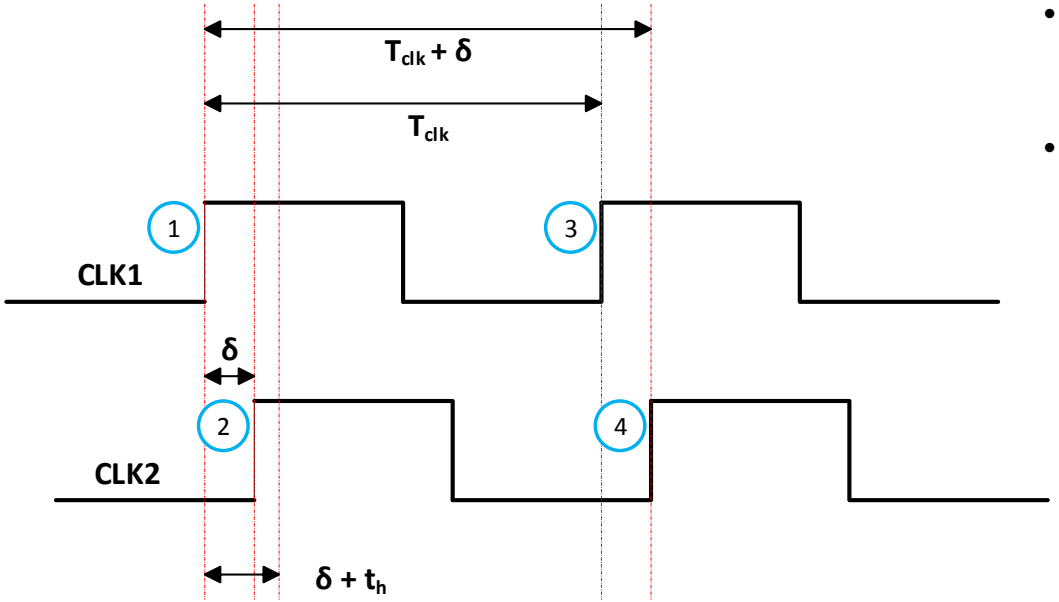




Timing diagram to study the impact of positive clock skew on performance and functionality.

The rising clock edge is delayed by a positive δ at the second register.

Positive Clock Skew



Timing constraint of positive clock skew

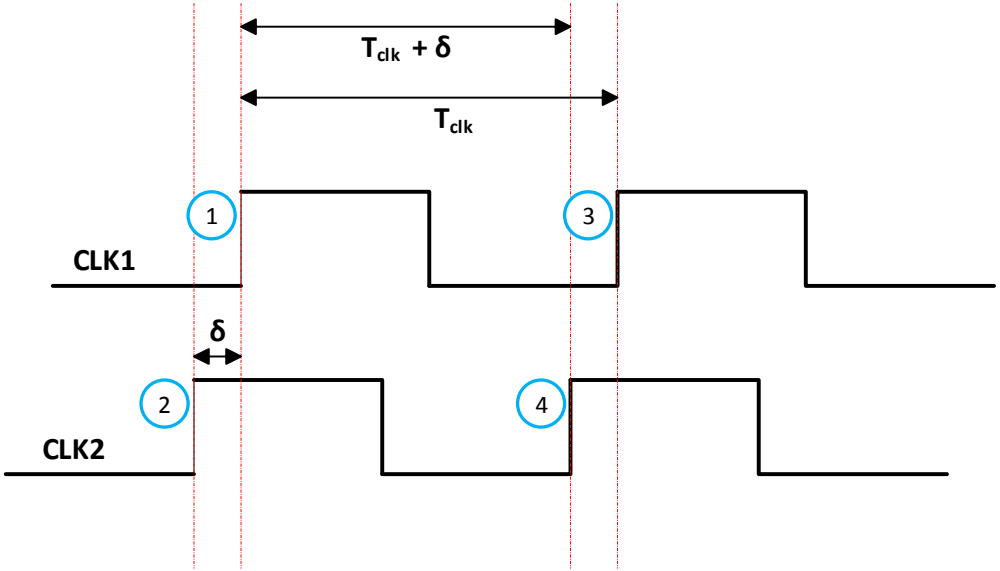
- If the clock skew is positive, the time available for signal to propagate from R1 to R2 is increased by the skew δ.
- The constraint on the minimum clock period can then be derived as:

$$T + \delta > t_{c_q} + t_{\text{logic}} + t_{su}$$

- if the minimum delay of the combinational logic block is small, the inputs to R2 may change before the clock edge 2, resulting in incorrect evaluation.
- The constraint of the minimum propagation delay through the register and logic would be

$$\delta + t_{hold} < t_{c_q,cd} + t_{\text{logic},cd}$$

Negative Clock Skew

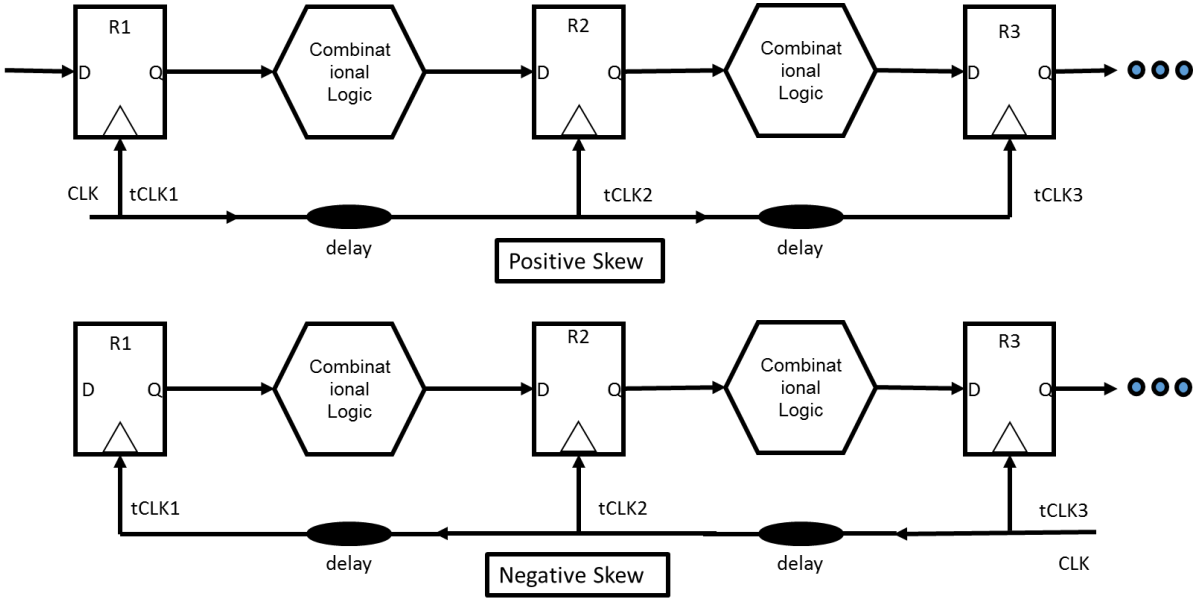


Timing diagram for negative clock skew (δ < 0).

- The rising edge of CLK2 happens before the rising edge of CLK1.
- Here δ is negative,
- The constraint on the minimum clock period becomes more stringent.

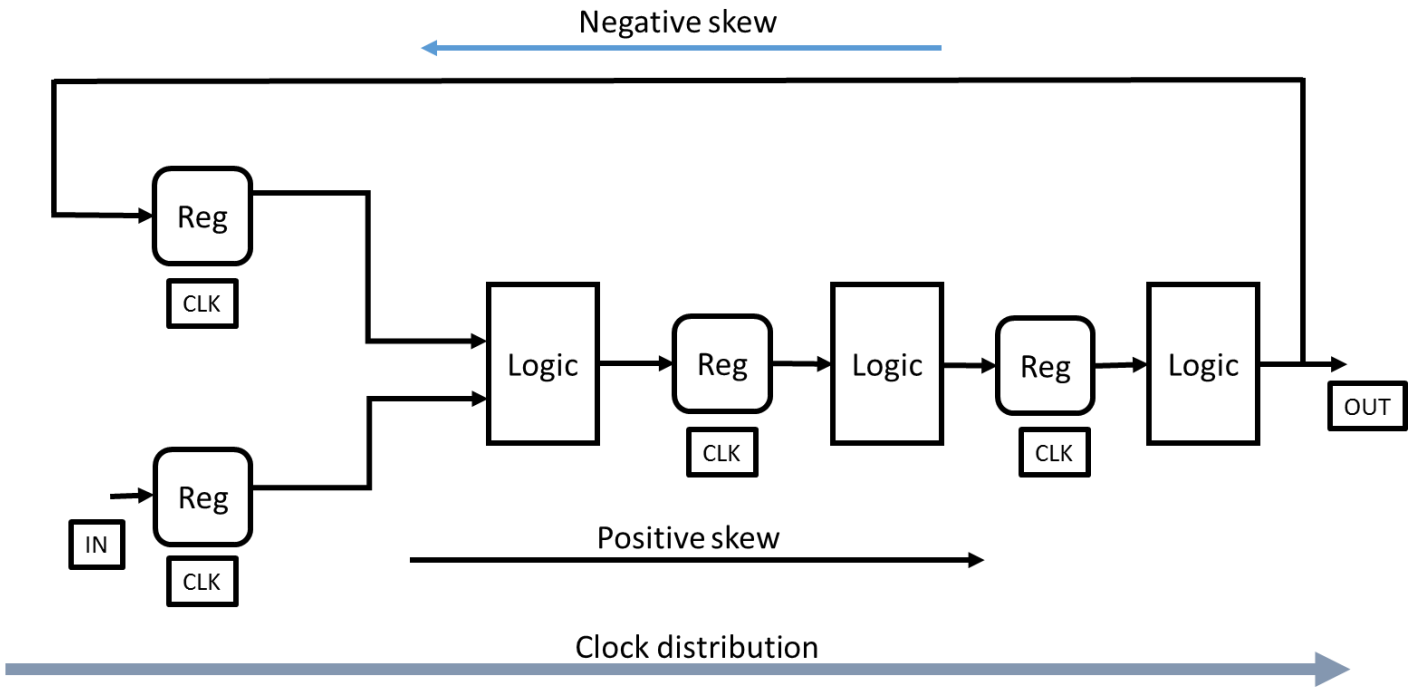
$$T + \delta > t_{c_q} + t_{\text{logic}} + t_{su}$$

Example scenarios for positive and negative clock skew



- During positive clock skew ($\delta > 0$), the main constraint is $\delta + t_{hold} < t_{c_q,cd} + t_{\log ic,cd}$
- The circuit does malfunction **independent of the clock period.**
- During negative clock skew ($\delta < 0$), When the clock is routed in the opposite direction of the data.

Timing issue in Datapath with feedback



Clock jitter

- **Clock jitter** refers to the **temporary variation** of the clock period at a given point. means the clock period can reduce or expand on a cycle-by-cycle basis.
- Cycle-to-cycle jitter refers to time varying deviation of a single clock period,
- At given location i,

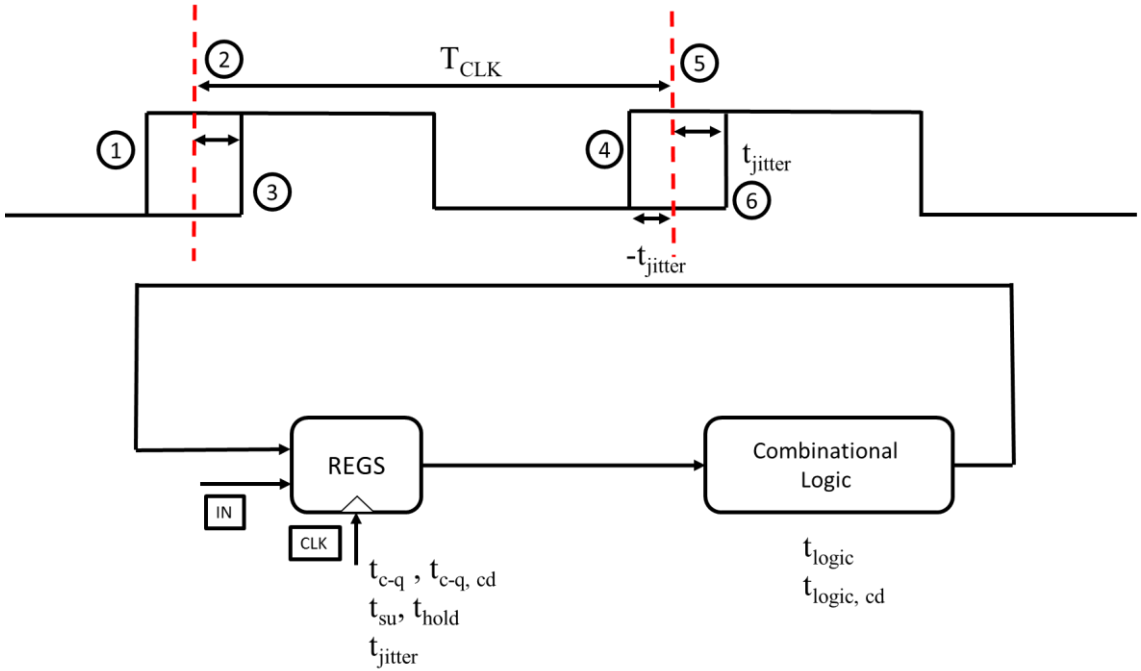
$$T_{jitter,i}(\mathrm{n}) = T_{i,n+1} - T_{i,n} - T_{CLK}$$

Where, $T_{i,n}$ is the clock period for period n,
$T_{i,\,n+1}$ is clock period for period n+1,
T_{CLK} is the nominal clock period.

Circuit performance under clock jitter

- Jitter directly impacts the performance of a sequential system.
- The total time available to complete the operation is reduced by 2 t_{jiiter} in the worst case.

$$T_{clk} - 2t_{jitter} \geq t_{c_q} + t_{\text{logic}} + t_{su}$$



Timing diagram of a circuit under clock jitter

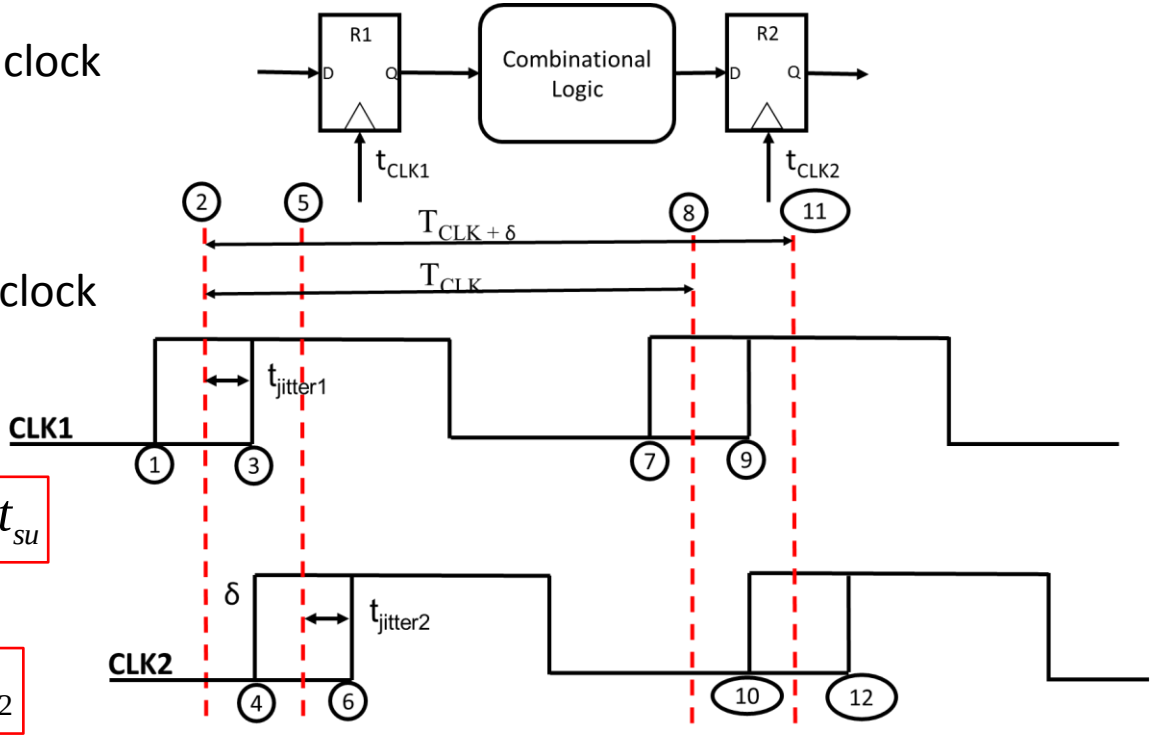
Impact of Clock Skew and Clock Jitter

- A static skew δ is present in two clock signals (CLK1 and CLK2). (δ >0).
- CLK1 has jitter of $t_{jitter1}$.
- CLK2 has jitter of $t_{jitter2}$.
- The constraint on the minimum clock period -

$$T_{CLK} + \delta - t_{jitter1} - t_{jitter2} \geq t_{c_q} + t_{logic} + t_{su}$$

or

$$T \geq t_{c_q} + t_{logic} + t_{su} - \delta + t_{jitter1} + t_{jitter2}$$



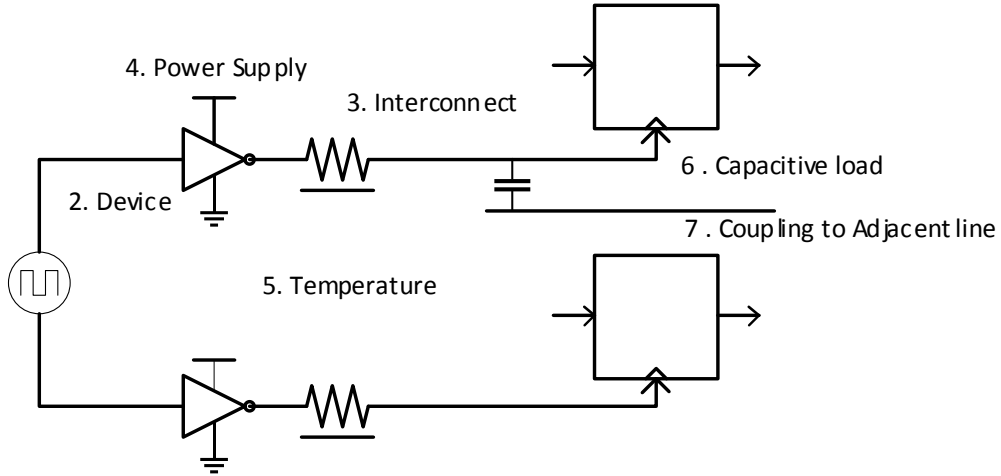
Circuit performance under skew (δ >0). and jitter

Source of Skew and Jitter

- A ideal clock signal can not be achieved because of the variety of the process and environmental variations.
- Off chip or on-chip generated clock signal is distributed through multiple “matched” path.
- Errors can be classified in to two categories :

- **1) Systematic Error**
  - Predictable.
  - Identical in chip to chip
  - Modeled and corrected at design time.

- **2) Random Error**
  - Manufacturing variations
  - Difficult to model and eliminate
  - e.g., dopant fluctuations



various sources of skew and jitter

Sources of Skew and Jitter

1. **Clock generation**
   - Source of clock generator itself causes jitter.
   - Core of a PLL is a Voltage Control Oscillator- which is very sensitive to the device noise and supply variation.
   - Analog circuits are affected by noisy digital circuits.
   - Cycle-to-cycle clock variation due to substrate noise.

2. **Manufacturing Device Variations**
   - Mismatch among the clock buffer circuits in the distributed network.
   - Because of the process variations, device parameters in buffer circuits vary –results static skew error.
   - Variation in oxide layer, dopant profile, dimension ratio affect the over all performance.

Sources of Skew and Jitter

3. **Mismatch in Interconnects**
   - The dimension variations in routing causes interconnect capacitance and resistances to vary – statics skew between different paths.
   - Inter-level-thickness variations.
   - Variation in polish rate in planarization process.
   - Deviation in the width of the wires and line spacing.

4. **Environmental variations**
   - Most significant sources to contribute jitter and skew.
   - Temperature gradient because of variation in power dissipation.
   - Activity region is chip varying depending on design.
   - Variation in temperature is time varying.

Sources of Skew and Jitter

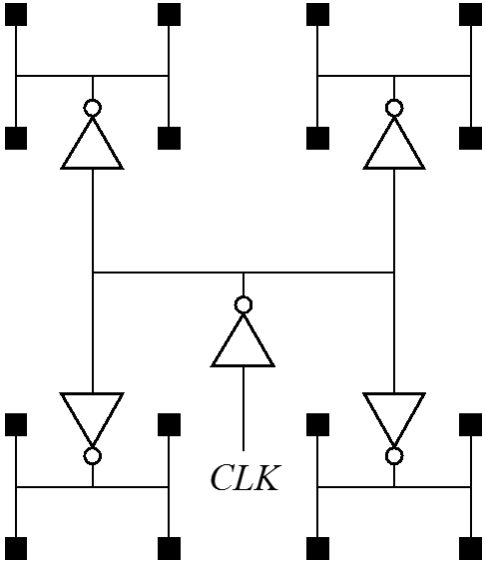
5. **Power supply variations**
   - Major source of clock jitter in circuit.
   - Delay through buffers is a very strong function of power supply.
   - The buffer delay along one path is very different than the buffer delay along another path.
   - Instantaneous IR drops along the power grid due to fluctuations in switching activity.
   - Clock signal is modulated on a cycle-by-cycle basis, resulting in jitter.

6. **Capacitive coupling**
   - The variation in capacitive load also contributes to timing uncertainty.
   - Coupling between the clock lines and adjacent signal wires.
   - Variation in gate capacitance.
   - The adjacent signal can transition in arbitrary directions and at arbitrary times, This results in clock jitter.

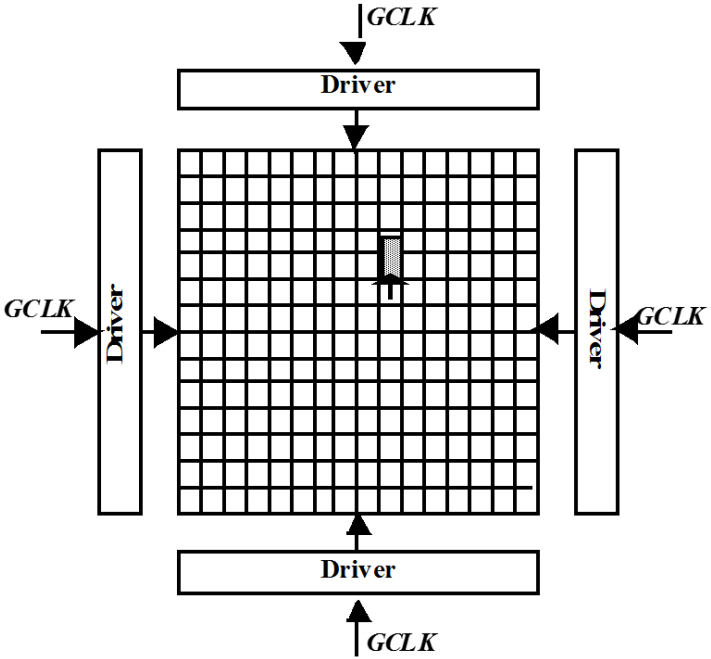
Design Techniques to Reduce of Skew and Jitter

- A balanced clock paths from a central distribution sources - using H-tree structures or routed tree structures.
- The use of local clock grids can reduce skew.
- If data flows in one direction, route data and clock in opposite directions.
- Avoid data dependent noise by shielding clock wires from adjacent signal wires.
- Dummy fills are very common and reduce skew by increasing uniformity.
- High frequency power supply variation can be reduced by addition of on-chip decoupling capacitors.

Clock Distribution



H-tree



Grid structures

Advantages of Synchronous Design

- **Ensures that the physical timing constraint are met**
  - After the system comes in steady state, only the next clock starts.
  - Allowed only the legal values for the next computation.
  - Always consider the worst case to ensure physical timing constraint.
- **Serves as a logical ordering mechanism**
  - For a global system events.
  - All the system events are clearly orchestrated by clock.
  - Structured and deterministic approach.

Recapitulation

- As a result of process and environmental variations, the clock signal can have spatial and temporal variations.
- Clock skew and jitter has a major impact on the functionality and performance of a system.
- Clock skew is caused by static path-length mismatches in the clock load and by definition skew is constant from cycle to cycle.
- Realize in clock distribution is that the absolute delay through a clock distribution path is not important; what matters is the relative arrival time between the output of each path at the register points.

Thank You