IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

# MICROLECTRONICS: DEVICES TO CIRCUITS

## Sequential Logic Design-I

**SUDEB DASGUPTA**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



# Outline

- Introduction
- Timing Metrics for Sequential Circuits
- Classification of Memory Elements
- Static Latches and Registers

(a) The Bi-stability Principle

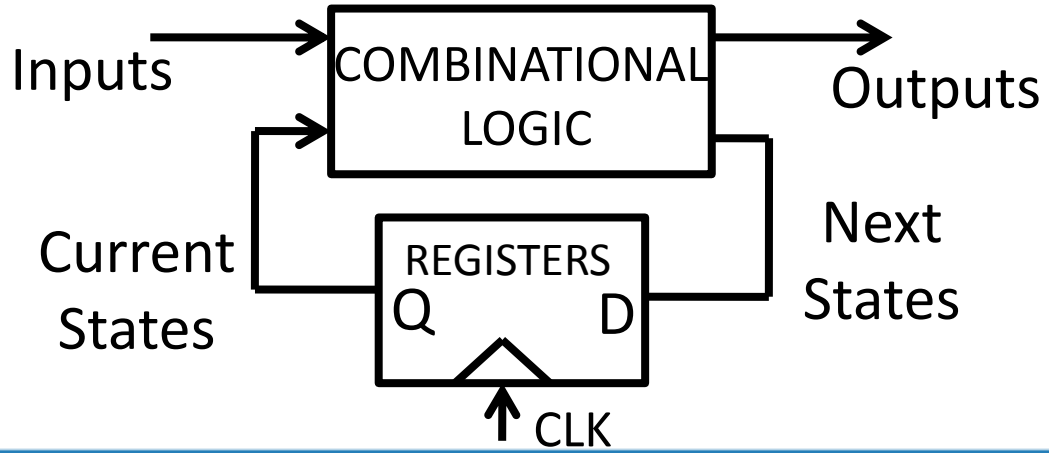
(b) Multiplexer Based Latches

(c) Master-Slave Edge Triggered Register

(d) Low Voltage Static Latches

# Introduction

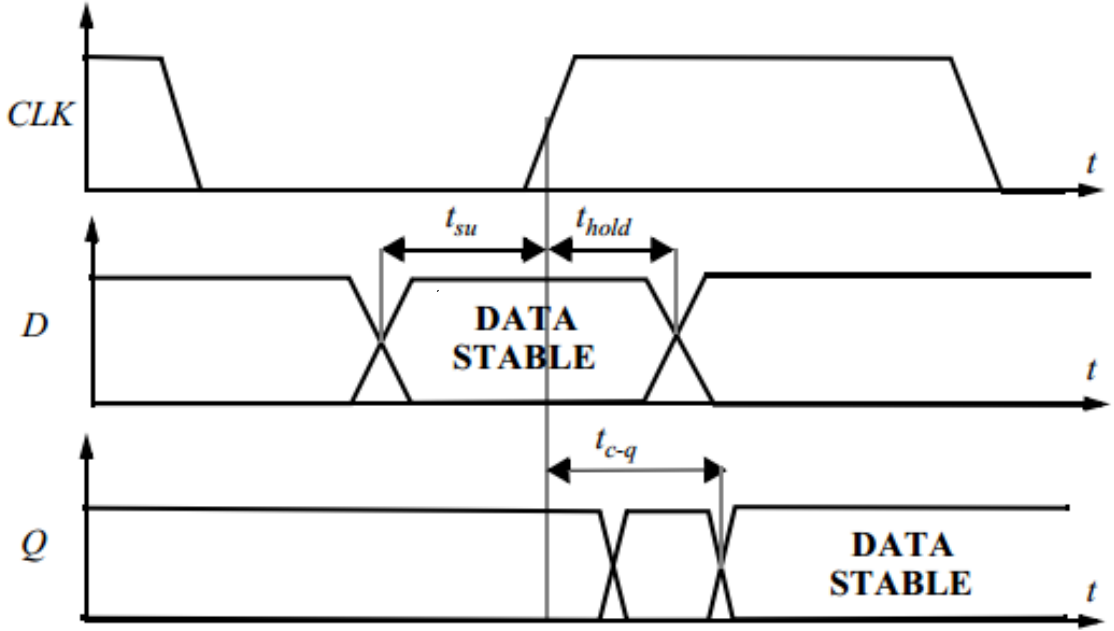
- Combinational Logic Circuits are the function of current input values but Sequential Logic Circuits are the function of current values of the inputs and also on the preceding input values.
- In other words, a sequential circuit remembers some of the past history of the system-*it has memory*.



# Timing Metrics for Sequential Circuits

- *Setup Time ($t_{su}$)*-The time that the data input must be valid before the clock transition. (i.e. 0⟶1 transition for a positive edge-triggered register).
- *Hold Time ($t_{hold}$)*-The data input must remain valid after the clock edge.
- *Clock Period (T)*-The time at which the sequential circuit operates, must thus accommodate the longest delay of any stage in the network.
- $t_{plogic}$-the worst propagation delay.
- $t_{cd}$-minimum delay which is also called contamination delay.

# Cont…




$$T \geq t_{cq} + t_{plogic} + t_{su}$$

$$t_{cdregister} + t_{cdlogic} \geq t_{hold}$$

Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

# Classification of Memory Elements

*Foreground versus Background Memory-*

- Memory that is embedded into logic is foreground memory is often organized as individual registers or register banks.
- Large amounts of centralized memory core are referred to as background memory.

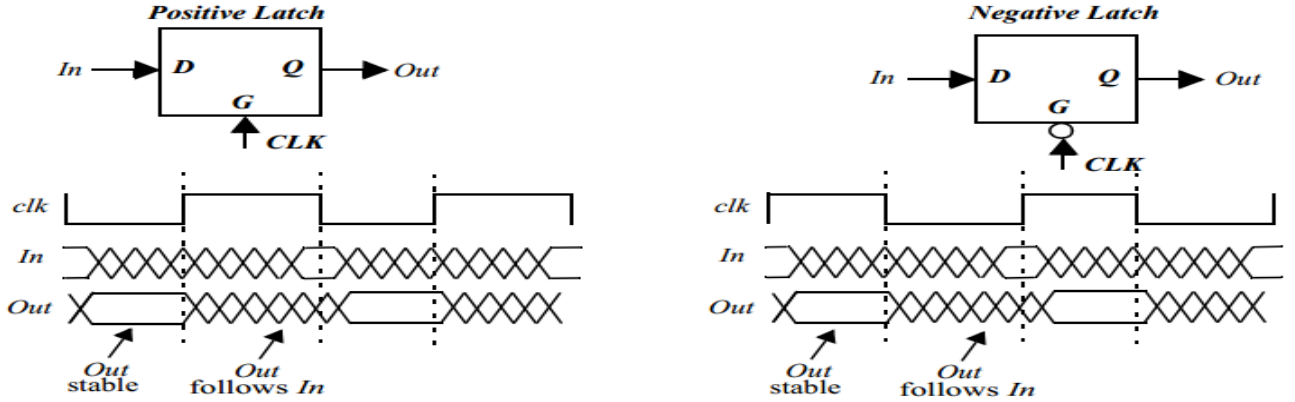
*Static versus Dynamic Memory-*

- Static memories preserve the state as long as the power is turned on. They are built by using positive feedback or regeneration.
- Dynamic memories store data for a short period of time, perhaps milliseconds.

## *Latches versus Registers-*

**Cont…**

- A latch is a level sensitive circuit that passes the input to the output when clock signal is high. This latch is said to be in transparent mode.
- Contrary to level-sensitive latches, edge-triggered registers only sample the input on a clock transition-that is, 0→ 1 for a positive edge triggered register and 1→0 for negative edge triggered register.

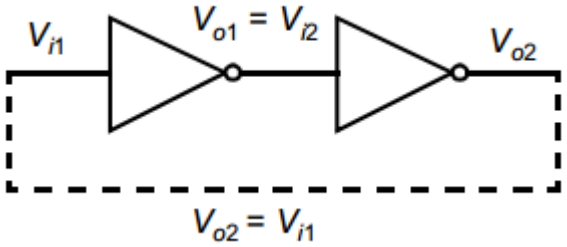


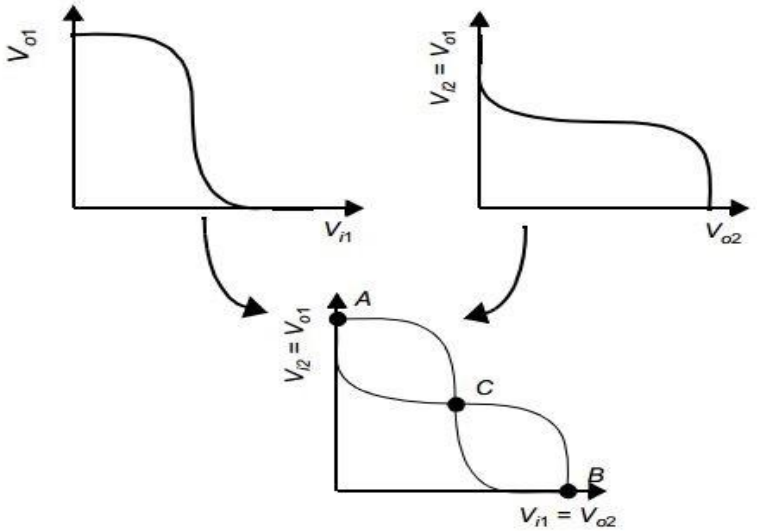

Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuit,” PHI Learning Pvt. Ltd., 2011.

# Static Latches and Registers

*The Bi-stability Principle-*

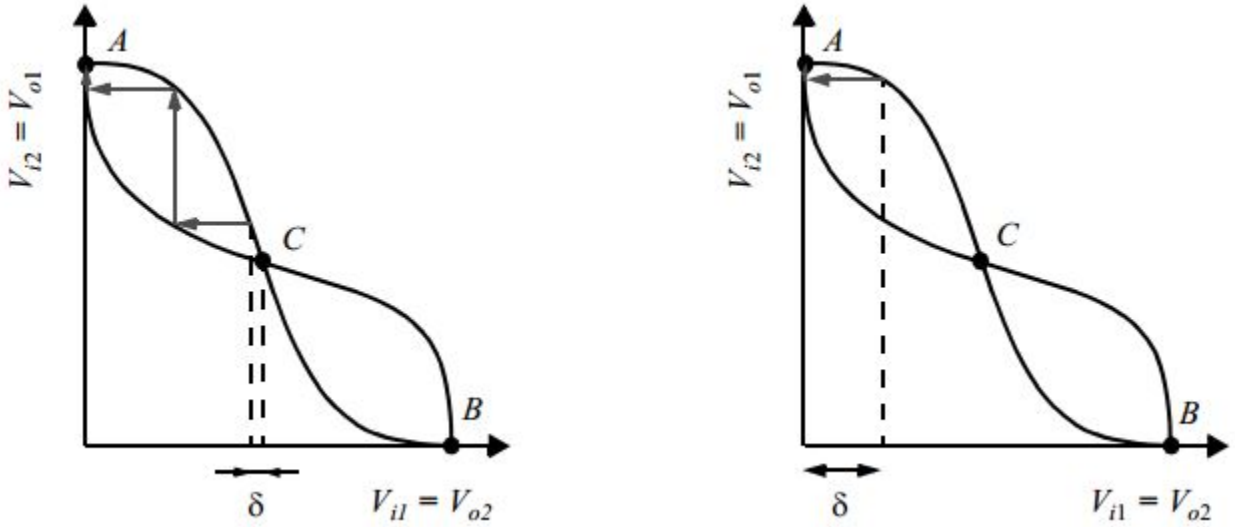
- Static memories use positive feedback to create a bi-stable circuit-a circuit having two stable states that represent 0 and 1.




Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

- When the gain of the inverter in the transient region is larger than 1, A and B are the only stable operation points, and C is a meta-stable operation point.



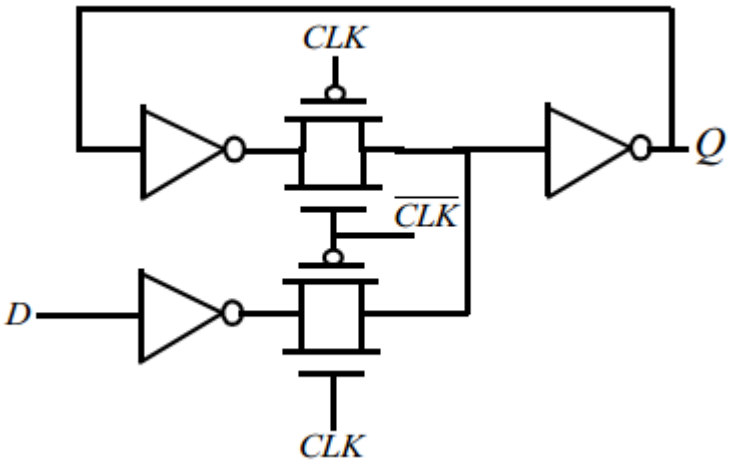

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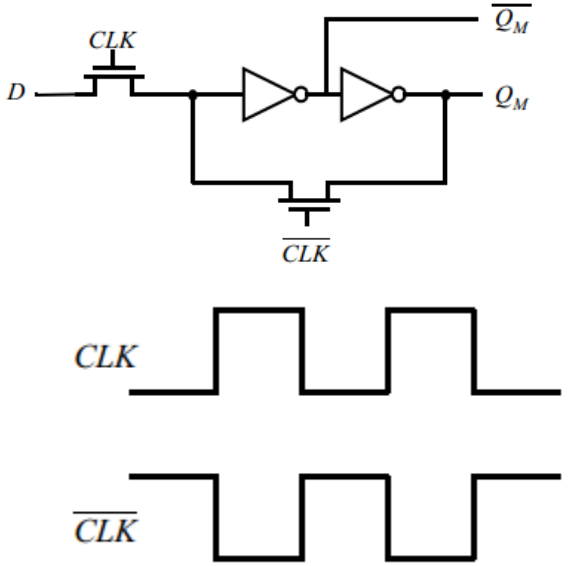
- A bi-stable circuit also known as flip-flop is useful only if there exists a means to bring it from one state to the other one. In general two different approaches may be used-

1. *Cutting the feedback loop-* Once the feedback loop is open, a new value can easily be written into output. Such a latch is called multiplexer based.
2. *Overpowering the feedback loop-* By applying a trigger signal at the input of the flip-flop, a new value is forced into the cell by overpowering the stored value. A careful sizing of the transistors in the feedback loop is necessary.

# *Multiplexer-Based Latches-*

- The most robust and common technique to build a latch involves the use of transmission-gate multiplexers.

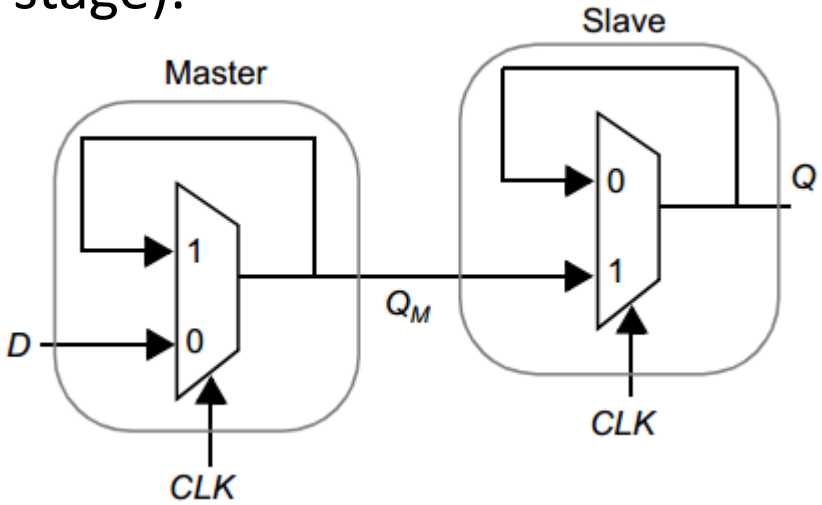


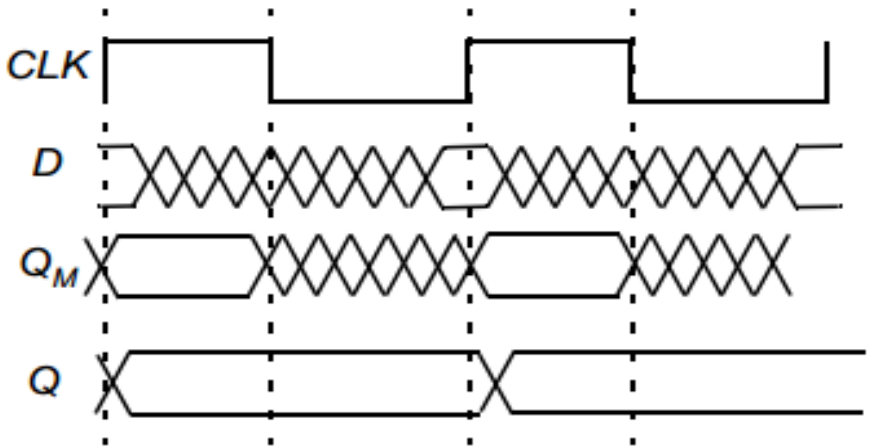




Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuit,” PHI Learning Pvt. Ltd., 2011.

# *Multiplexer-Based Latches-*

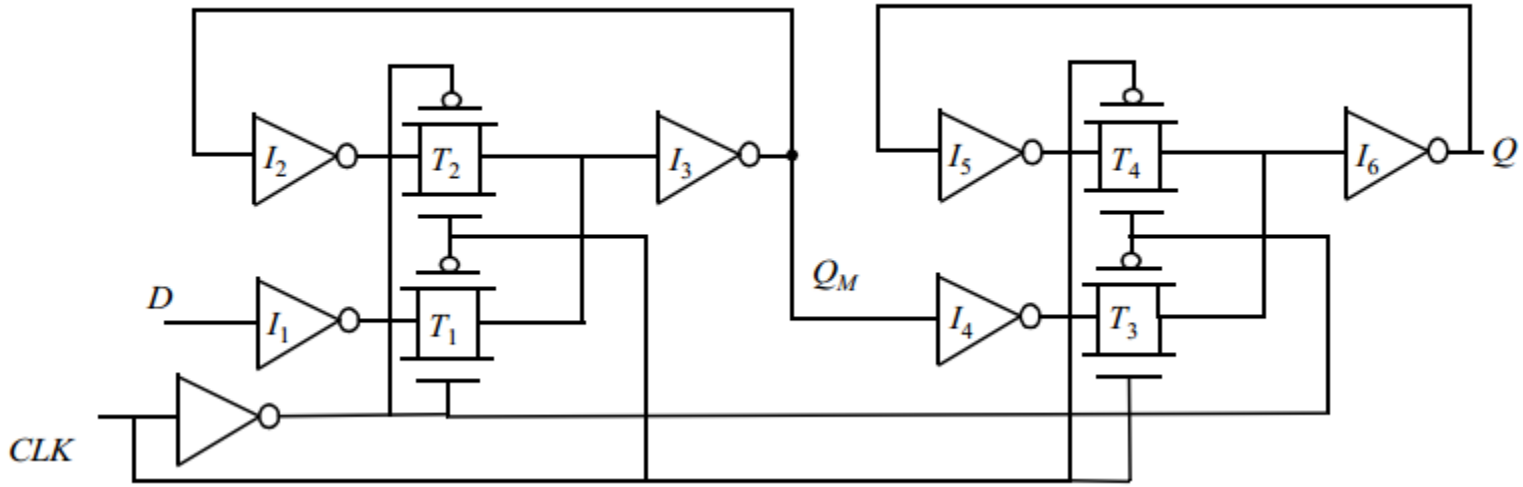
- The most common approach for constructing an edge-triggered register is to use master slave configuration. The register consists of cascading a negative latch (master stage) with a positive one (slave stage).




Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

# Cont…



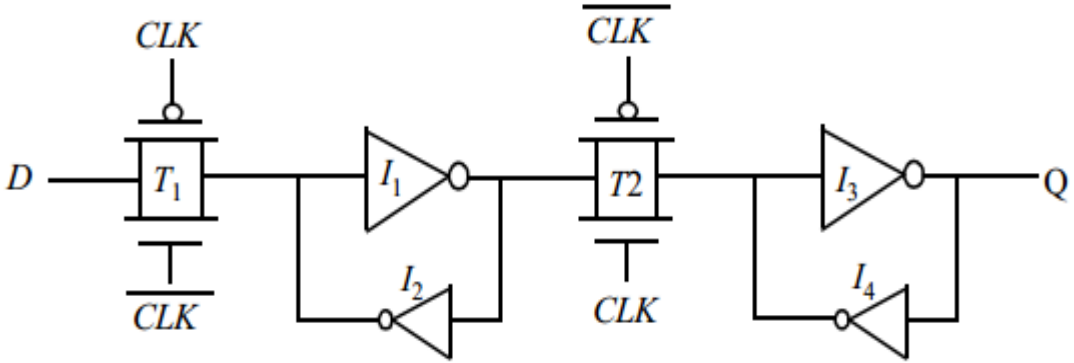

$$t_{su} = 3\times t_{pd_inv} + t_{pd_tx}.$$

$$t_{c\text{-}q} = t_{pd_inv} + t_{pd_tx}.$$

$$t_{hold} = 0$$

# Cont…

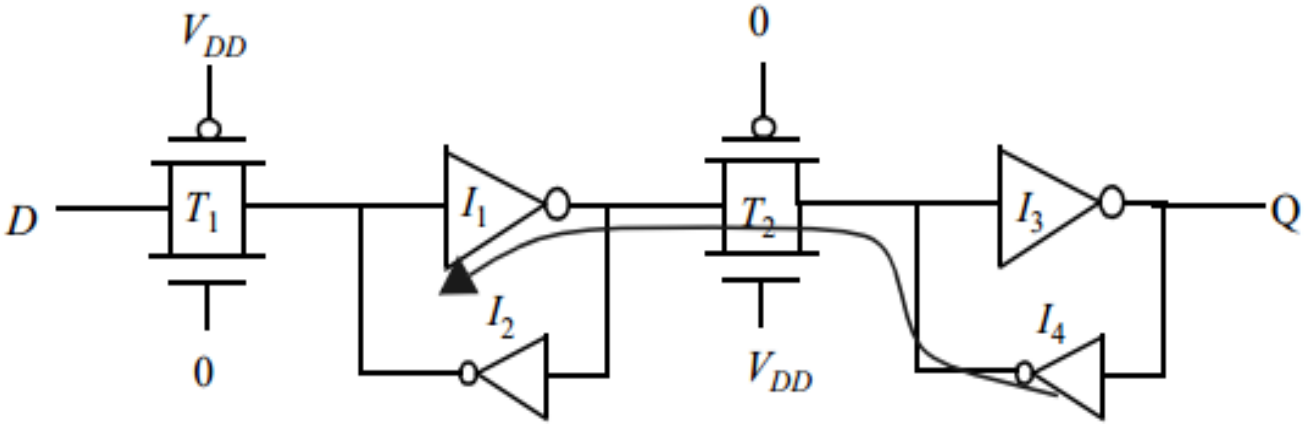
- The drawback of the transmission gate register is the high capacitive load presented to the clock signal.
- One approach to reduce the clock load at the cost of robustness is to make the circuit ratioed.




Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuit,” PHI Learning Pvt. Ltd., 2011.

# Cont…

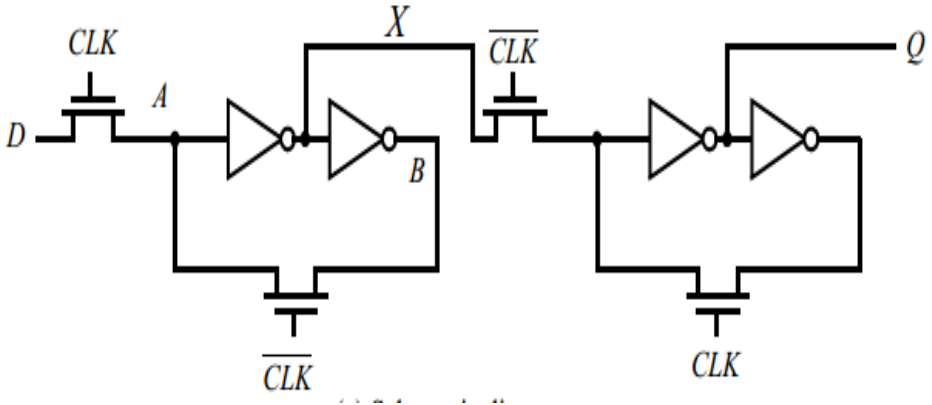
- The penalty paid for the reduced in clock load is an increase design complexity. The sizing of the transmission gate is a crucial parameter.
- Another problem with this scheme is reverse conduction.

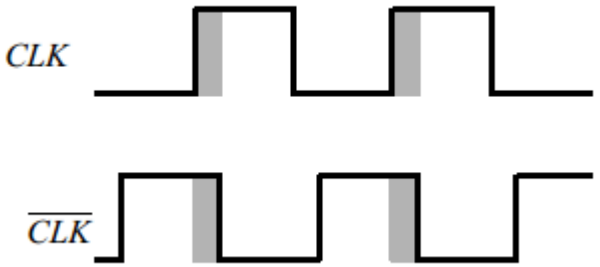



Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuit,” PHI Learning Pvt. Ltd., 2011.

# *Non-Ideal Clock Signals-*

- So far, we have assumed CLK is a perfect inversion of CLK, or in other words, that the delay of the generating inverter is zero. This effect is called clock skew.

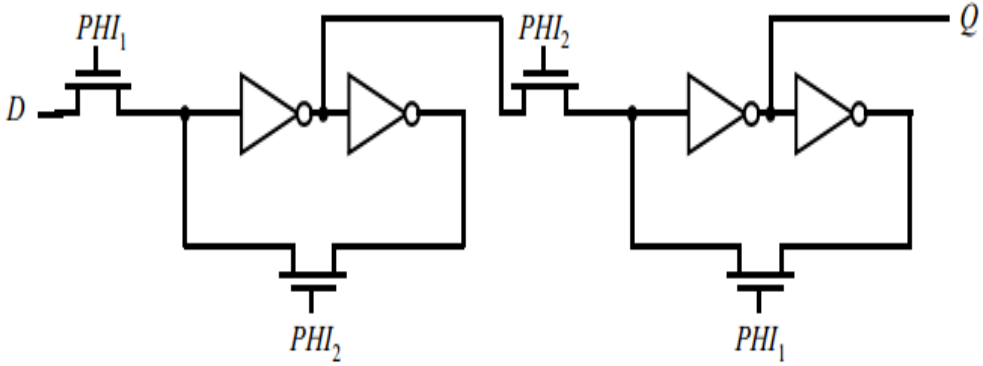


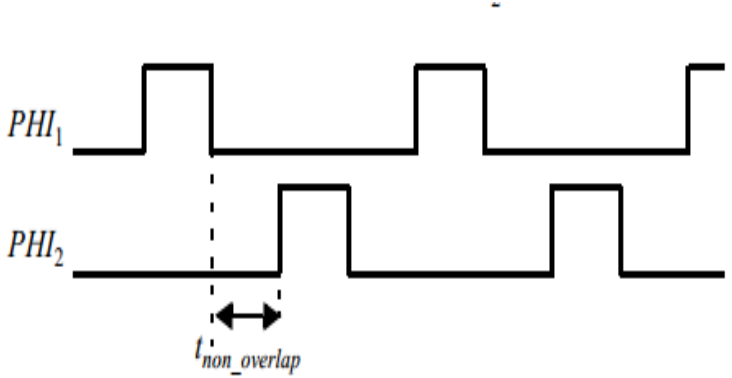




Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuit,” PHI Learning Pvt. Ltd., 2011.

# Cont…

- These problems can be avoided by using two non-overlapping clocks instead $PH_1$ and $PH_2$.

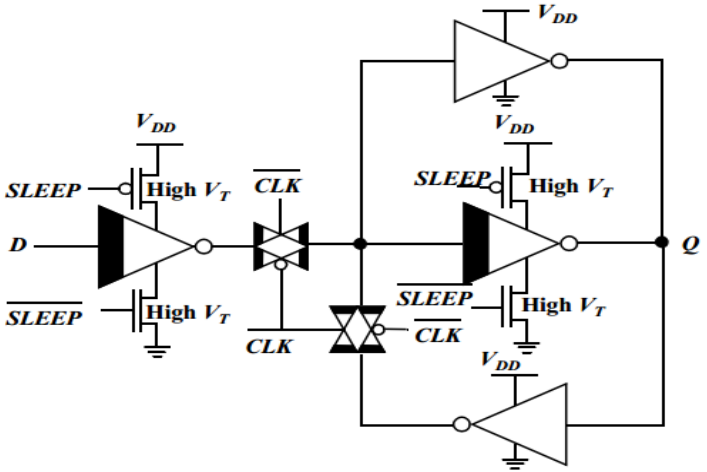



Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuit,” PHI Learning Pvt. Ltd., 2011.

## *Low Voltage Static Latches-*

- The scaling of the supply voltage is critical for low-voltage operation.
- Scaling to low supply voltages thus requires the use of reduced threshold devices.
- One approach to solve this problem is- Multiple Threshold Devices.




Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

# Recapitulation

- The sequential logic circuit has memory in which the output depends on the current input as well as preceding inputs.
- A latch is a level sensitive device while a register is an edge triggered device.
- Static memories use positive feedback to create a bi-stable circuit. This is having two stable states and one meta-stable states.
- To avoid the problem of Non-ideal clocks, we prefer two non-overlapping clocks.
- For low-voltage devices and scaling of the supply voltage, we prefer multiple threshold devices.

# Thank You