IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

MICROELECTRONICS: DEVICES TO CIRCUITS

Combinational Logic Design-IV

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

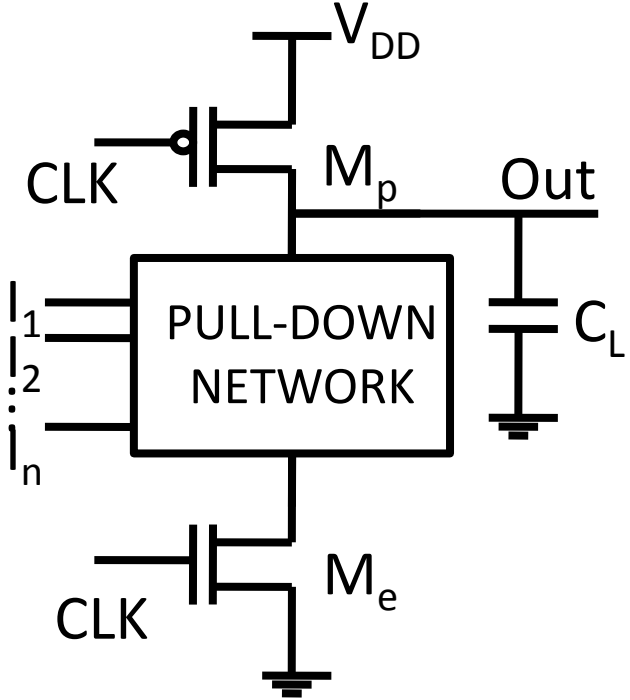


Outline

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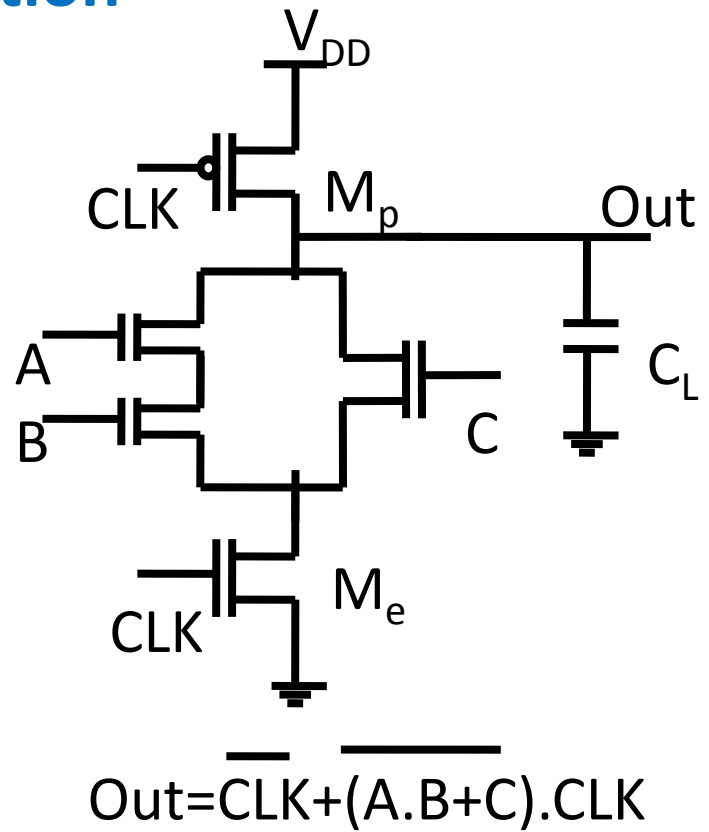
Dynamic CMOS Design: Basic Principles

- An alternate logic style to avoid static power dissipation is called Dynamic CMOS Design.



Pre-charge and Evaluation

- When CLK=0, the Out node is pre-charged to V_{DD} through M_p. During this time M_e is off which disables the PDN.
- For CLK=1, M_p gets off while M_e enables the PDN and based on the input topology of PDN the Out node gets discharged.
- Once the Out node is discharged, it cannot be charged until the next pre-charge cycle.

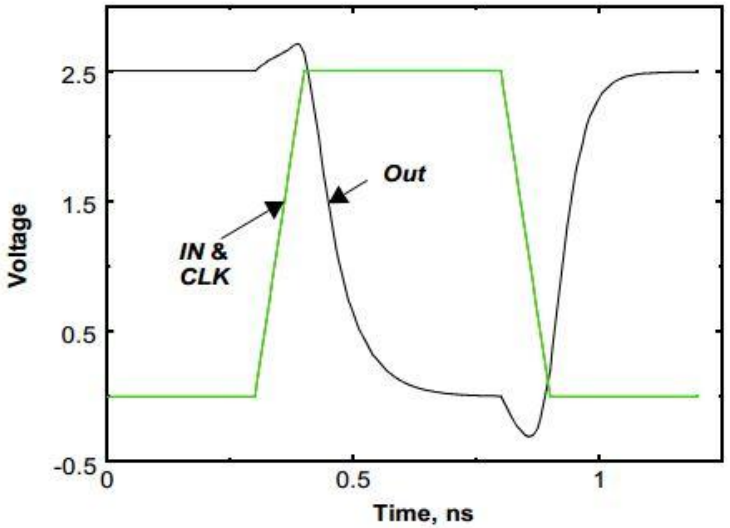


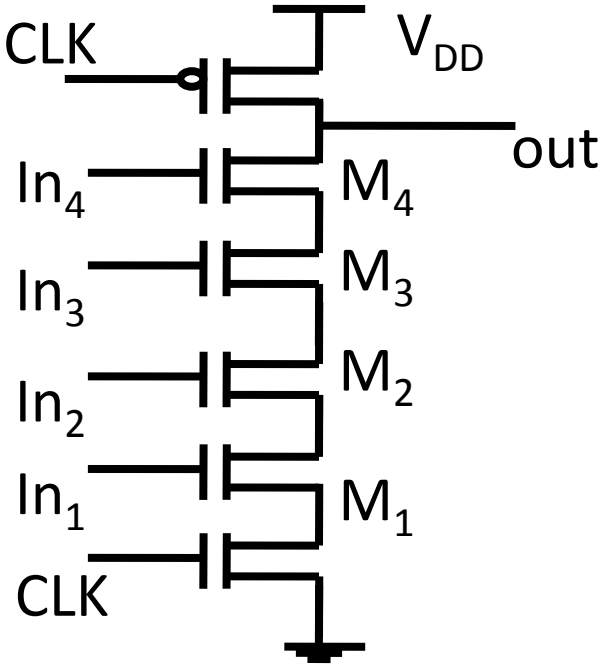
Properties of Dynamic Logic Gate

- The construction of the PDN is same as static CMOS.
- The number of transistor is substantially lower than in the static case, (N+2) versus 2N.
- It is non-ratioed. The sizing of PMOS pre-charge device is not important for realizing proper functioning of the gate.
- It only consumes dynamic power. The overall power dissipation, however, can be significantly higher compared with a static logic gate.
- These gates have faster switching speeds due to reduced load capacitance attributed to the lower number of transistor per gate and also due to the absence of short circuit current.

Speed and Power Dissipation of Dynamic Logic Gate

- The main advantage of dynamic logic are increased speed and reduced implementation area.



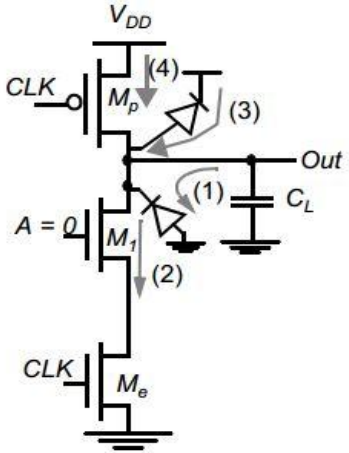


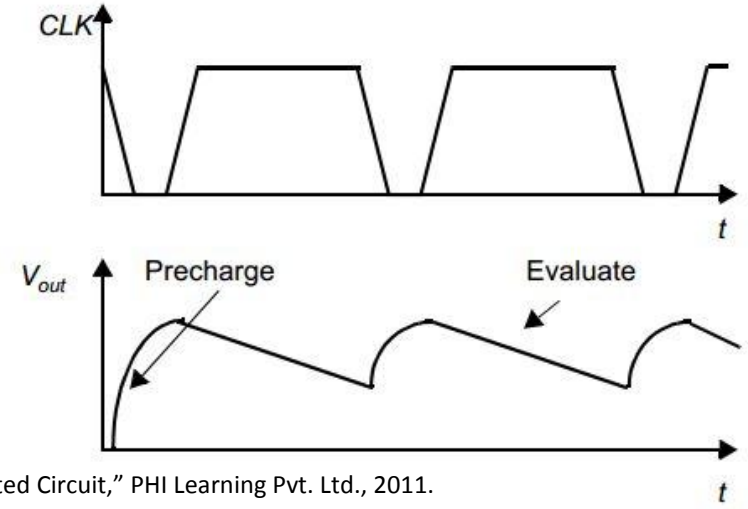
Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Signal Integrity Issues in Dynamic Design

1. Charge Leakage

- Ideally, if the pull-down network is off then output should be at V_{DD} during the evaluation phase.
- However, this charge gradually leaks away due to leakage currents.

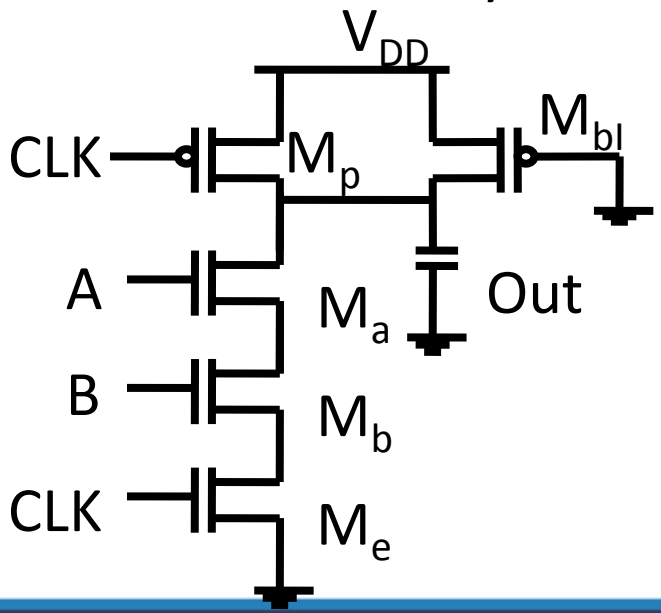


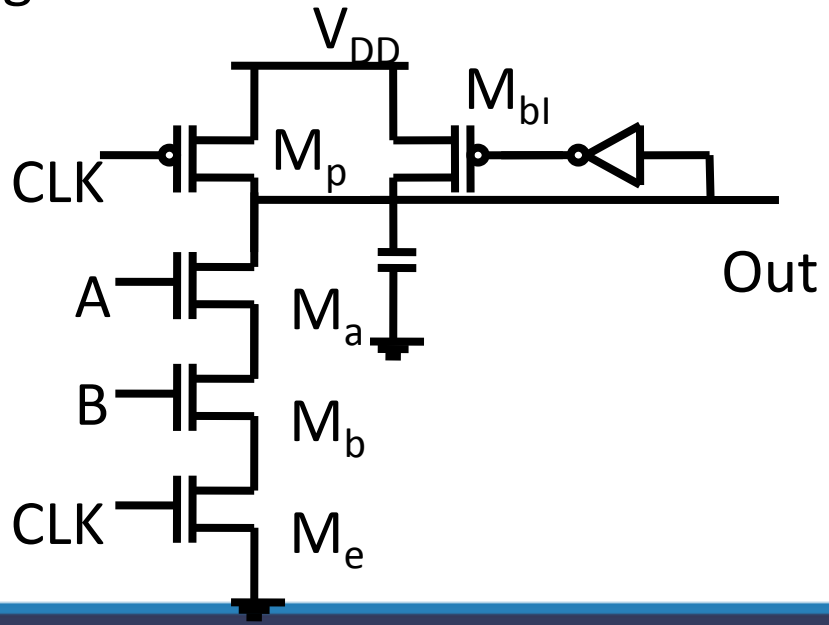


Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Charge Leakage Solution- Bleeder Transistor

- The reduction in the output impedance during evaluation phase will solve the leakage problem.
- This can be achieved by introducing a Bleeder Transistor.



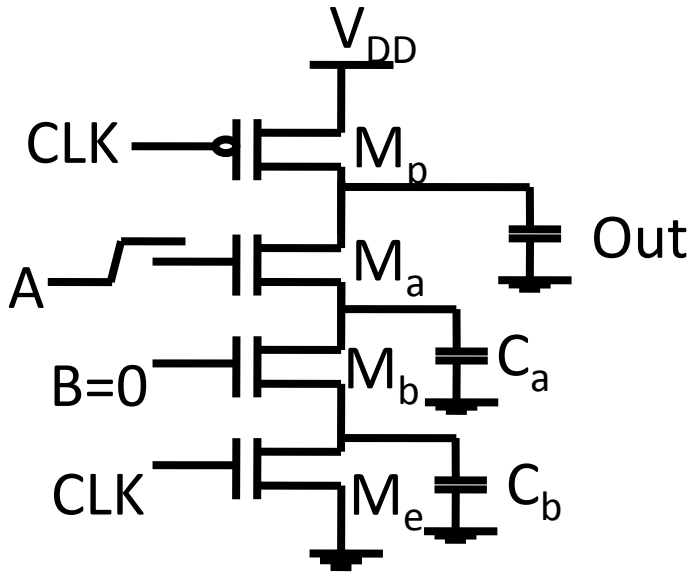


2. Charge Sharing

- Let the initial conditions are- $V_{out}(t=0)=V_{DD}$ and $V_X(t=0)=0$, then-

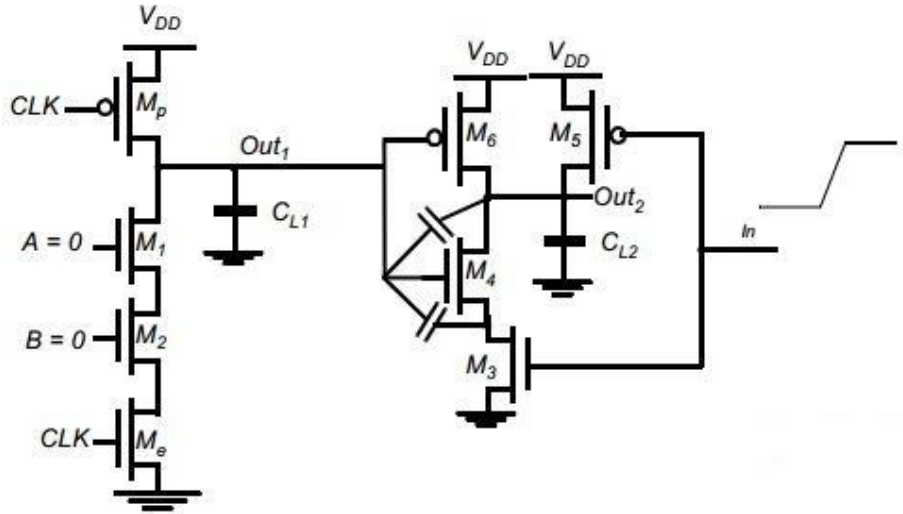
➢ Case-I ($\Delta V_{out}<V_{Tn}$)- the final value of V_X is $V_{DD}-V_{Tn}$

➢ Case-II ($\Delta V_{out}>V_{Tn}$)- then V_X and V_{DD} reach the same value. $\Delta V_{out}=-V_{DD}\left(\frac{C_a}{C_a+C_L}\right)$



3. Capacitive Coupling

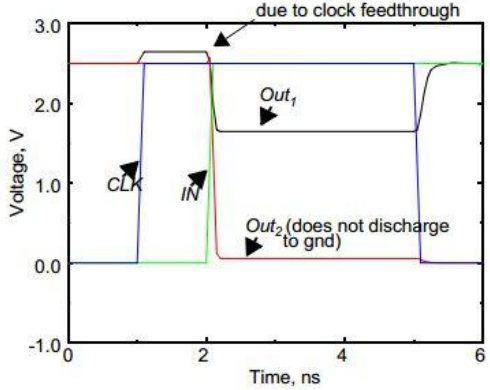
- The relative high impedance of the output node makes the circuit very sensitive to crosstalk effects. The wire next to a dynamic node may couple capacitive and destroy the floating node.



Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuit,” PHI Learning Pvt. Ltd., 2011.

4. Clock Feedthrough

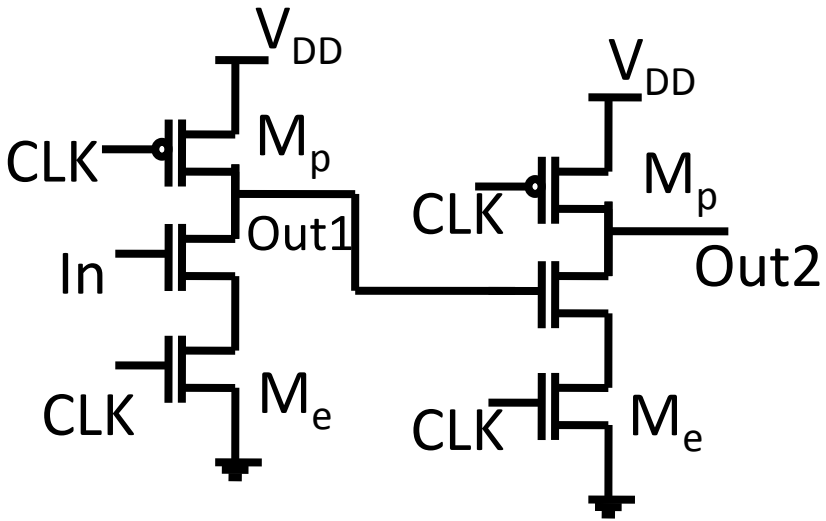
- An effect caused by the capacitive coupling between clock input of the precharge device and the dynamic output node.
- The danger of clock feedthrough is that it may cause the normally reverse biased junction diodes of precharged transistor to become forward biased, eventually results in faulty operation.

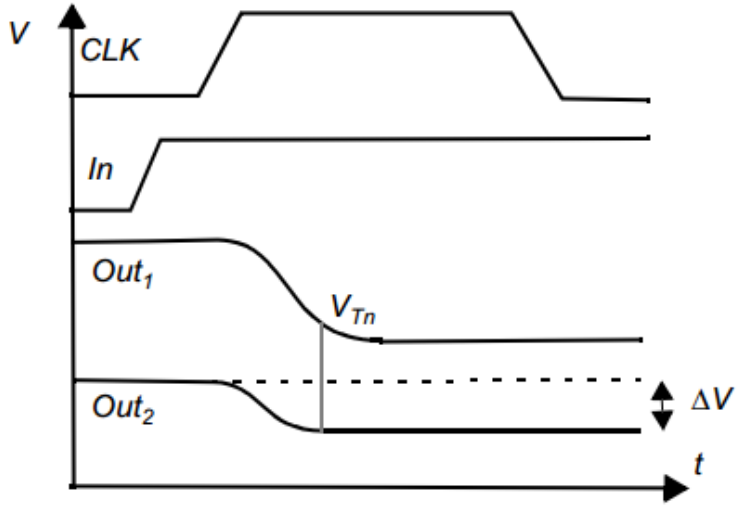


Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Cascading Dynamic Gates

- The direct cascading of two stages of dynamic gates causes problematic operation because the output of each stage i.e. the input of next stage is precharged to 1.

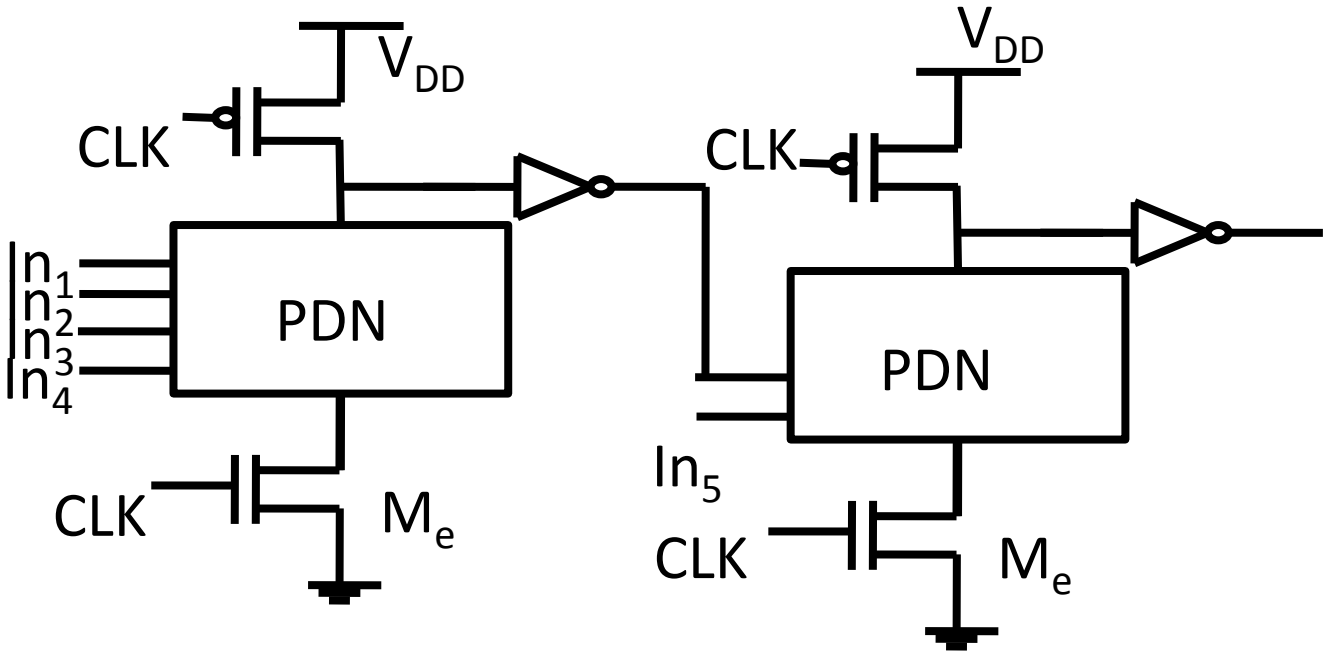




Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Domino Logic

- A domino logic module consists of an n-type dynamic logic block followed by a static inverter.

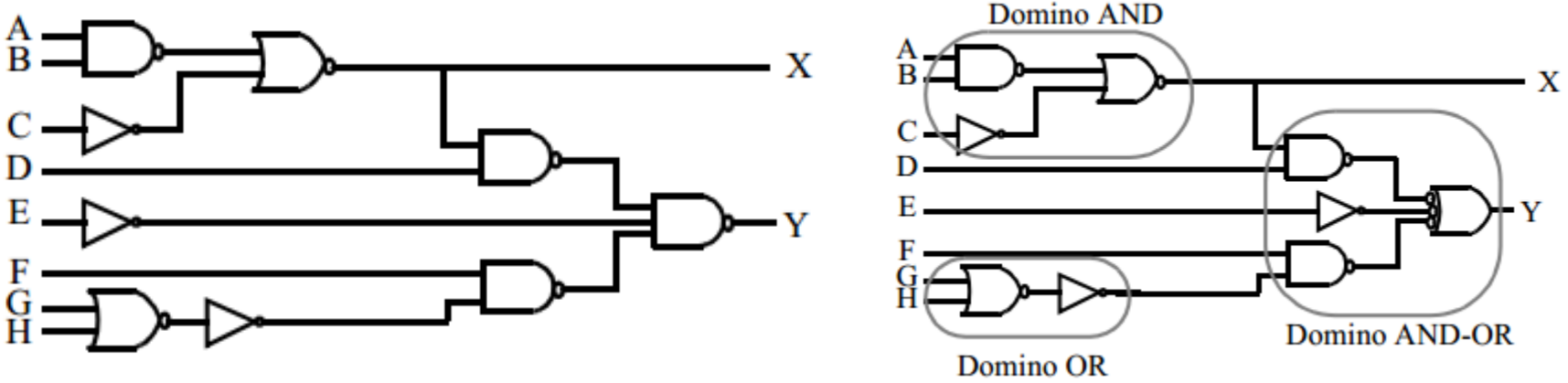


Properties of Domino Logic

- The introduction of static inverter has an advantage that the fan-out of the gate is driven by static inverter with a low impedance output, which increases noise immunity.
- Since each dynamic gate has a static inverter, only non-inverting logic can be implemented.
- Very high speeds can be achieved: only rising edge delay exists, while t_{pHL} equals zero.
- The inverter can be used to drive bleeder device to combat leakage and charge redistribution.

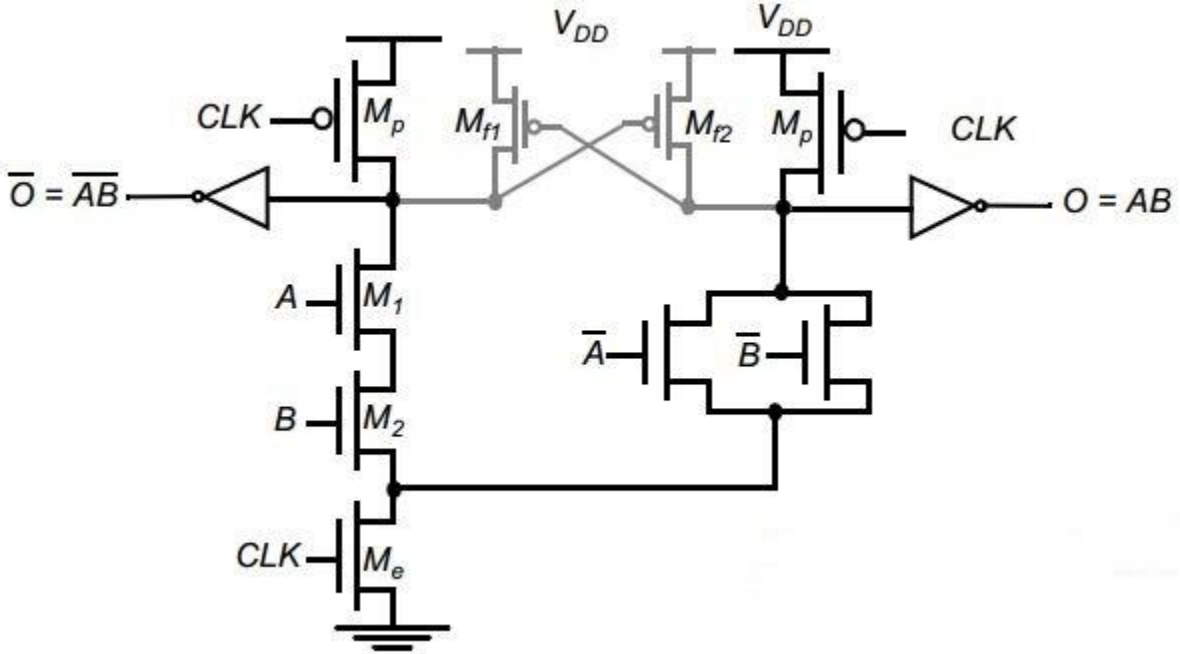
Dealing with non-inverting problem of Domino Logic

- A major limitation of domino logic is that only non-inverting logic can be implemented. The one way to deal this problem is reorganizing the logic using simple boolean transforms.



Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

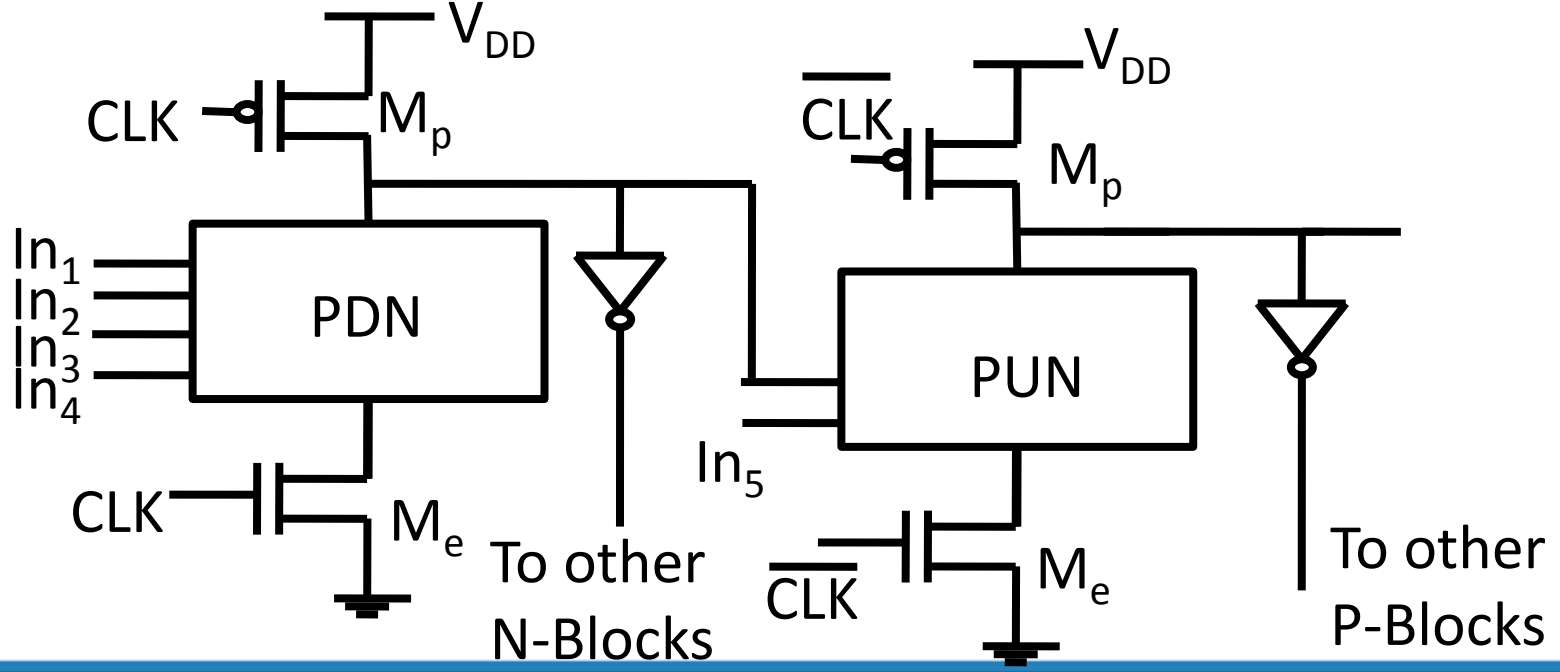
- Another (expensive) way to solve the problem is by incorporating differential logic. This is similar as DCVSL, and called as Dual-rail Domino.



Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuit,” PHI Learning Pvt. Ltd., 2011.

np-CMOS

- An alternative approach to cascade dynamic logic is np-CMOS, which consists two flavors of dynamic logic (n-tree and p-tree).



Recapitulation

- The operation of dynamic logic is divided into two major phases- precharge and evaluation.
- Charge Leakage, Charge Sharing, Capacitive Coupling and Clock Feed-through are causing signal integrity issues.
- To increase the noise immunity, the domino logic is proposed which consist a static inverter in the dynamic logic block.
- np-CMOS is an alternative approach to cascade the dynamic logic.

Thank You