IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

MICROELECTRONICS: DEVICES TO CIRCUITS

Combinational Logic Design-II

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Outline

- Power Consumption in CMOS Logic Gates
- Dynamic or Glitching Transitions
- Design Technique to reduce Switching Activity
- Ratioed Logic
- Pseudo NMOS Inverter
- How to build even better load
- Design Consideration
- Recapitulation

Power Consumption in CMOS Logic Gates

- The dynamic power dissipation is given by-

$$P=\alpha_{0\rightarrow1} C_L V_{DD}^2 f$$

Here $\alpha_{0\rightarrow1}$ is called switching activity, which is having two components-

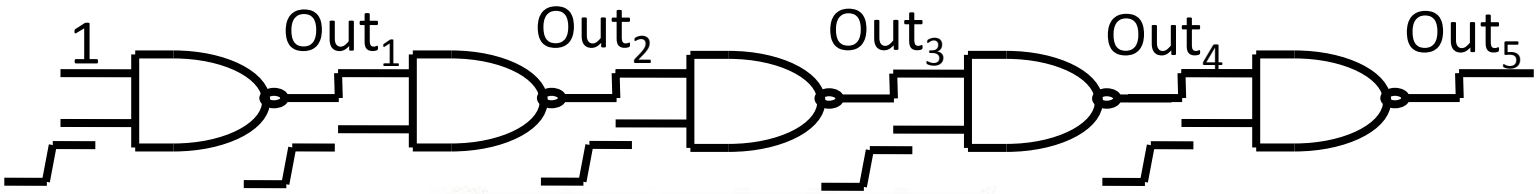
1. Static component, which is a function of network topology.
2. Dynamic component, which is a function of timing behavior of the circuit (glitches).

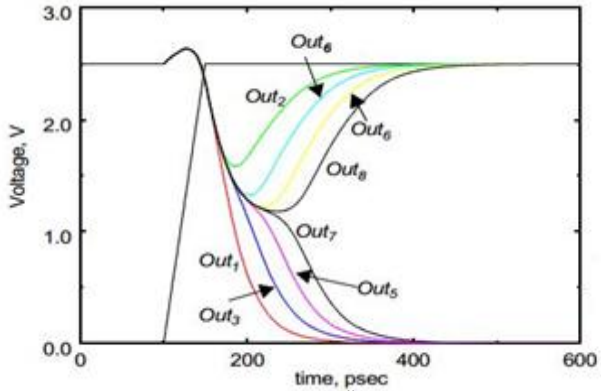
Let p_0 be the probability that the output will be in zero state in one cycle, and p_1 be the probability that the output will be one state in next cycle then-

$$\alpha_{0\rightarrow1} = p_0.p_1 = p_0(1-p_0)$$

Dynamic or Glitching Transitions

- The finite propagation delay appear from one logic block to the next can cause spurious transitions known as Glitches or Dynamic Hazards.

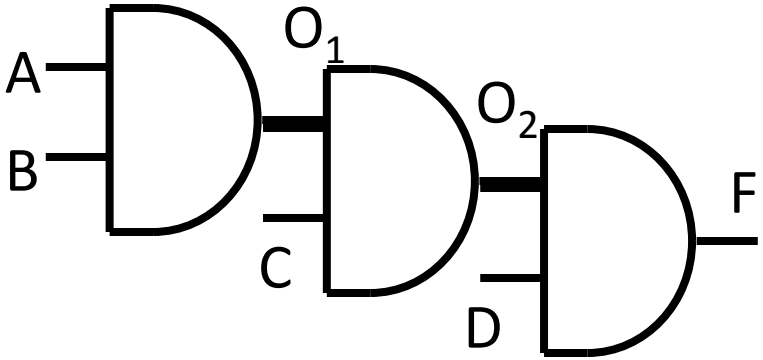




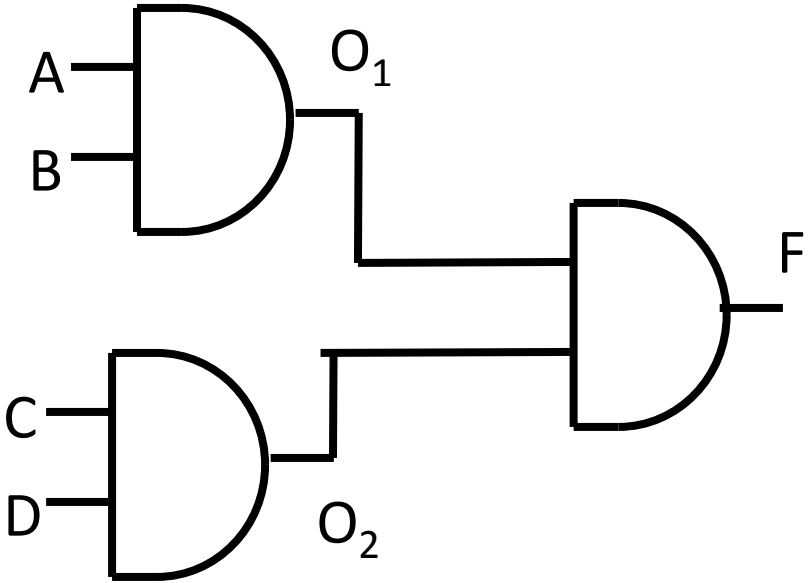
Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Design Techniques to reduce Switching Activity

1. Logic Restructuring



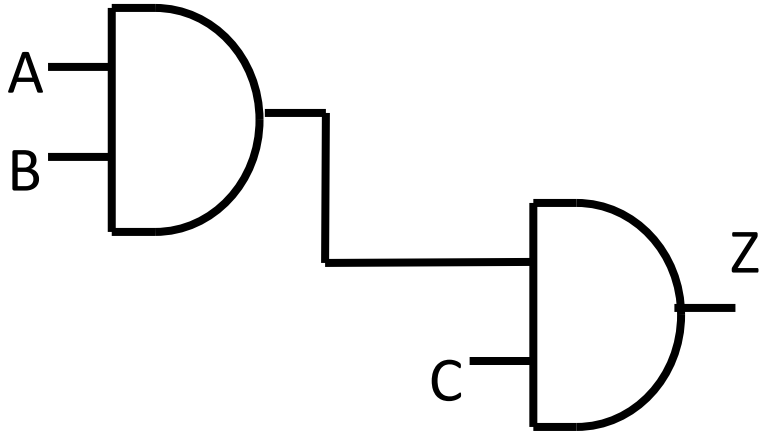
Chain Structure



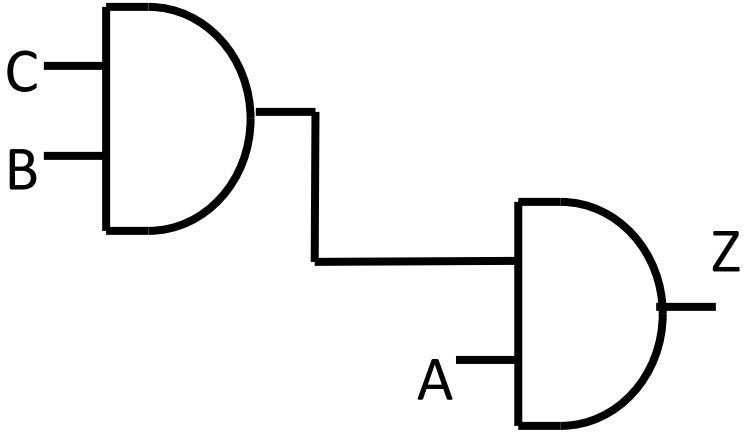
Tree Structure

2. Input Ordering

Let the probabilities that A, B and C are equal to 1 are 0.5, 0.2 and 0.1 respectively.



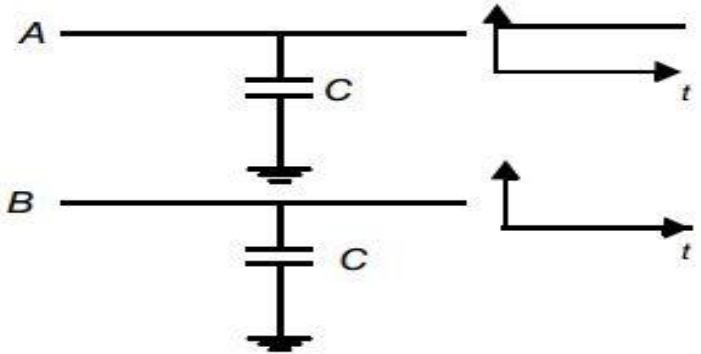
for this $\alpha_{0\to1} = 0.09$



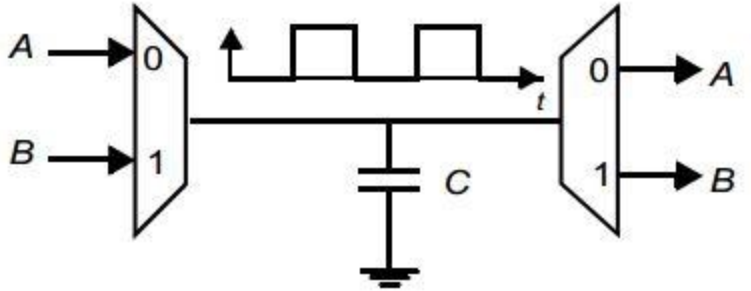
for this $\alpha_{0\to1} = 0.0196$

3. Time-multiplexing Resources

- To minimize the implementation area the time multiplexing technique is used but this does not provide lowest switching activity always.



Parallel data transmission

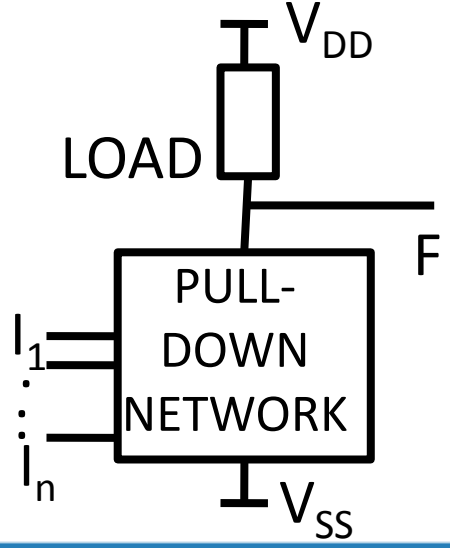


Series data transmission

Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuit,” PHI Learning Pvt. Ltd., 2011.

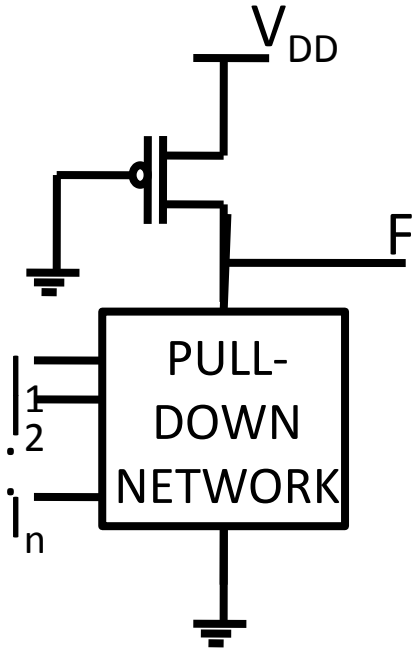
Ratioed Logic

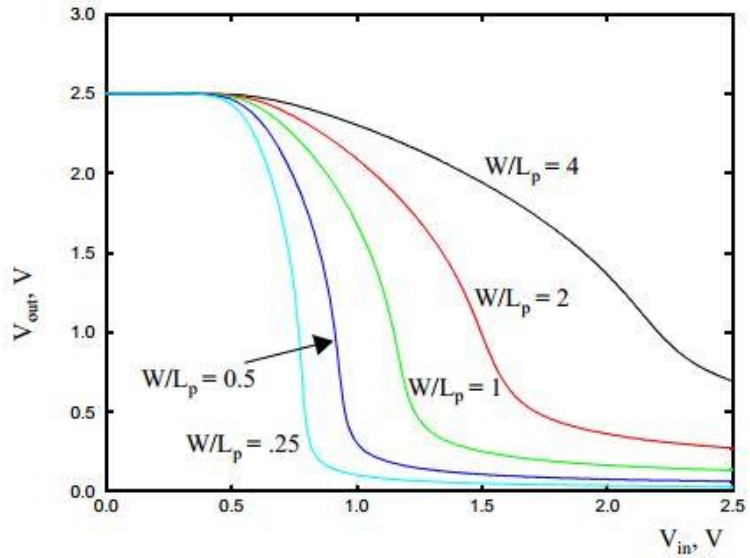
- Ratioed Logic is used to reduce the transistor count but at the cost of extra power dissipation.
- In ratioed logic the entire PUN is replaced by a single unconditional load.
- The nominal high voltage (V_{OH}) is V_{DD}, but the nominal low voltage (V_{OL}) is not zero, which results a static power dissipation.
- This also reduced the Noise-Margin.
- Since, the output voltage depends on the sizes of the transistor so it is called ratioed logic.



Pseudo NMOS Inverter

- The impact of sizing of PMOS is shown below-

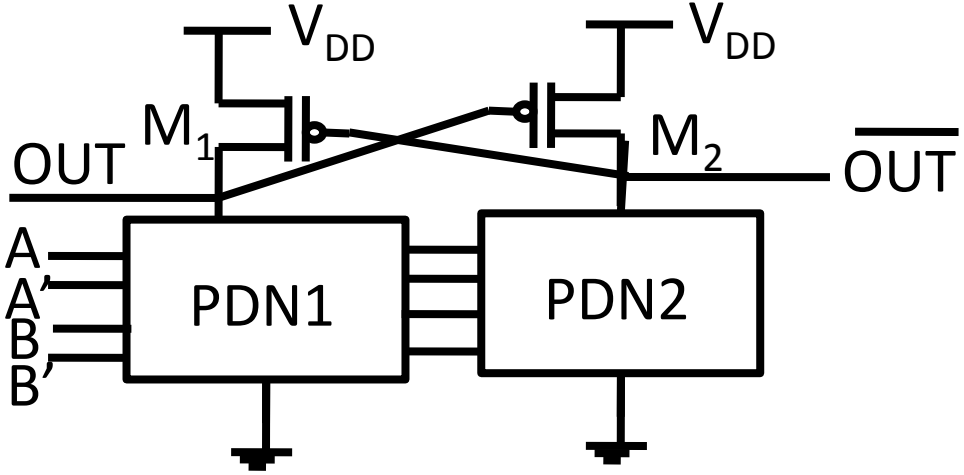




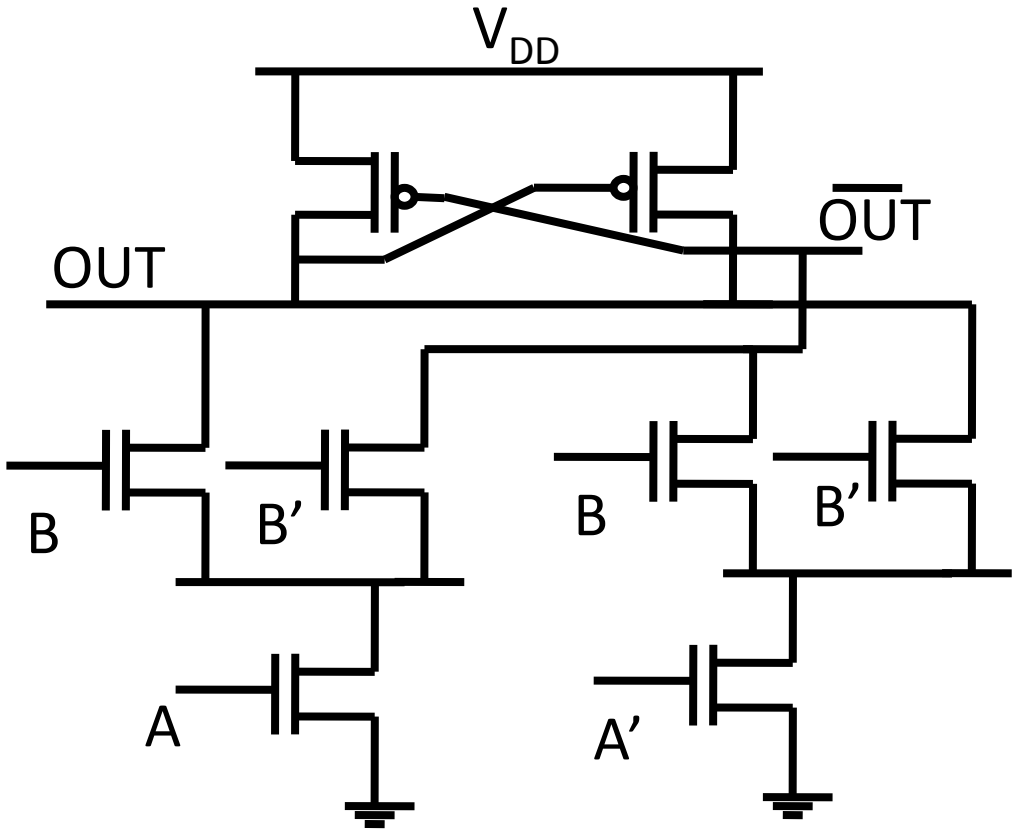
Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, “Digital Integrated Circuit,” PHI Learning Pvt. Ltd., 2011.

How to Build Even Better Load

- To completely eliminate the static power dissipation and get rail-to-rail swing, we require a new type of load.
- This type of load is called Differential Cascode Voltage Switch Logic (DCVSL) which is based on differential logic and positive feedback.

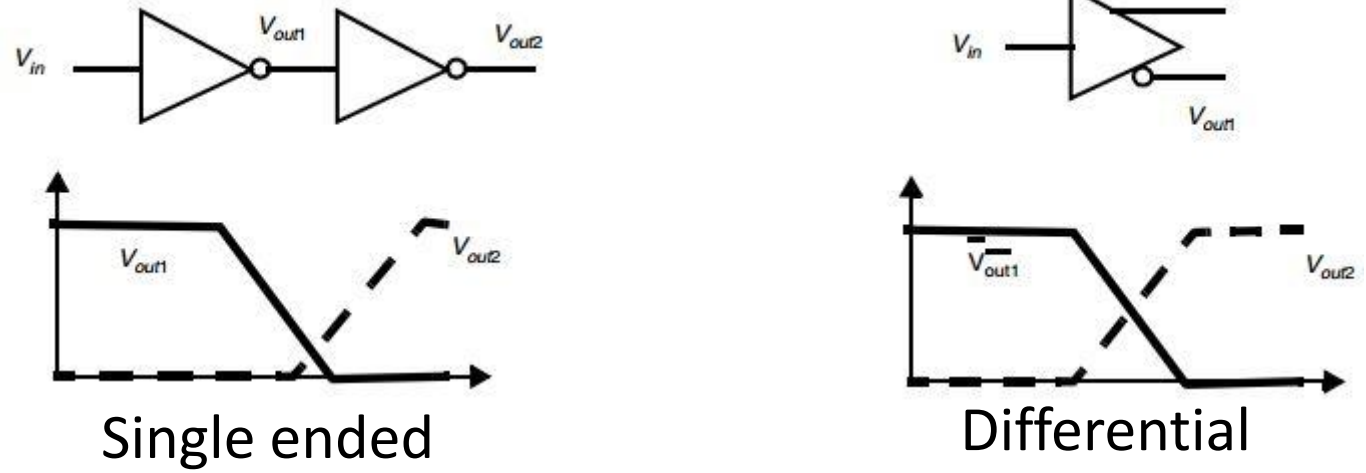


XOR-XNOR gate based DCVSL



Design Consideration

- The DCVSL provides the differential output and its complement simultaneously, which eliminate the use of an extra inverter.
- The differential implementation reduces the transistor count by factor of two.



Single ended

Differential

Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Recapitulation

- Power consumption in CMOS Logic gate is a strong function of switching activity.
- Dynamic Hazards are due to the finite propagation delay of the gates.
- Logic restructuring, Input ordering and time multiplexing are techniques to reduce the switching activity factor.
- Ratioed logic are used to minimise the transistor count but at the cost of static power dissipation.
- To reduce the static power we use DCVSL which depends on differential logic and positive feedback.

Thank You