IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

MICROELECTRONICS: DEVICES TO CIRCUITS

Combinational Logic Design-I

SUDEB DASGUPTA

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

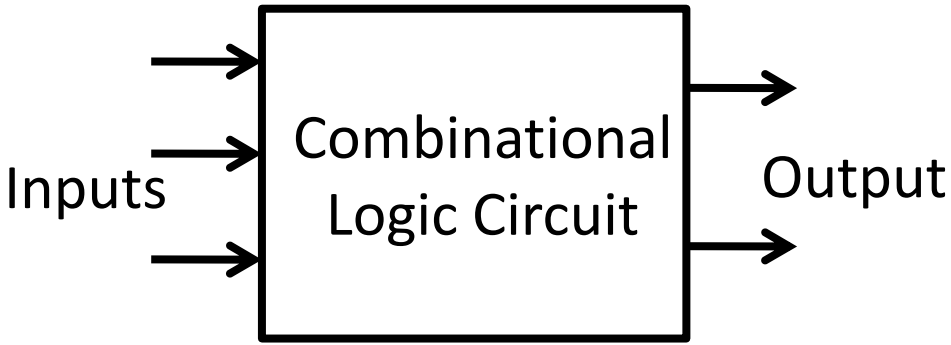


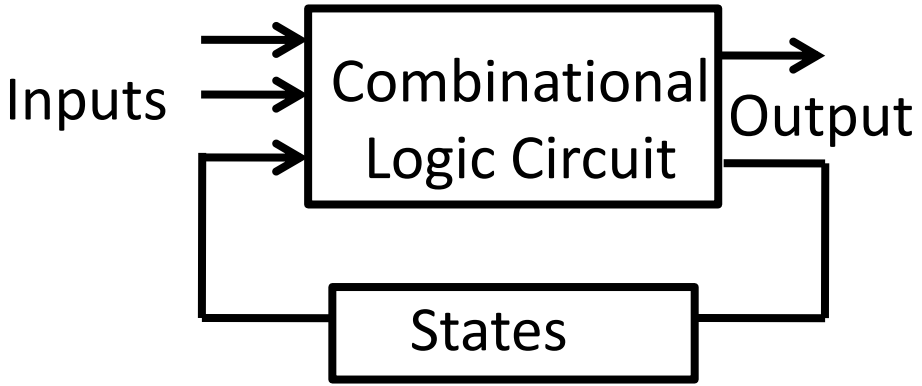
Outline

- Introduction
- Static & Dynamic Logic Design
- Choice of Pull-up and Pull-down Network
- Two Input NAND Gate
- Static Properties of Complementary CMOS Gates
- Propagation Delay of Complementary CMOS Gates
- Problems of Complementary CMOS Gates
- Design Techniques of Large Fan-in
- Recapitulation

Introduction

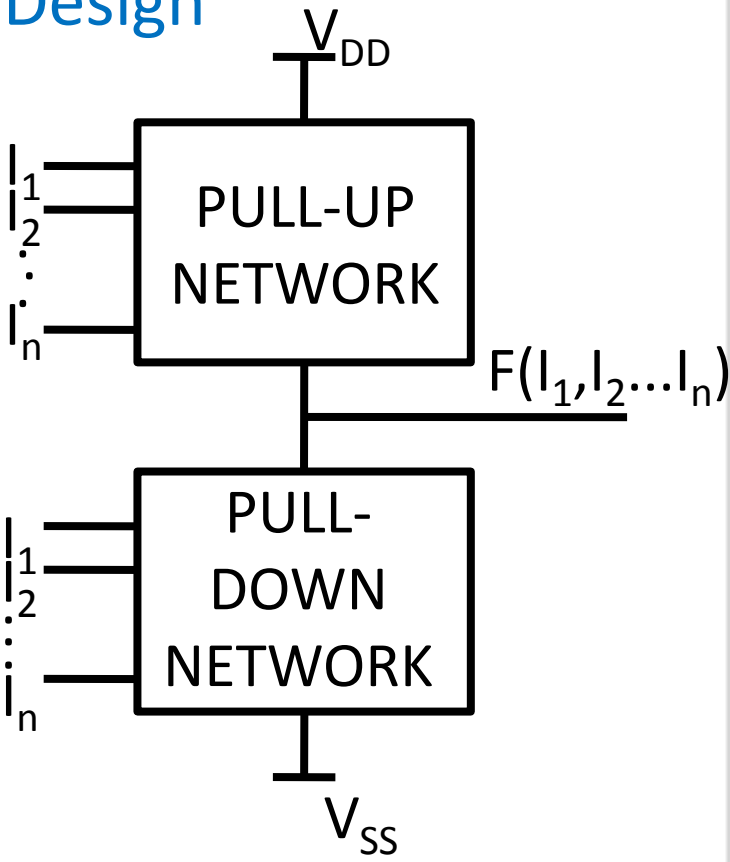
- In the combinational logic or non-regenerative circuits, the output at any instant of time depends only on the signal present at its input.
- In contrast to this if the output depends on the current input data along with the previous state of input then it is called as sequential or regenerative logic.





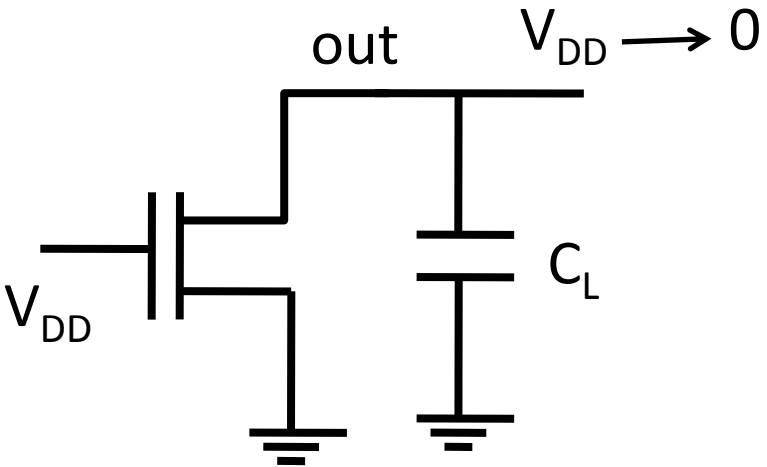
Static & Dynamic logic Design

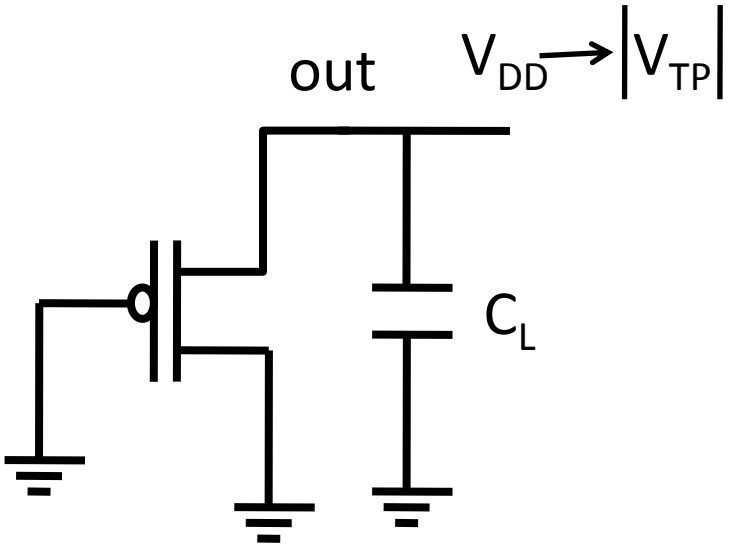
- Static Design-At every point of time, each gate output is either connected to V_{DD} or V_{SS} via a low resistance path.
- Dynamic Design-This relies on temporary storage of signal values on the capacitance of high-impedance circuit nodes.
- Complementary Logic- This is a widely used static logic, consists of pull-up (PUN) and pull-down network (PDN).



Choice of Pull Down Network

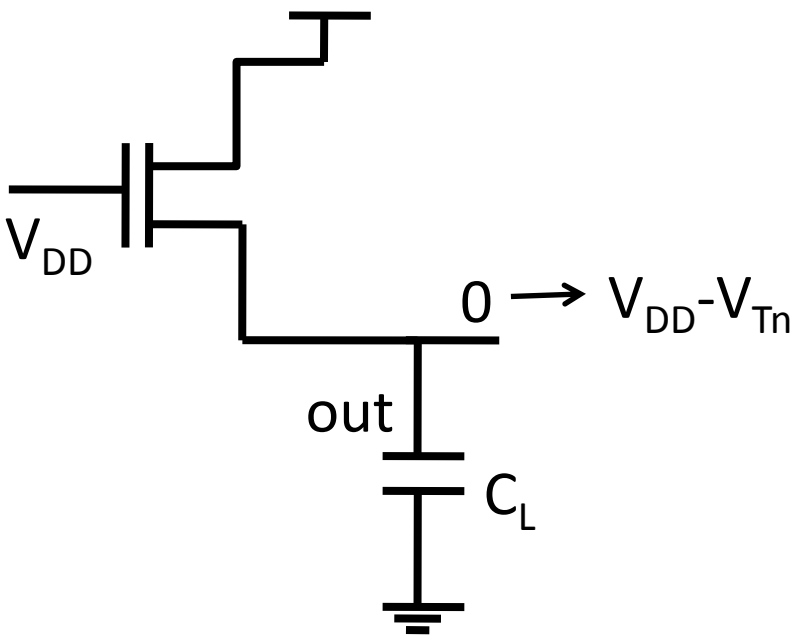
- What type of MOS is preferable for PDN?

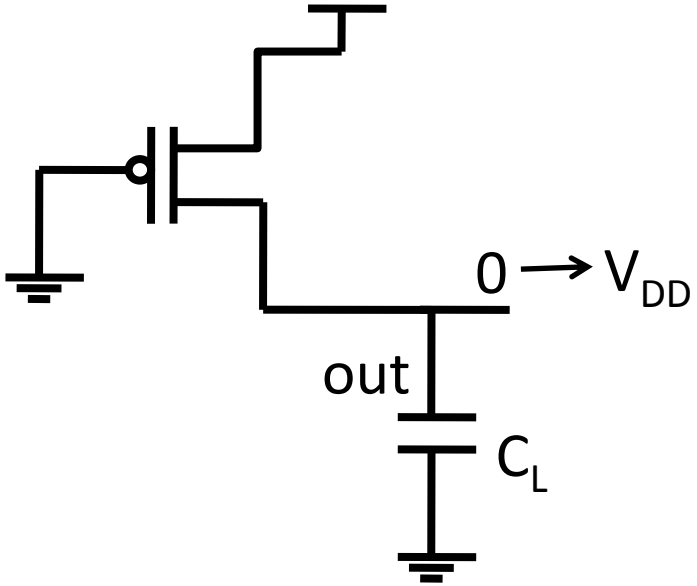




Choice of Pull UP Network

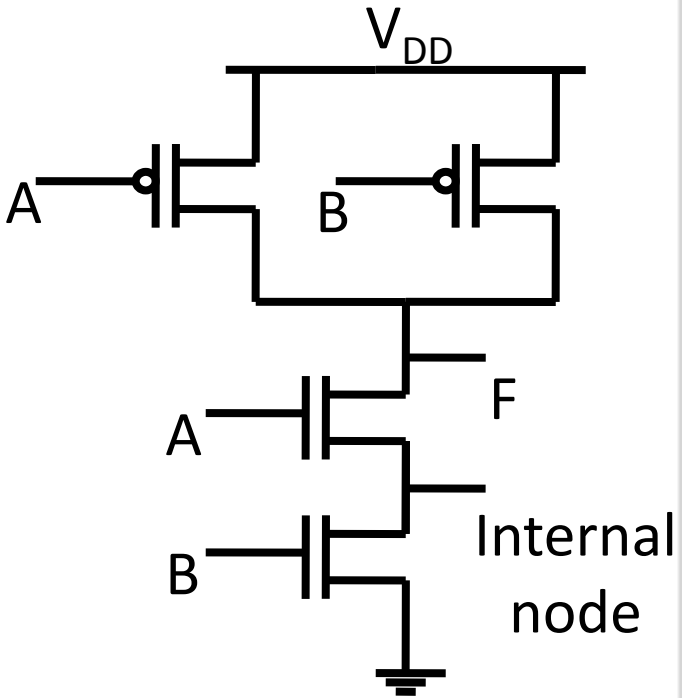
- What type of MOS is preferable for PUN?





Two-Input NAND Gate

- N-input logic implementation requires 2N gates.
- NMOS in series forms an AND logic, while in parallel they form an OR logic.
- Complementary CMOS logics are dual networks (De Morgan's Theorem).

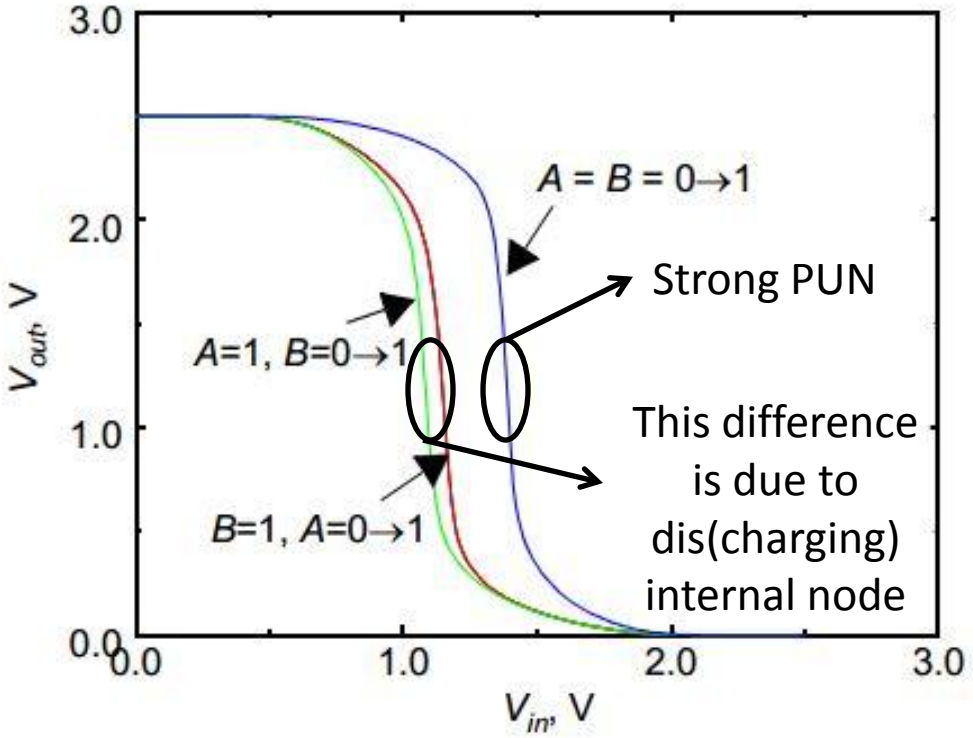


❖ Assignment-

Realize $F=\overline{D+B.(A+C)}$ using complementary CMOS design.

Static Properties of Complementary CMOS Gates

- The complementary CMOS logic gates exhibits rail-to-rail swing, with no static power dissipation. VOH = VDD; VOL = GND
- The analysis of VTC is more complicated as it depends on input pattern.



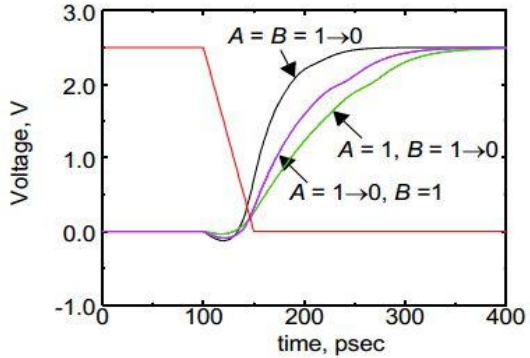
Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

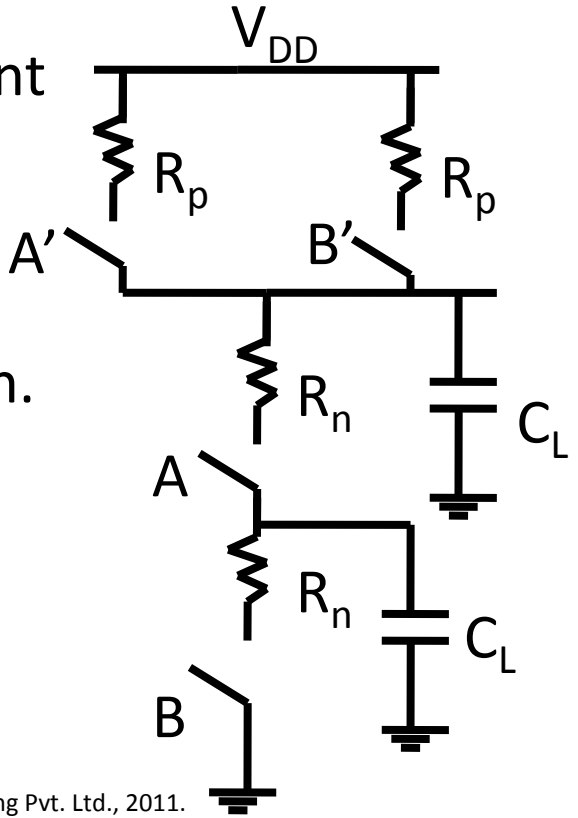
Propagation Delay of Complementary CMOS Gates

- Each transistor will replace by its equivalent resistance and capacitance.
- We calculate simple RC delay as-

$$0.69\times(R_p \text{ or } R_n)\times C_L.$$

- The propagation delay depends on input pattern.





Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Problems of Complementary CMOS Gates

1. The number of transistor required to implement an N fan-in gates is 2N.
2. The large number (2N) of transistors increases the overall capacitance of the gate.
3. Propagation delay of the gates deteriorate as a function of fan-in.
4. The series connection of the transistor in either PUN or PDN network causes an additional slowdown.
5. Therefore, the delay becomes a quadratic function of the fan-in.

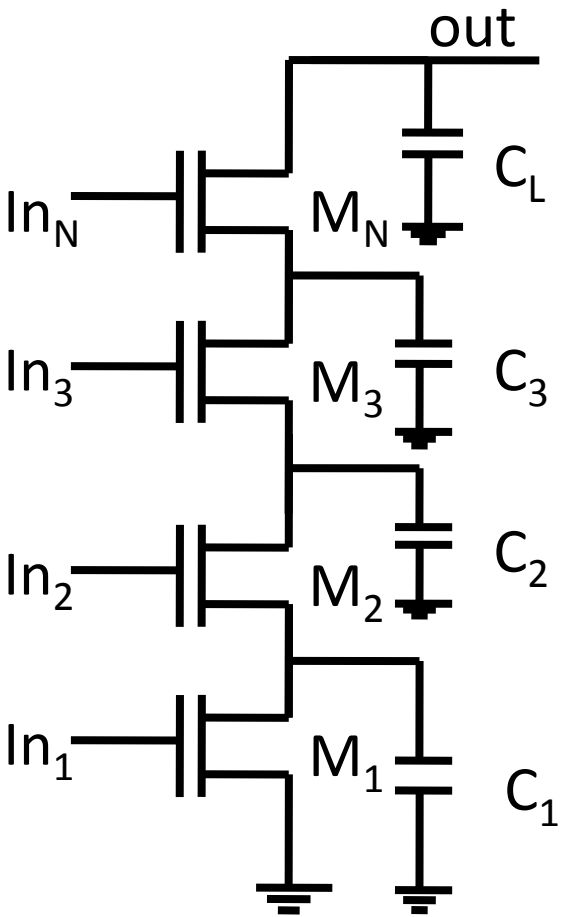
Design Techniques of Large Fan-in

1. Transistor Sizing

- To reduce the delay and resistance of the device, the designer must have to increase the sizes.
- However, increase in size increases the parasitic capacitors which adds its effects in the preceding gate.
- If the load capacitor is dominated over the intrinsic capacitor then widening the device only creates a self loading effect.
- Sizing is only effective when the load is dominated by the fan-out.

2. Progressive Transistor Sizing

- This technique reduces the dominant resistance while keeping the capacitance in bounds.
- Progressive scaling of transistor is beneficial: $M_1 > M_2 > M_3 > M_4$.
- The progressive scaling is easy in schematic diagram but it is not as simple in layout.

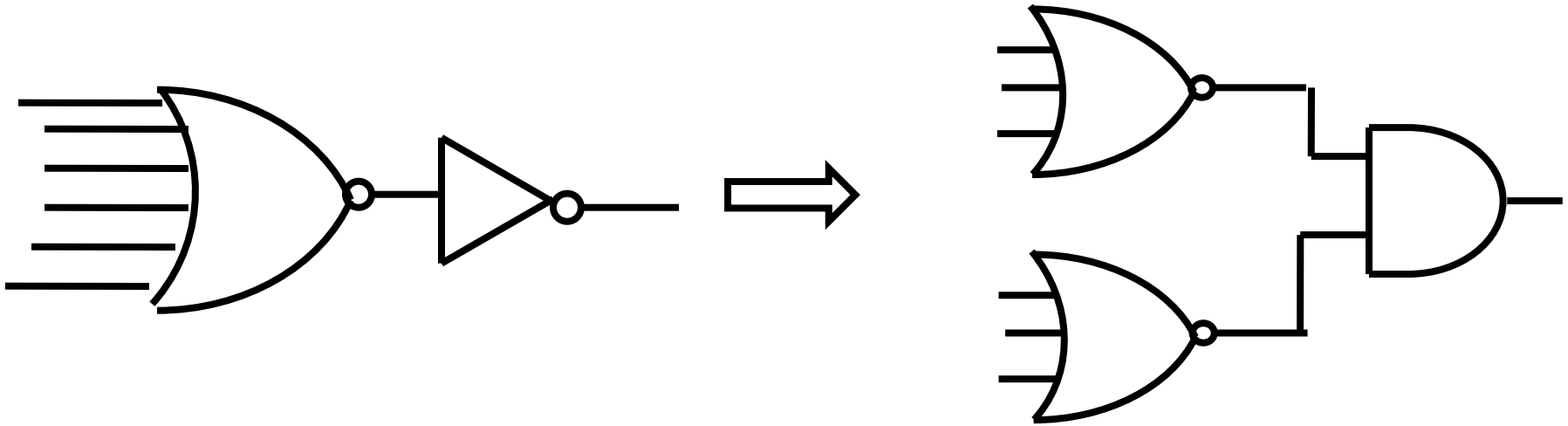


3. Input Reordering

- All the signals in the complex logic blocks might not appear at the same time due to propagation delay or preceding logic gates.
- The signal, last to all the inputs which have a stable value can be called as a critical signal an the path over which the ultimate speed of the structure can be calculated is called critical path.
- Putting the critical path transistor closer to the output gives a higher speed of operation.

4. Logic Restructuring

- Manipulating the logic equation can reduce the fan-in requirement and thus reduces the gate delay.



Recapitulation

- The most widely used logic style is static complementary CMOS.
- NMOS is a better choice for PDN and PMOS is a better choice for PUN.
- Complementary Logic is a dual in nature.
- The propagation delay of the complex network follows the Elmore Delay Rule.
- Progressive Transistor Sizing, Input Reordering and Logic Restructuring are the design technique of large fan-in.

Thank You