IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

Microelectronics: Devices to Circuits

Large Signal Operation of Op-Amp and Second Order Effects

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Outline

- Large-Signal Operation of Op Amps
- Slew-Rate
- Finite Open Loop Gain (Inverting Amplifier)
- Finite Open Loop Gain (Non-Inverting Amplifier)
- Inverting Amplifier Closed-Loop Input Resistance
- Non-Inverting Amplifier Closed-Loop Input Resistance
- Nonzero Output Resistance
- Frequency Response
- Gain Bandwidth Product
- Offset Voltage
- Offset Voltage Compensation
- Input Bias Current
- Bias Current Compensation
- Recapitulation

Large-Signal Operation of Op Amps

Output Voltage Saturation:

- op amps operate linearly over a limited range of output voltages.

Output Current Limits:

- Another limitation on the operation of op amps is that their output current is limited to a specified maximum.

Source: Microelectronics Circuits, Sedra and Smith, Fifth edition

Slew-Rate

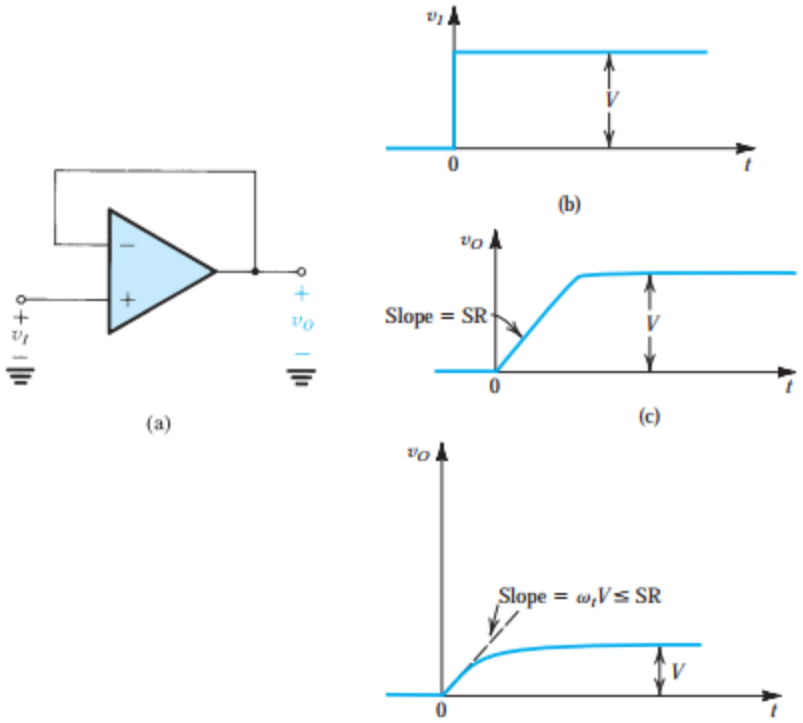
- Implicit in the frequency response analysis for the closed-loop amplifier is the assumption that the sinusoidal input signals are small.
- If a large sinusoidal signal or step function is applied to an op-amp circuit, the input stage can be overdriven and the small-signal model will no longer apply.
- Nonlinear distortion when large output signals are present is slew-rate limiting.
- Maximum rate of change possible at the output of a real op amp, this maximum is known as the slew rate (SR) of the op amp.

Source: Microelectronics Circuits, Sedra and Smith, Fifth edition

$$SR = \left| \frac{d v_0}{dt} \right|_{\max}$$

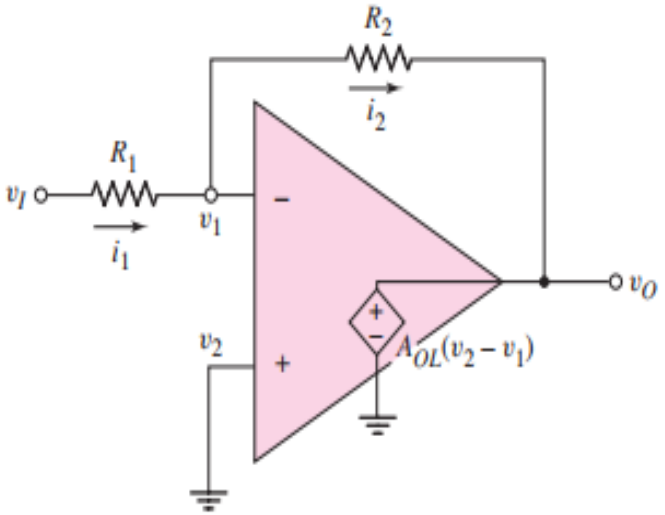
$$\frac{V_0}{V_t} = \frac{1}{1 + \frac{S}{w_t}}$$

$$v_0(t) = V\left(1 - e^{-w_t t}\right)$$



Source: Microelectronics Circuits, Sedra and Smith, Fifth edition

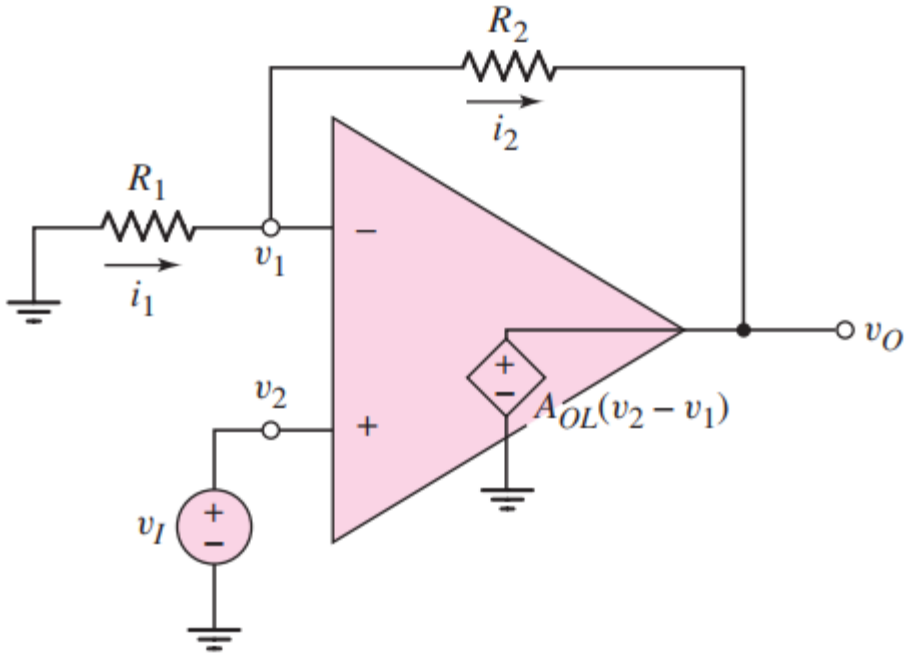
Finite Open Loop Gain (Inverting Amplifier)



$$A_{CL} = \frac{v_o}{v_I} = \frac{-\frac{R_2}{R_1}}{1 + \frac{1}{A_{OL}}\left(1 + \frac{R_2}{R_1}\right)}$$

Source: Microelectronics Circuit Analysis and Design Donald A. Neamen, Fourth edition

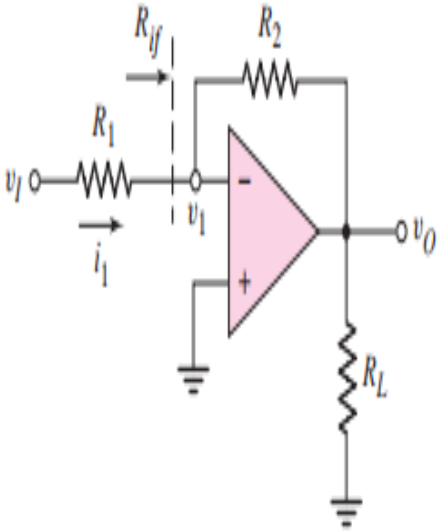
Finite Open Loop Gain (Non-Inverting Amplifier)

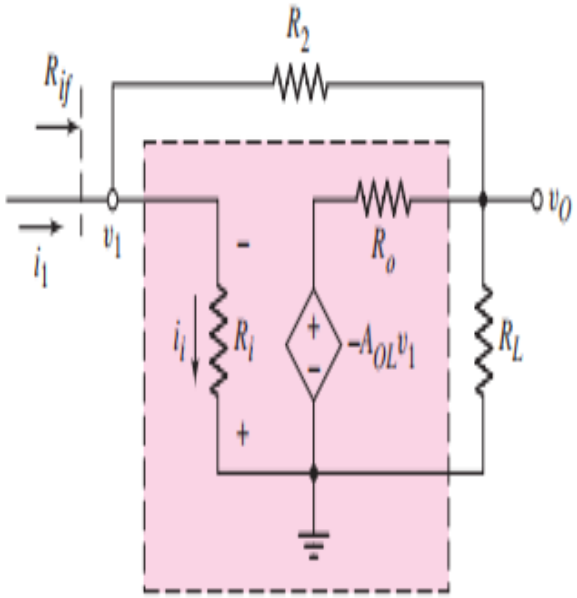


$$A_{CL} = \frac{v_o}{v_I} = \frac{1 + \frac{R_2}{R_1}}{1 + \frac{1}{A_{OL}}\left(1 + \frac{R_2}{R_1}\right)}$$

Source: Microelectronics Circuit Analysis and Design Donald A. Neamen, Fourth edition

Inverting Amplifier Closed-Loop Input Resistance

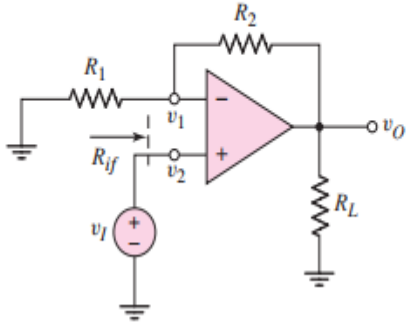


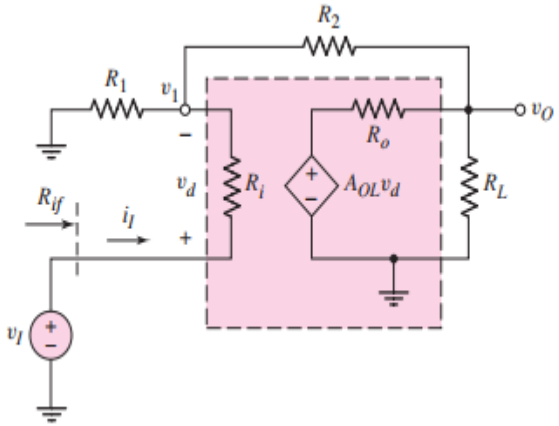


$$\frac{i_1}{v_1} = \frac{1}{R_{if}} = \frac{1}{R_i} + \frac{1}{R_2}\frac{1 + A_{OL} + \frac{R_o}{R_L}}{1 + \frac{R_o}{R_L} + \frac{R_o}{R_2}}$$

Source: Microelectronics Circuit Analysis and Design Donald A. Neamen, Fourth edition

Non-Inverting Amplifier Closed-Loop Input Resistance



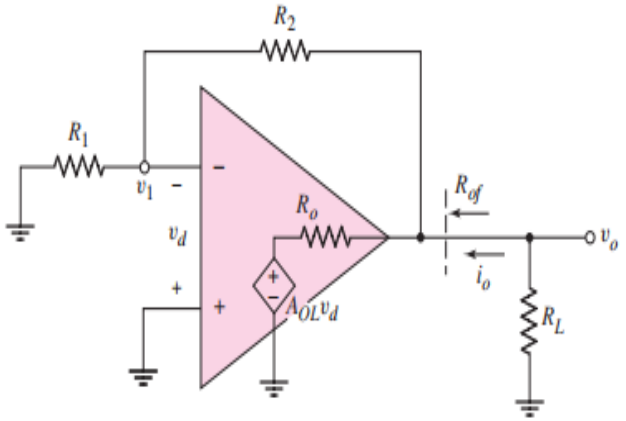


$$R_{if} = \frac{v_I}{v_I} = \frac{R_i\left(1 + A_{OL}\right) + R_2\left(1 + \frac{R_i}{R_2}\right)}{1 + \frac{R_2}{R_1}}$$

Source: Microelectronics Circuit Analysis and Design Donald A. Neamen, Fourth edition

Nonzero Output Resistance

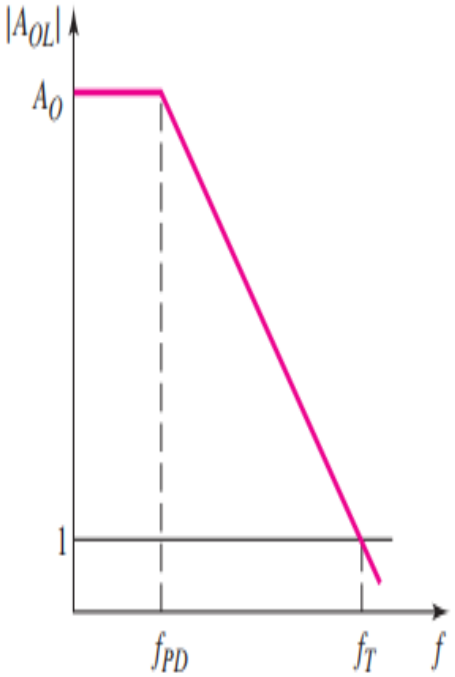
- The ideal op-amp has a zero output resistance, the output voltage is independent of the load impedance. The op-amp acts as an ideal voltage source and there is no loading effect.
- An actual op-amp circuit has a nonzero output resistance, which means that the output voltage, and therefore the closed-loop gain, is a function of the load impedance.

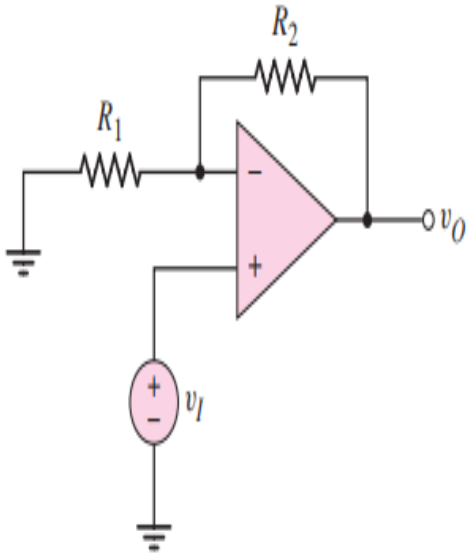


$$\frac{1}{R_{of}} = \frac{1}{R_o}\left[\frac{A_{OL}}{1+\frac{R_2}{R_1}}\right]$$

Source: Microelectronics Circuit Analysis and Design Donald A. Neamen, Fourth edition

Frequency Response





$$A_{OL}(f) = \frac{A_o}{1 + j\dfrac{f}{f_{PD}}}$$

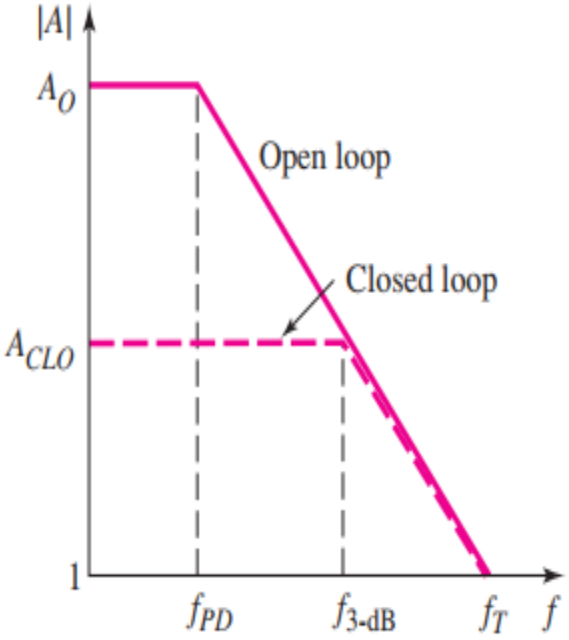
$$f_T = f_{PD} A_o$$

$$A_{CL} = \frac{A_{OL}}{1 + \beta A_{OL}}$$

$$f_{3dB} = f_{PD}\left(\frac{A_o}{A_{CLO}}\right)$$

Source: Microelectronics Circuit Analysis and Design Donald A. Neamen, Fourth edition

Gain Bandwidth Product

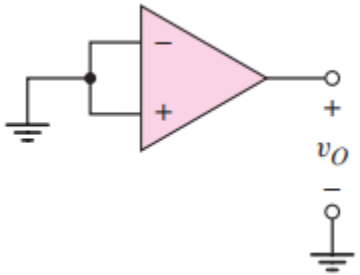


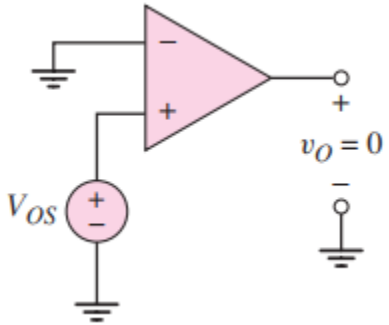
$$\left|A_{CL}\left(f = f_{unity}\right)\right| = 1 = \frac{A_{CLO}}{\sqrt{1+\left[\frac{f_{unity}}{f_{PD}\left(A_O / A_{CLO}\right)}\right]^2}}$$

$$f_{unity} = f_T$$

Source: Microelectronics Circuit Analysis and Design Donald A. Neamen, Fourth edition

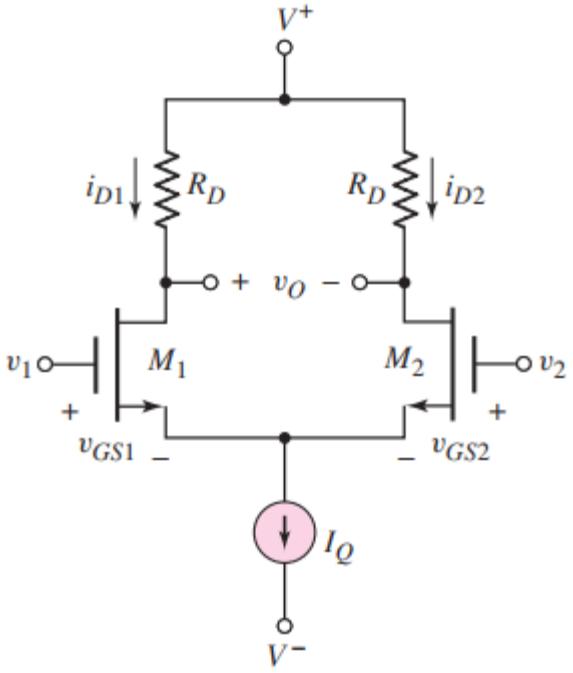
Offset Voltage





- The output dc offset voltage is the measured open-loop output voltage when the input voltage is zero.
- The input dc offset voltage is defined as the input differential voltage that must be applied to the open-loop op-amp to produce a zero output voltage.

Source: Microelectronics Circuit Analysis and Design Donald A. Neamen, Fourth edition



$$v_{OS} = v_{GS1} - v_{GS2}$$

$$v_{OS} = \sqrt{\frac{i_{D1}}{K_{n1}}} + V_{TN1} - \left(\sqrt{\frac{i_{D2}}{K_{n2}}} + V_{TN2}\right)$$

$$i_{D1} = i_{D2} = \frac{I_Q}{2}$$

$$i_{D1} = K_{n1}\left(v_{GS1} - V_{TN1}\right)^2$$

$$v_o = 0$$

$$i_{D2} = K_{n2}\left(v_{GS2} - V_{TN2}\right)^2$$

$$V_{OS} = -\frac{1}{2}\sqrt{\frac{I_Q}{2K_n}}\left(\frac{\Delta K_n}{K_n}\right)$$

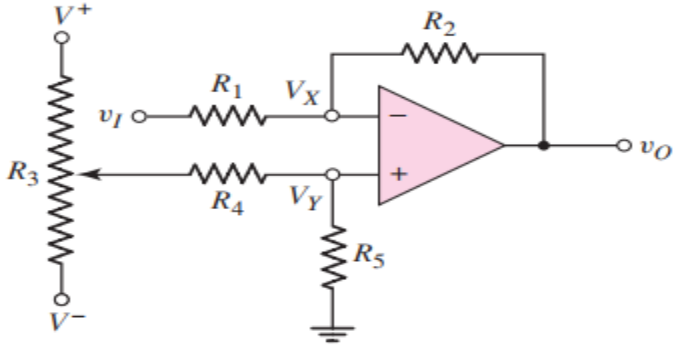
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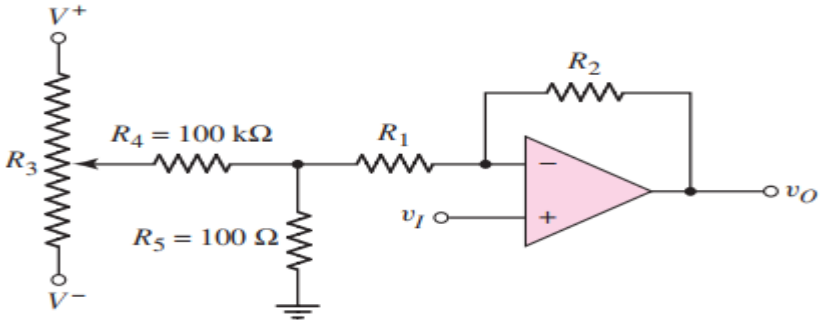
Offset Voltage Compensation

Two Methods:

a) An externally connected offset compensation network.

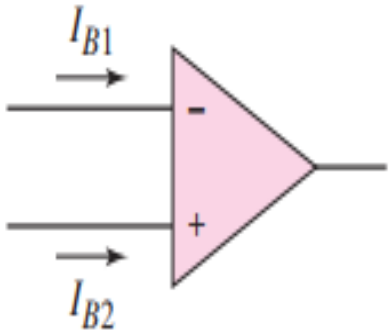
b) An operational amplifier with offset-null terminals.

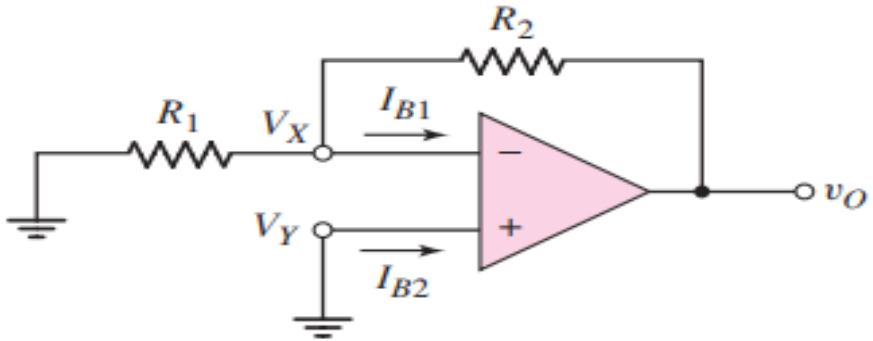




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Input Bias Current





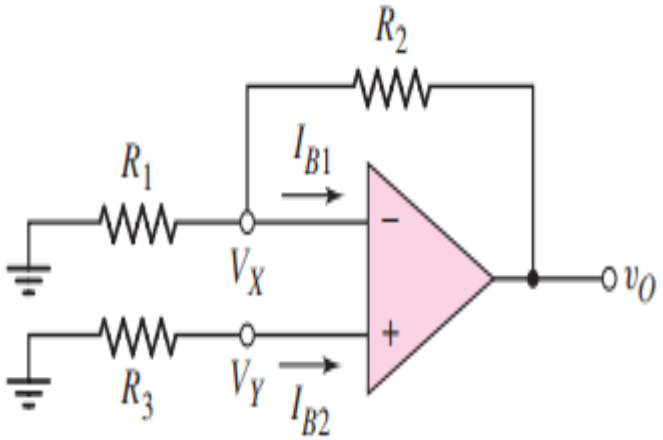
$$I_B = \frac{I_{B1} + I_{B2}}{2} \qquad I_{OS} = |I_{B1} - I_{B2}|$$

- If the input stage is symmetrical, with all corresponding elements matched, then IB1 = IB2.

Source: Microelectronics Circuit Analysis and Design Donald A. Neamen, Fourth edition

Bias Current Compensation

- The effect of bias currents in op-amp circuits can be minimized with a simple compensation technique.



Source: Microelectronics Circuit Analysis and Design Donald A. Neamen, Fourth edition

Recapitulation

- Op-amp slewing can result in nonlinear distortion of output signal waveforms.
- Capacitive coupling, an op amp reduces the dc offset voltage at the output considerably.
- The effect of V_{OS} on performance can be evaluated by including in the analysis a dc source V_{OS} in series with the op-amp positive input lead.
- The input offset voltage, V_{OS} , is the magnitude of dc voltage that when applied between the op amp input terminals, with appropriate polarity, reduces the dc offset voltage at the output to zero.

Thank You