IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

Microelectronics: Devices to Circuits

Multistage Amplifier with SPICE Simulation

SUDEB DASGUPTA

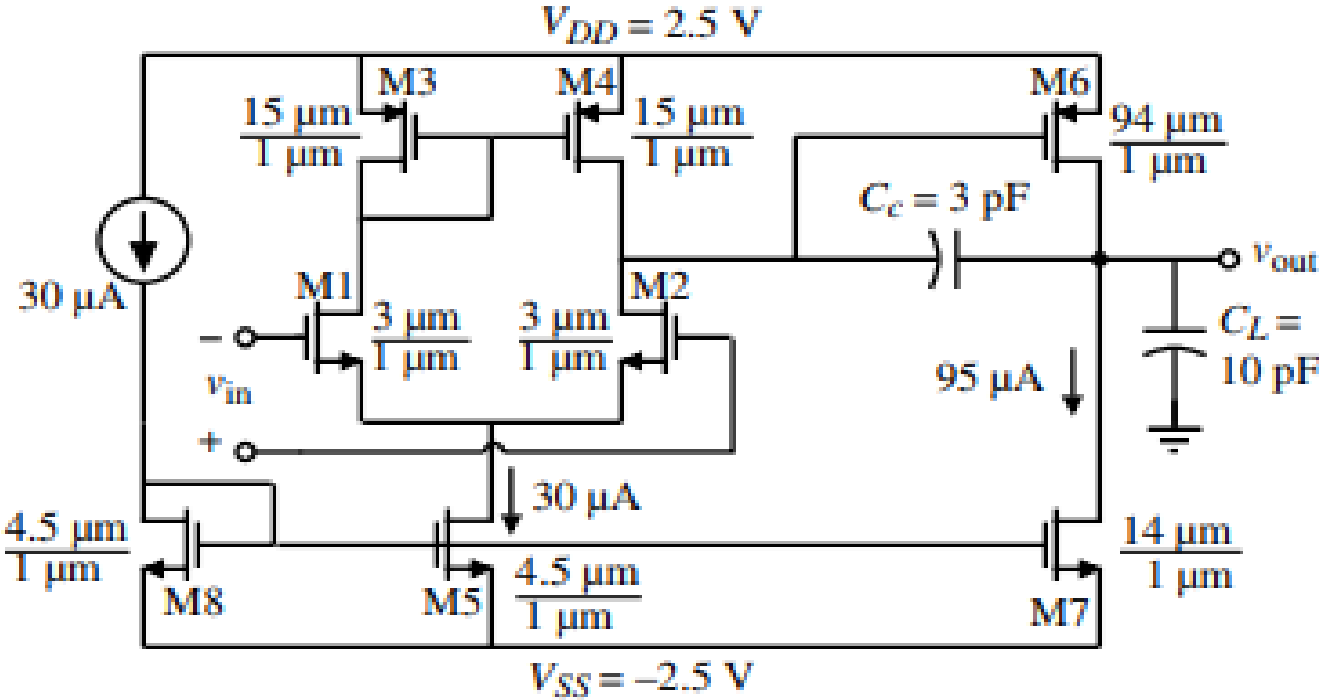
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



Outline

- CMOS Operational Amplifiers
- Spice Code of CMOS Op-amp
- Spice code for open loop gain
- Spice code for unity gain configuration
- Recapitulation

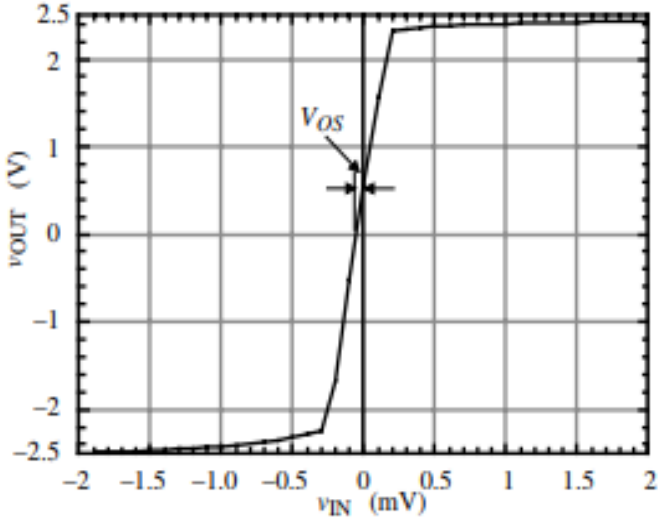
CMOS Operational Amplifiers



Source: CMOS Analog Circuit Design,Phillin E. Allen, Holberg, Second edition

Spice Code of CMOS Op-amp

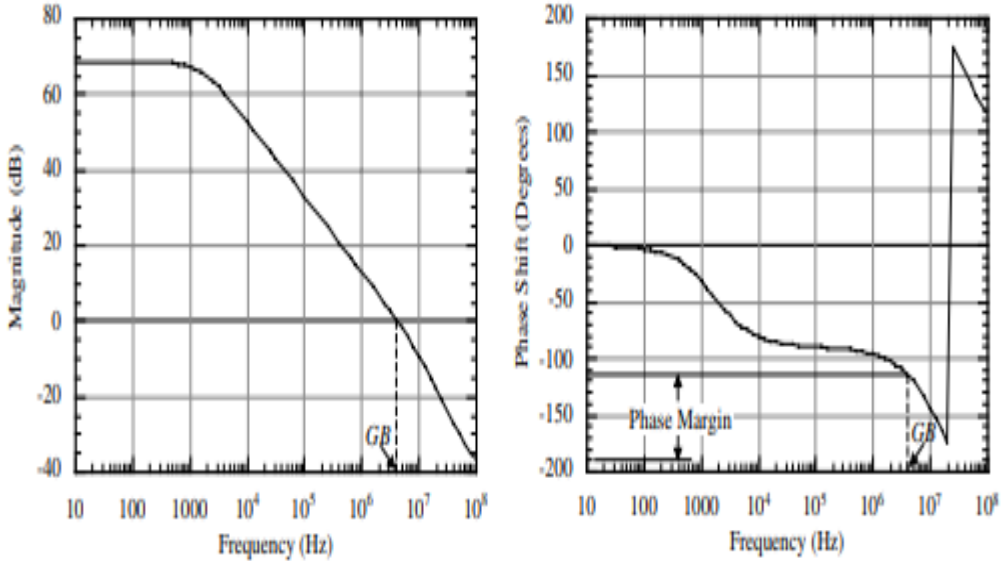
```
.SUBCKT OPAMP 1 2 6 8 9
M1 4 2 3 3 NMOS1 W = 3U L = 1U AD = 18P AS = 18P PD = 18U PS =
+ 18U
M2 5 1 3 3 NMOS1 W = 3U L = 1U AD = 18P AS = 18P PD = 18U PS =
+ 18U
M3 4 4 8 8 PMOS1 W = 15U L = 1U AD = 90P AS = 90P PD = 42U PS = 42U
M4 5 4 8 8 PMOS1 W = 15U L = 1U AD = 90P AS = 90P PD = 42U PS = 42U
M5 3 7 9 9 NMOS1 W = 4.5U L = 1U AD = 27P AS = 27P PD = 21U PS = 21U
M6 6 5 8 8 PMOS1 W = 94U L = 1U AD = 564P AS = 564P PD = 200U PS = 200U
M7 6 7 9 9 NMOS1 W = 14U L = 1U AD = 84P AS = 84P PD = 40U PS = 40U
M8 7 7 9 9 NMOS1 W = 4.5U L = 1U AD = 27P AS = 27P PD = 21U PS = 21U
CC 5 6 3.0P
.MODEL NMOS1 NMOS VTO = 0.70 KP = 110U GAMMA = 0.4 LAMBDA = 0.04 PHI =
+ 0.7 MJ = 0.5 MJSW = 0.38 CGBO = 700P CGSO = 220P CGDO = 220P CJ
+ = 770U CJSW = 380P LD = 0.016U TOX = 14N
.MODEL PMOS1 PMOS VTO = -0.7 KP = 50U GAMMA = 0.57 LAMBDA = 0.05 PHI
+ = 0.8 MJ = 0.5 MJSW = .35 CGBO = 700P CGSO = 220P CGDO = 220P CJ
+ = 560U CJSW = 350P LD = 0.014U TOX = 14N
IBIAS 8 7 30U
.ENDS
```



Source: CMOS Analog Circuit Design,Phillin E. Allen, Holberg, Second edition

Spice code for open loop gain

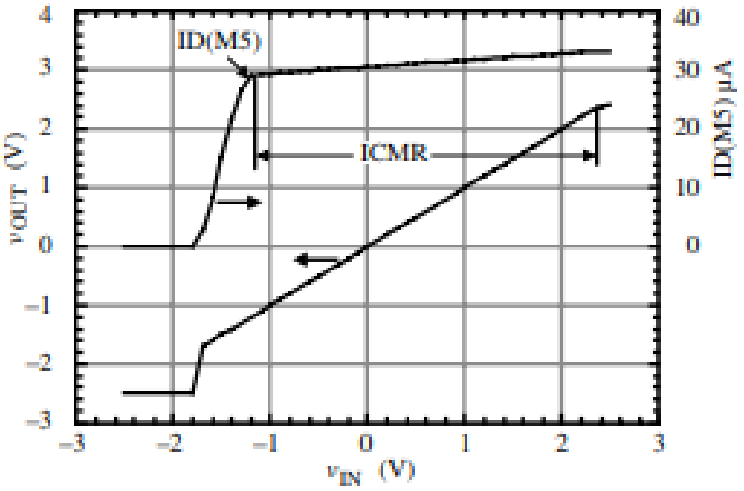
```
.OPTION LIMPTS = 1000
VIN+ 1 0 DC 0 AC 1.0
VDD 4 0 DC 2.5
VSS 0 5 DC 2.5
VIN - 2 0 DC 0
CL 3 0 10P
X1 1 2 3 4 5 OPAMP
        .
        .
        .
(Subcircuit of Table 6.6-1)
        .
        .
        .
.OP
.TF V(3) VIN+
.DC VIN+ -0.005 0.005 100U
.PRINT DC V(3)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE (This entry is unique to PSPICE)
.END
```



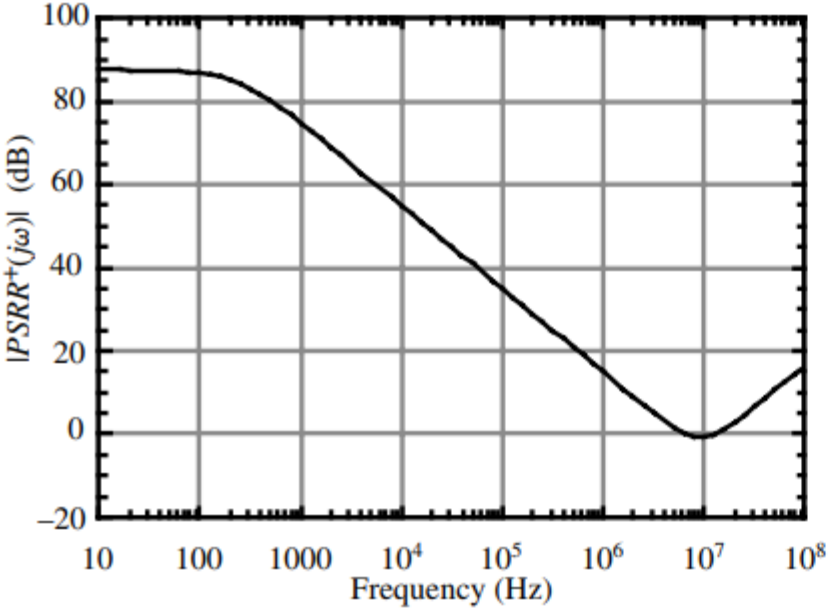
Source: CMOS Analog Circuit Design,Phillin E. Allen, Holberg, Second edition

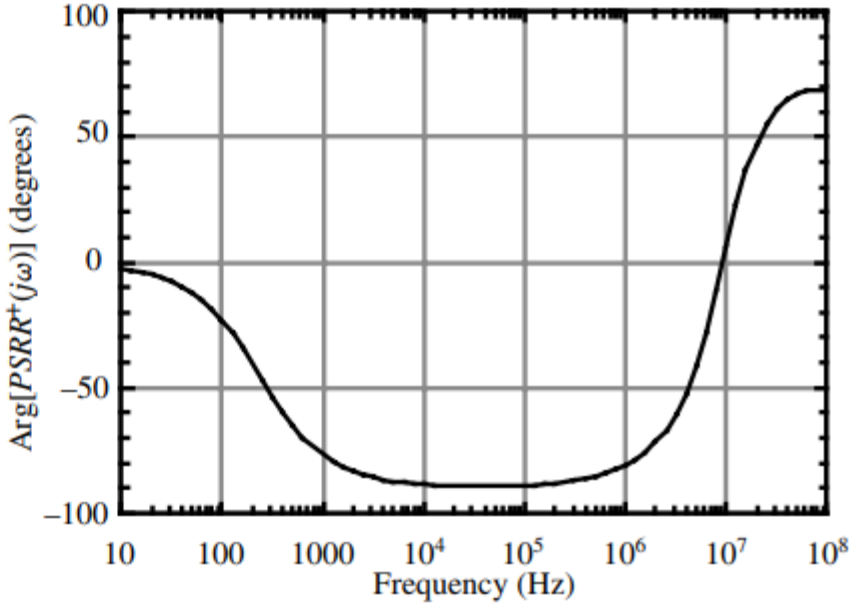
Spice code for unity gain configuration

```
.OPTION LIMPTS = 501
VIN+ 1 0 PWL(0 -2 10N -2 20N 2 2U 2 2.01U -2 4U -2
+ 4.01U -.1 6U -.1 6.01U .1 8U .1 8.01U -.1 10U -.1)
VDD 4 0 DC 2.5 AC 1.0
VSS 0 5 DC 2.5
CL 3 0 20P
X1 1 3 3 4 5 OPAMP
  .
  .
  .
(Subcircuit of Table 6.6-1)
  .
  .
  .
.DC VIN+ -2.5 2.5 0.1
.PRINT DC V(3)
.TRAN 0.05U 10U 0 10N
.PRINT TRAN V(3) V(1)
.AC DEC 10 1 10MEG
.PRINT AC VDB(3) VP(3)
.PROBE (This entry is unique to PSPICE)
.END
```

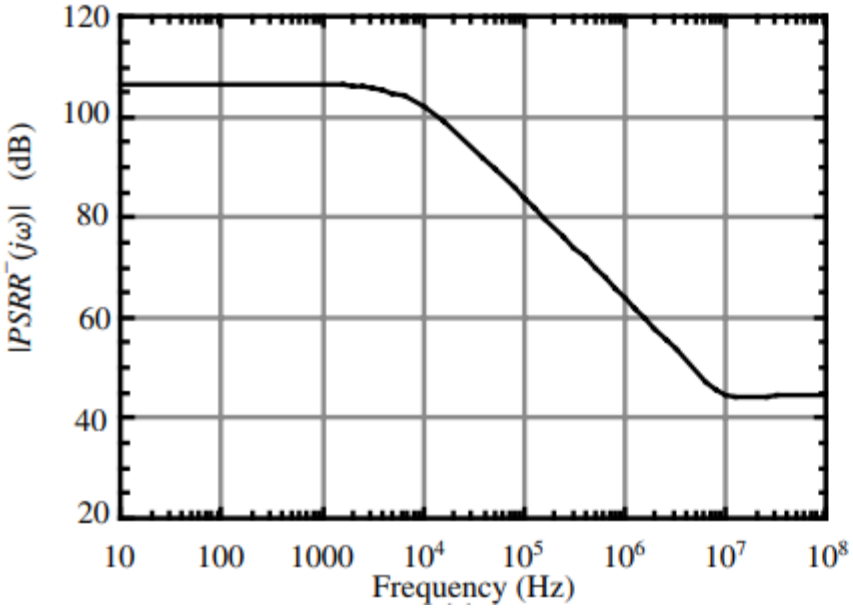


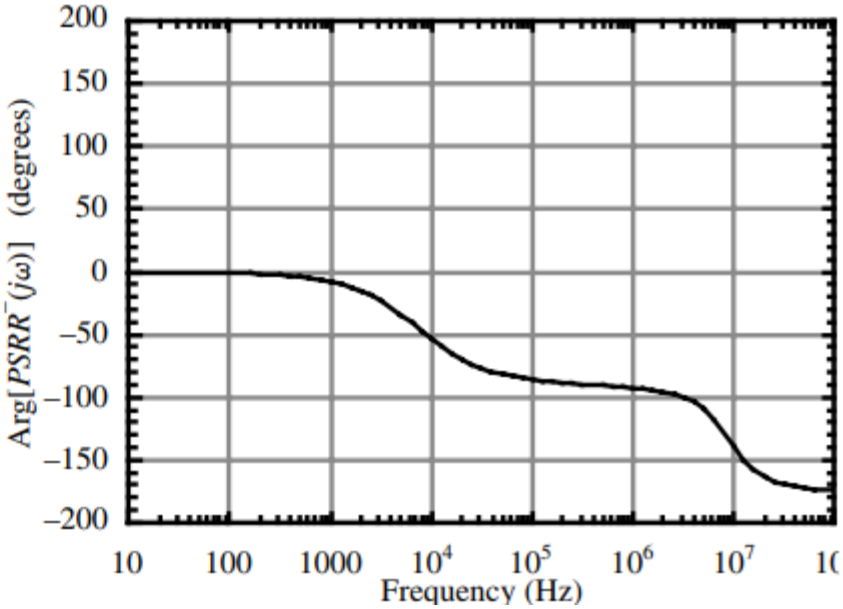
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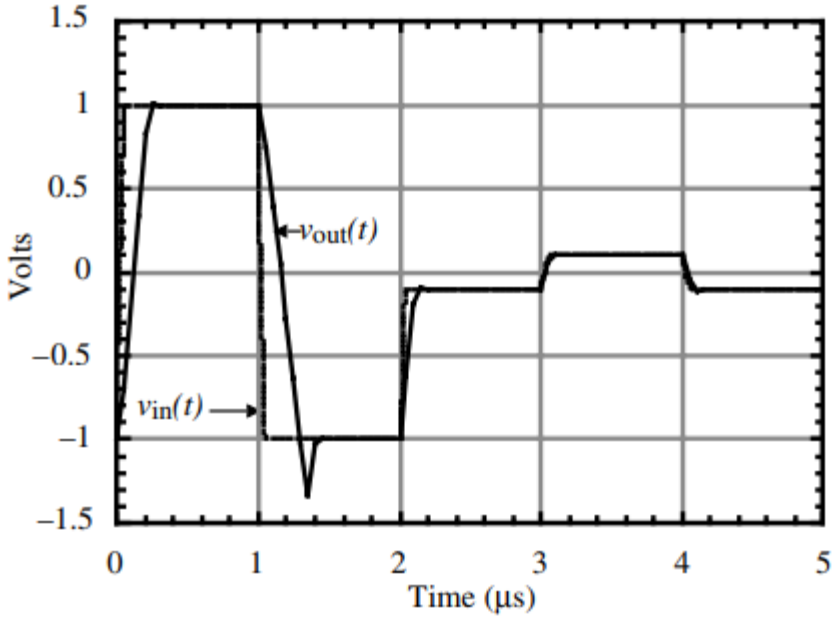


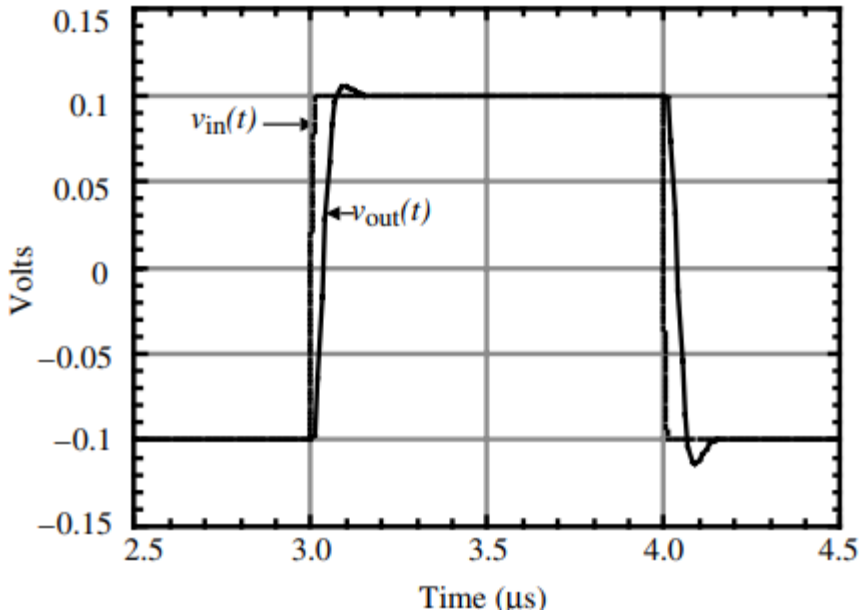
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Recapitulation

Specification (Power supply = ±2.5 V)	Design (Example 6.3-1)	Simulation (Example 6.6-1)
Open-loop gain	>5000	10,000
GB (MHz)	5 MHz	5 MHz
ICMR (volts)	−1 to 2 V	+2.4 V, −1.2 V
Slew rate (V/μs)	>10 (V/μs)	+10, −7 (V/μs)
P_{diss} (mW)	<2 mW	0.625 mW
V_{out} range (V)	±2 V	+2.3 V, −2.2 V
$PSRR^+$ (0) (dB)	—	87
$PSRR^-$ (0) (dB)	—	106
Phase margin (degrees)	60°	65°
Output resistance (kΩ)	—	122.5 kΩ

Source: CMOS Analog Circuit Design,Phillin E. Allen, Holberg, Second edition

Thank You