IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

MICROELECTRONICS: DEVICES TO CIRCUITS

Fabrication Process -II

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



Outline

- Design rule check
- Scalable design rules
- Micron-rules process
- Circuit under test
- Packaging ICs
- Cleanroom environment
- Productivity trends

Design Rules

- Act as an interface between the circuit designer and the process engineer to satisfy both in achieving –
  - High circuit density/performance.
  - Tighter/ smaller designs.
  - Reproducible and high-yield process.
- Fundamental unity is the *minimum line width or mask dimension.*
  - *Generally set by resolution of patterning process like optical lithography, Electron beam EUV/X-ray sources.*
- *Differ from company to company and process to process even in same minimum dimensions.*
  - *This makes porting a design between processes a time-consuming task.*
  - *Such issue can be adressed by advanced CAD techniques or by scalable design rules.*

Scalable Design Rules

- Defines all rules as a function of single parameter, λ which can be changed accordingly to achieve scaling of dimension (Linear Scaling).
- For a process, λ is set to a specific value and all design dimensions are translated to absolute numbers. (Typically – min line width is 2λ).
- Disadvantages –
  - Linear scaling has limited range of dimensions. Scaling over large range, relations between layers vary non-linearly.
  - They are conservative: Over-dimensioned and less dense designs.
- Normally avoided by industry due to above reasons.
- Most companies use Micron Rules (for circuit density).

Micron-Rules Process

A complete design-rule entities are –

- Set of layers.
- Relations between object on same layers.
- Relations between object on different layers.

Layer Constraints – CMOS design entities

- Substrates/wells ***p-type*** (for NMOS devices) and ***n-type*** (PMOS devices).
- Diffusion or Active regions (n+ and p+).
- One or more polysilicon layers – *to form gate electrodes and serve as interconnect layers.*
- Metal interconnect layers.
- Contact and Via layers for interlayer connections.

Intra-layer Constraints

- Defines the minimum dimension of objects on each layer and
- Minimum spacing between objects on the same layer.

Micron-Rules Process

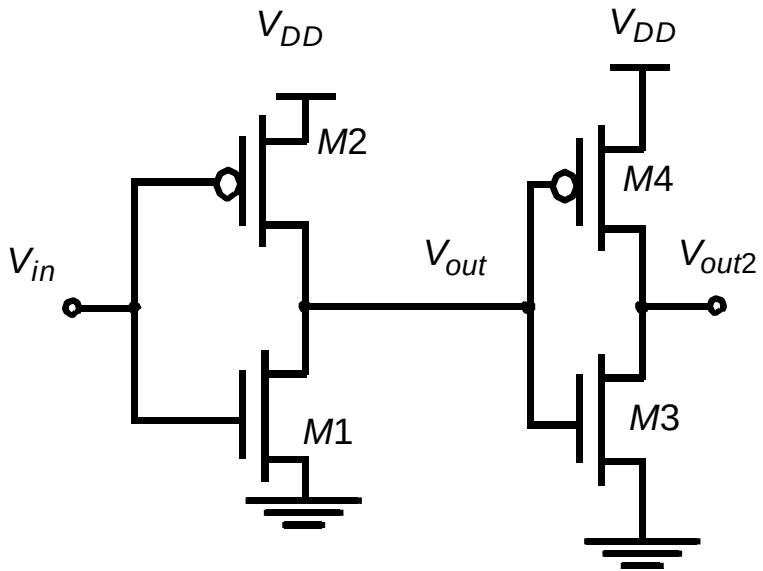
Interlayer Constraints (Involves multiple layer and hence complex.)

- **Transistor Rules –**
  - Form by overlap of active and polysilicon layers (min width of polysilicon and min width of diffusion).
  - Extra Rules include spacing between active area and well boundary, the gate overlap of active area.
- **Contact and Via Rules –**
  - Formed by overlapping the two interconnecting layers and providing a contact hole, filled with metal between the two.
  - Excessive changes between interconnect layers in routing should be avoided.
- **Well and Substrate Contacts –**
  - These regions are to be adequately connected to supply voltages.
  - Failing will lead to a resistive path and lead to parasitic effects like latchup.
  - Example – p+ diffusion layer is used to connect supply rail and *p-type* material.

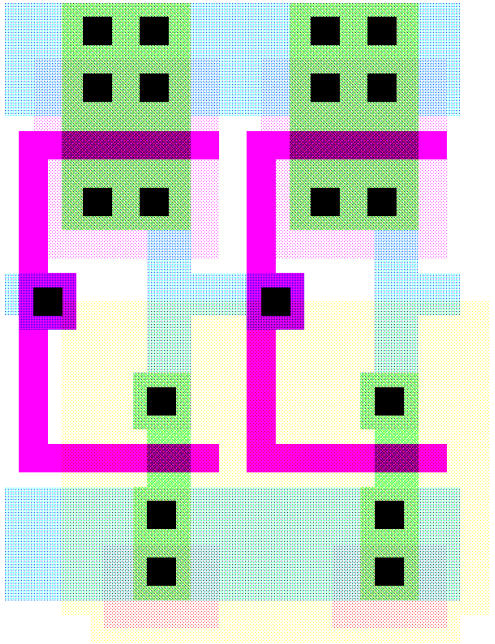
Layout Verfication

- Computer aided Design Rule Check (DRC) is performed to ensure a functional design.

Circuit under test



Schematic view



Layout view

Packaging ICs

There are four basic functions of a package –

1. Substantial lead system - electrical connectivity
   - Pins should exhibit low Capacitance, Resistance and Inductance.
   - Large characteristic impedance should be tuned to optimize transmission line behaviour.
   - Intrinsic IC impedance are high.
2. Physical protection
   - Strong connection from Die to package and package to board.
   - Mechanical reliability require good matching between thermal properties of die and carrier.
3. Low Cost and Environmental protection
   - Cost factor is reasonable in industry, Ceramics packages being superior in performance than plastic packages but are expensive.
   - Package should have a industry standards with IPA protection.
4. Heat Dissipation
   - Heat removal rate should be as high as possible.
   - Also important for chips that are used in mobile computing. Lower heat dissipation, by reduced power consumption, is also important for mobile computing since this save battery life.

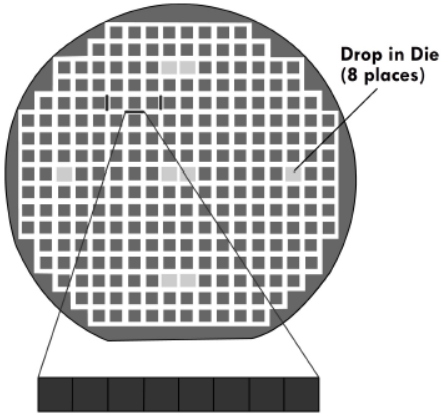
Characteristics that effect Packaging

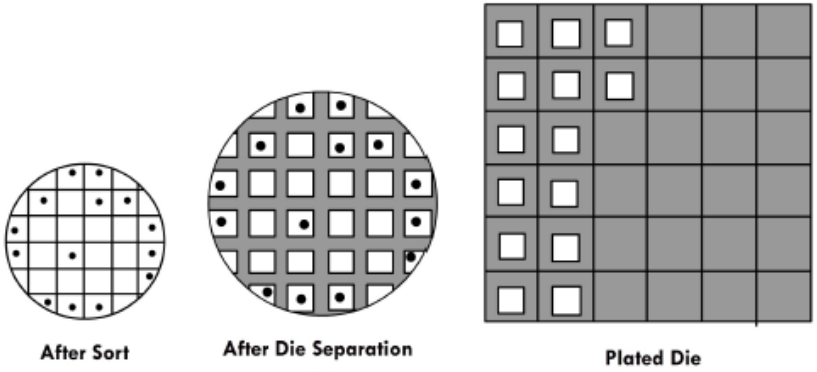
1. Integration level
2. Wafer thickness
3. Chip dimensions
4. Environmental sensitivity - important for lead free packaging
5. Physical vulnerability
6. Heat generation
7. Heat sensitivity

- Heat generation and sensitivity are important during operation since adequate provision must be given for heat dissipation).
- A passivation layer is grown on top of the wafer, at the end of the fabrication.
- Passivation layer can be a hard layer (like silicon nitride or oxide) or a soft layer like polyimide.

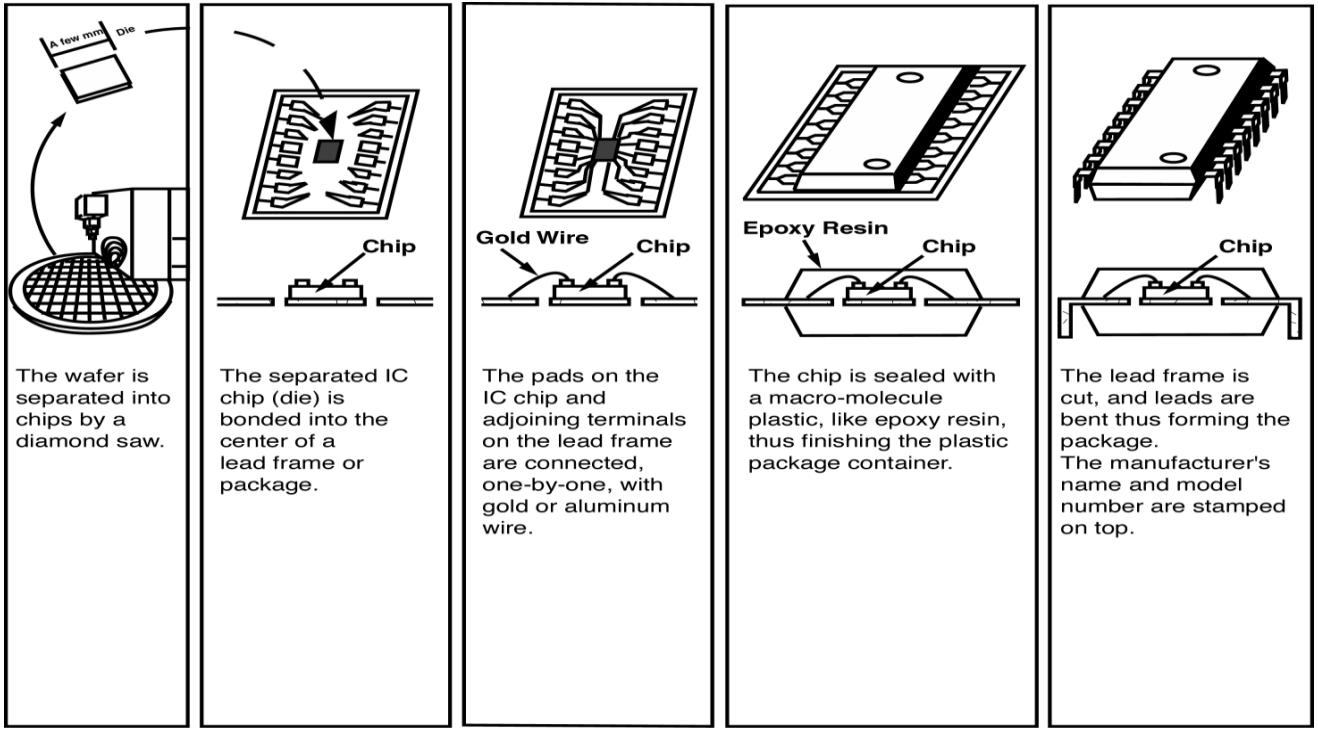
Packaging Process

- **Backside Prep**
  - Wafer is thinned by chemical mechanical polishing.
- **Die Separation**
  - Usually done by sawing or scribing wafer on patterned scribe lines.
- **Die Pick and Place**
  - Good/bad dies are identified in sort.
- **Die Inspection**
  - Inspected for cracks/defects on the good dies using automated optical microscope.
- **Die Attach**
  - Process is used to create a strong bond between the die and package (precursor for wire and tape bond process).





Assembling Process



The wafer is separated into chips by a diamond saw.

The separated IC chip (die) is bonded into the center of a lead frame or package.

The pads on the IC chip and adjoining terminals on the lead frame are connected, one-by-one, with gold or aluminum wire.

The chip is sealed with a macro-molecule plastic, like epoxy resin, thus finishing the plastic package container.

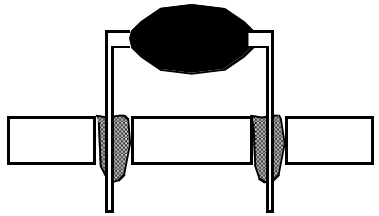
The lead frame is cut, and leads are bent thus forming the package.
The manufacturer's name and model number are stamped on top.

IC Packaging Classification

IC package categories:

PTH (pin-through-hole)

- Pins are inserted into through-holes in the circuit board and soldered in place from the opposite side of the board
  - Sockets available
  - Manual P&P possible

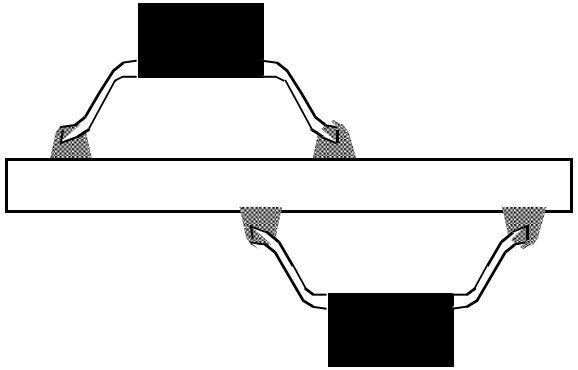


IC Packaging Classification

SMT (surface-mount-technology)

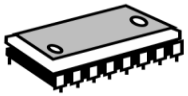
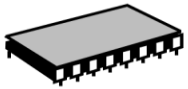
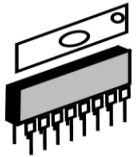
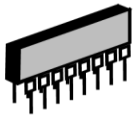
SMT packages have leads that are soldered directly to corresponding exposed metal lands on the surface of the circuit board

- Elimination of holes
- Ease of manufacturing (high-speed P&P)
- Components on both sides of the PCB
- Smaller dimensions
- Improved package parasitic components
- Increased circuit-board wiring density

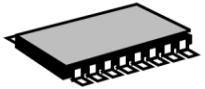
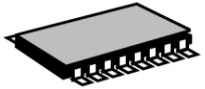
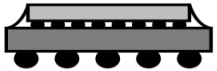


Different type of Packages

Through Hole Packages

a		DIP (Dual In-line Package)
b		SH-Dip (Shrink DIP)
c		SK-DIP, SL-DIP (Skinny DIP, Slim DIP)
d		SIP (Single In-Package)
e		ZIP (Zig-zag In-line Package)
f		PGA (Pin Grid Array) or Column Package

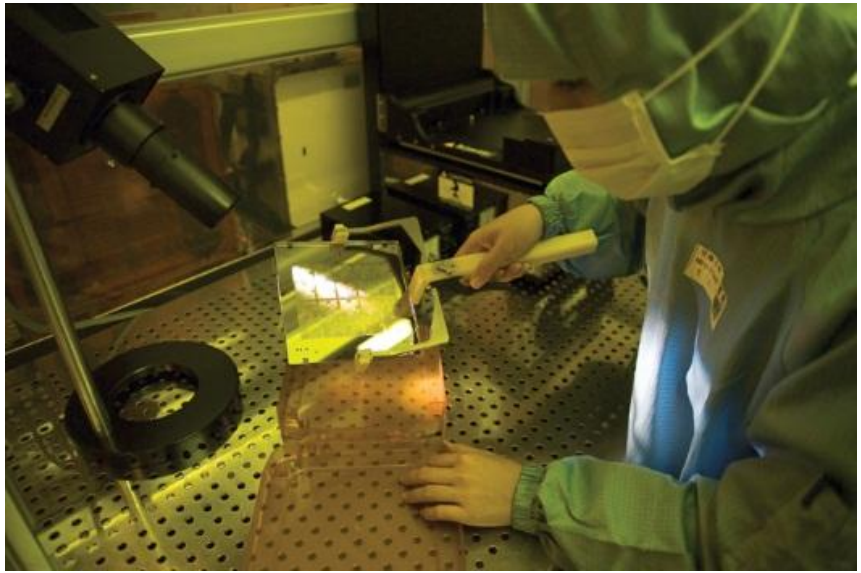
Surface Mount Packages

g		SO or SOP (Swell Out-Package)
h		CFP (Quad Flat Package)
i		LCC (Leadless Chip Carrier)
j		PLCC, SOJ (Plastic Leader Chip Carrier with Butt Leads)
k		BGA (Ball Grid Array)
l		TAB (Tape Automated Bonding)
m		CSP (Chip Scale Package)

Characteristic of Cleanroom environment

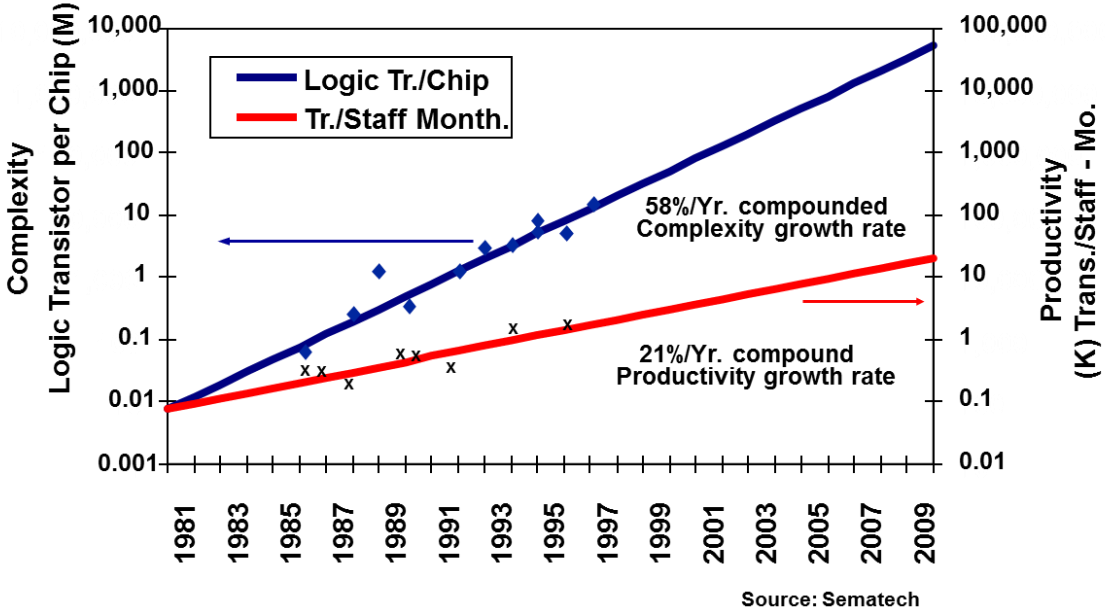
- Air is highly filtered – < 35 particles/ft^3
- Cleanroom clothing is used to prevent substances from being released off
- Air flow should remove most particles generated by process





Source :**Taiwan Semiconductor Manufacturing Co., Ltd.**

Productivity Trends



Complexity outpaces design productivity

Courtesy, ITRS Roadmap

Recapitulation

- Various Design rules can be implemented based on the device specification and packaging.
- Micron Rules being the most used in the industry due to its circuit density factor.
- Fabrication process of various IC chips can be analyzed to achieve better overview of the design.
- In electronics industry IC packaging is the final stage of device fabrication.
- Characteristics and stages of packaging may give details on the fabrication process and type of device.
- Cleanroom clothing and various SMT techniques are necessary in fabrication of an IC Chip and its testing.

Thank You