IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

MICROELECTRONICS: DEVICES TO CIRCUITS

Fabrication Process - I

SUDEB DASGUPTA

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING



Outline

- Fabrication
- Silicon wafer
- Photolithography
- Diffusion and Ion Implantation
- Deposition, Etching and Planarization
- Inverter cross-sectional view
- Fabrication steps

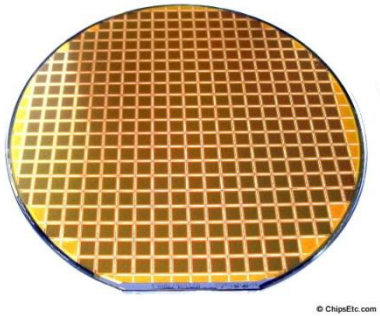
CMOS Fabrication

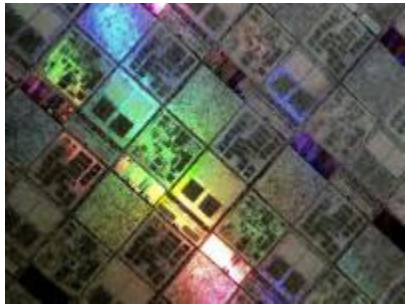
- CMOS Transistors are fabricated on Silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched

Silicon wafer

- Base material for MOS fabrication.
- Typical diameter 4 ~ 12 inches
- P-type doped with impurity level of $2 \times 10^{21} impurities / m^3$







Photolithography

- Photolithography transfers selective pattern from a mask to a photosensitive layer.
- Typical photolithography steps
  - Oxidation layering:
    - Optional steps to deposit very thin layer of SiO_2 over complete wafer.
  - Photoresist coating:
    - A light sensitive polymer, soluble in organic solvent.
    - Positive or negative type.
  - Stepper exposure:
    - Glass mask contain patterns to be imprinted on the wafer
    - Both the mask and wafer are exposed to ultraviolet light.
  - Development and bake:
    - The wafer is developed into the acid or base solution to remove the unwanted photoresist.
    - Soft bake to harden the remaining photoresist.
  - Acid etching:
    - Uncovered material are selectively remove by using of the acid or base solution.
  - Spin, rinse and dry:
    - Cleans the wafer with deionized water and dries it with nitrogen.

Diffusion and Ion Implantation

Diffusion Implantation

- The wafer is placed in a quatz tube embedded in a heated furnace ~900 to 1100 celcius.
- Dopants diffuse through into the exposed surface
- Dopant concentration is highest at the surface.

Ion Implantation

- Introduction of atoms into a solid substrate by bombardment with dopant ions
- This process provides excellent dose control.
- Complex doping profiles can be made using multiple energy implants.
- May damage the lattice because of nuclear collisions during the high energy implantation.

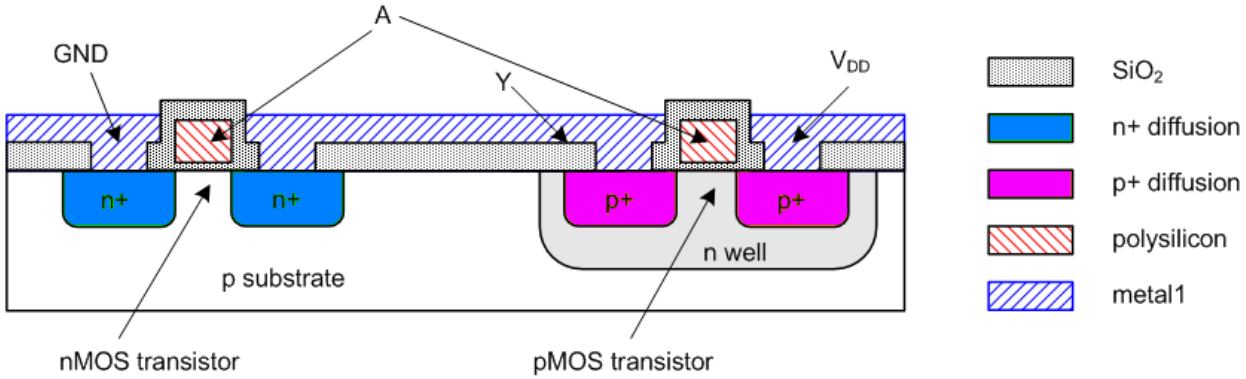
Deposition, Etching and Planarization

- Deposition :
  - Conducting layers such as poly-silicon and aluminium, and insulation and protection layers such as SiO_2 and Si_3N_4 are deposited onto the wafer surface by using the chemical vapor deposition (CVD) technique in a high-temperature chamber.
  - The deposition must be uniform throughout the wafer.
- Etching:
  - Once the mat, etching is used to remove excess material and form the required pattern.
  - Wet etching : chemical solution is used to etch away at a given temperature.
  - Dry etching : chemical reaction occurred between the material and gases and product will be gaseous.
- Planarization :
  - Chemical-mechanical planarization technique is included in fabrication process before depositing any metal layer.
  - To remove excess material.
  - To planarized the surface.

Inverter - Cross-Section view

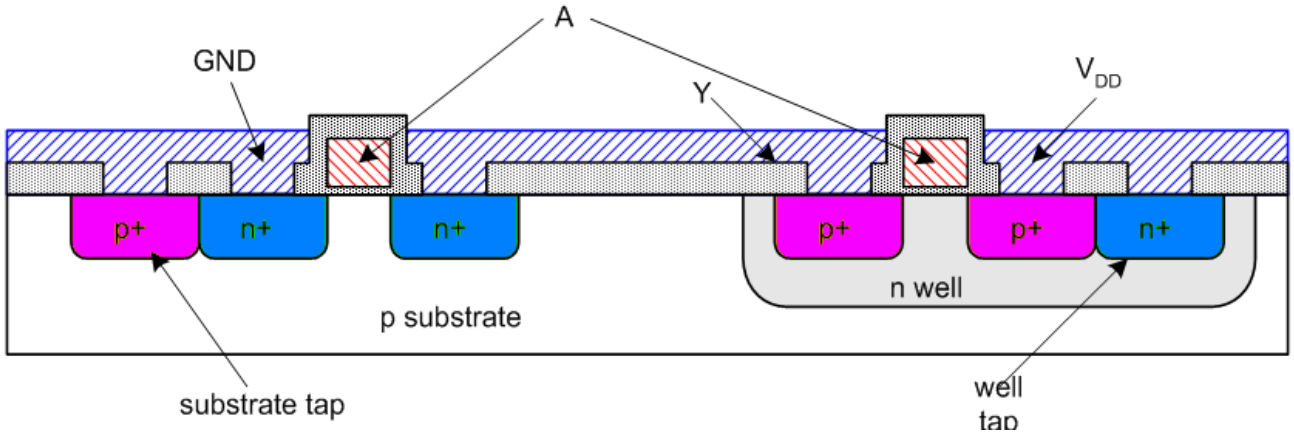
Typically use P-type substrate for NMOS transistors

- Requires n-well for body of pMOS transistors
- Several alternatives: SOI, twin-tub, etc.
- Silicon dioxide (SiO2) prevents metal from shorting to other layers



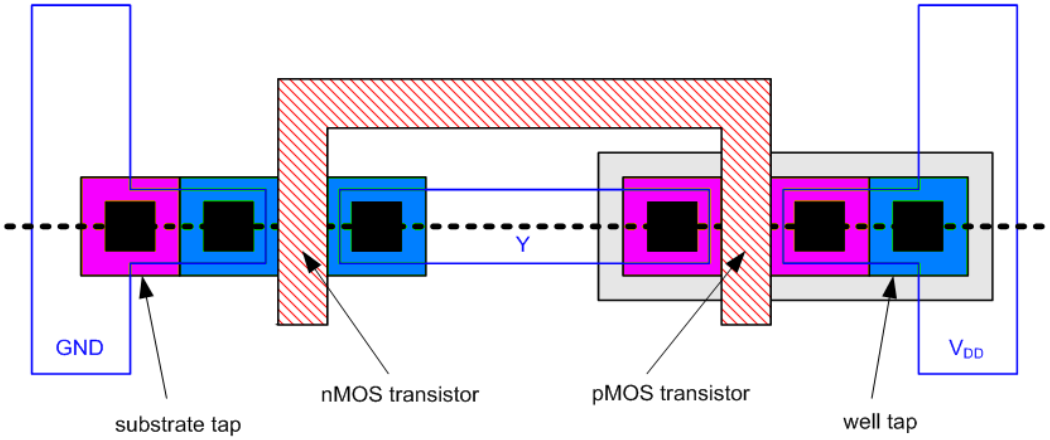
Well and Substrate Taps

- P-type substrate (body) must be tied to GND
- N-well is tied to VDD
- Use heavily doped well and substrate contacts / taps
- Create low resistance contact between substrate to supply line



Inverter Mask Set

- Transistors and wires are defined by masks
- Inverter can be obtained using six masks: n-well, poly-silicon, n+ diffusion, p+ diffusion, contacts and metal
- Cross-section taken along dashed line



Detailed Mask Views

n=well

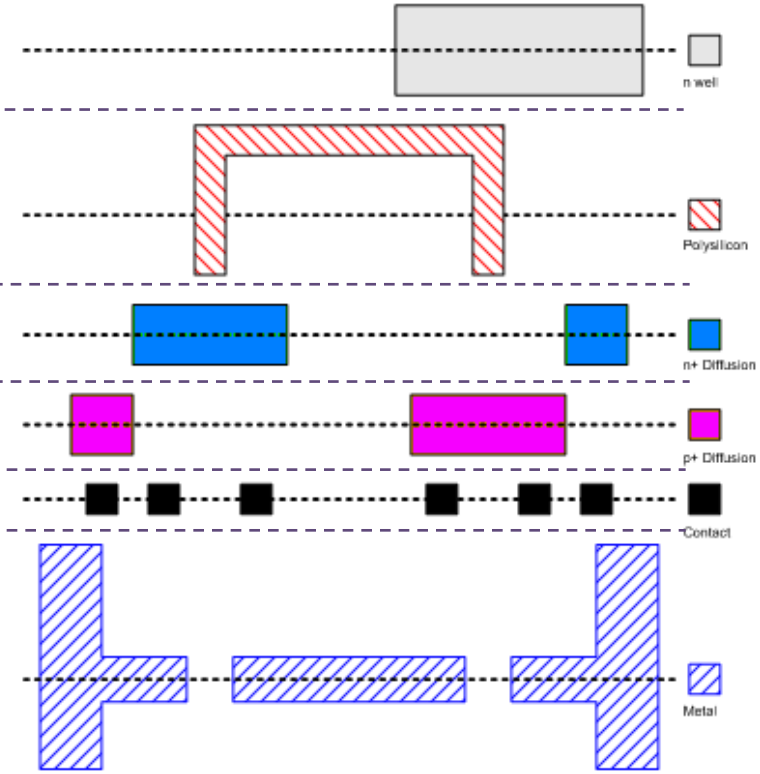
Polysilicon

N+ diffusion

P+ diffusion

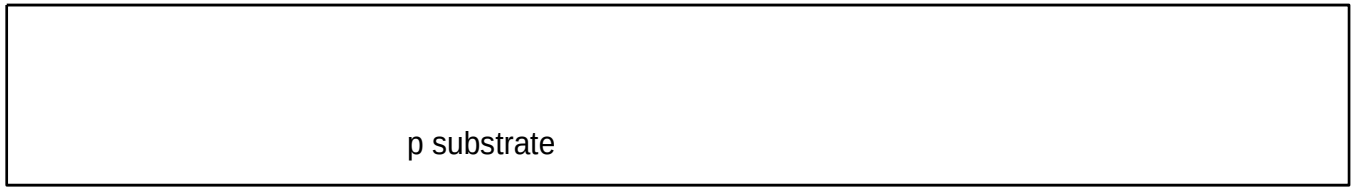
Contact

Metal



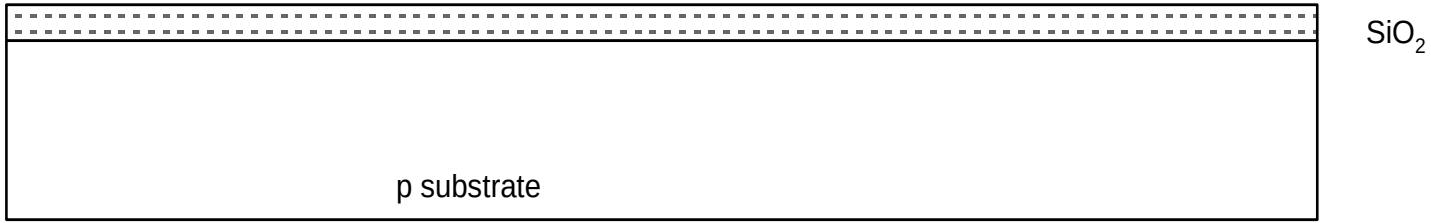
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO_2 (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO_2



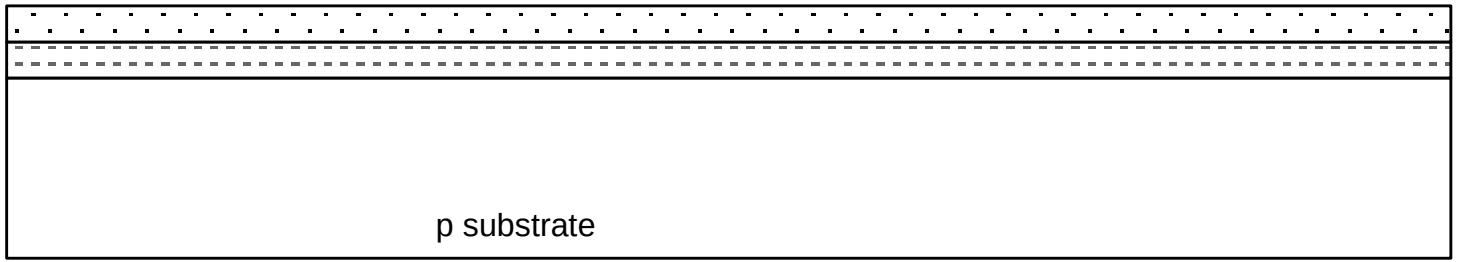
Oxidation

- Grow SiO_2 on top of Si wafer
- 900 – 1200 Celcius with H_2O or O_2 in oxidation furnace



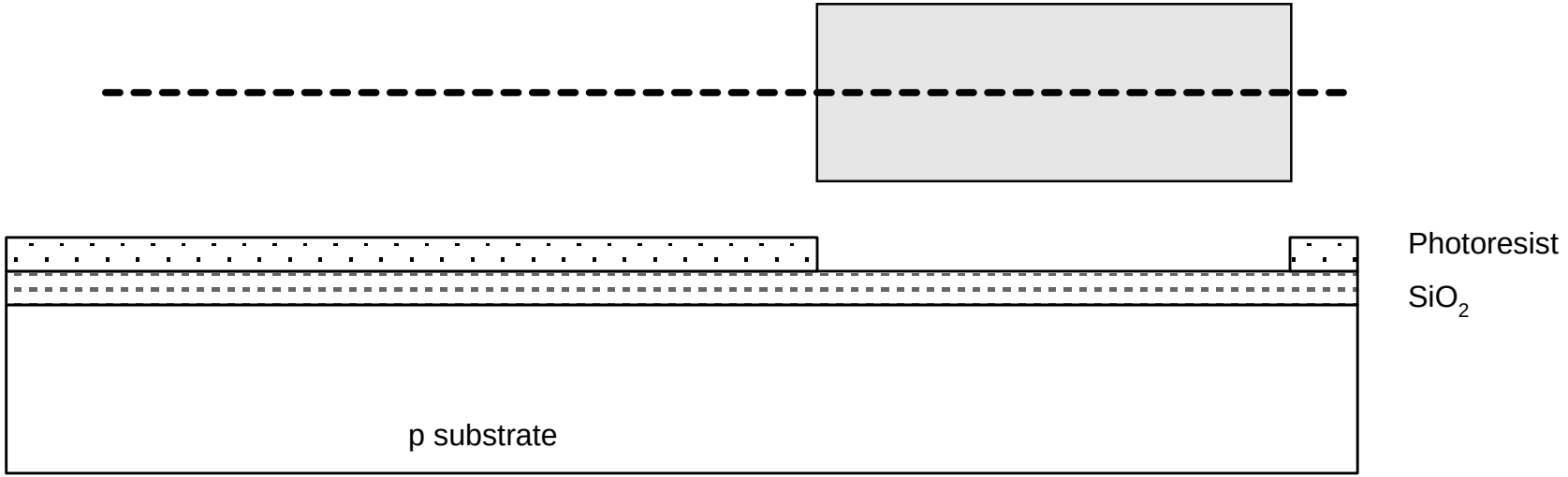
Photoresist

- Spin on photoresist
- Photoresist is a light-sensitive organic polymer
- Softens where exposed to light



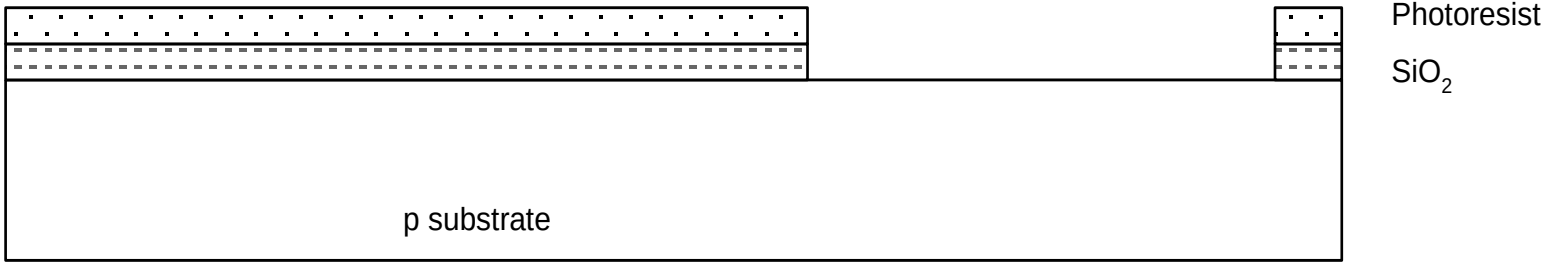
Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist



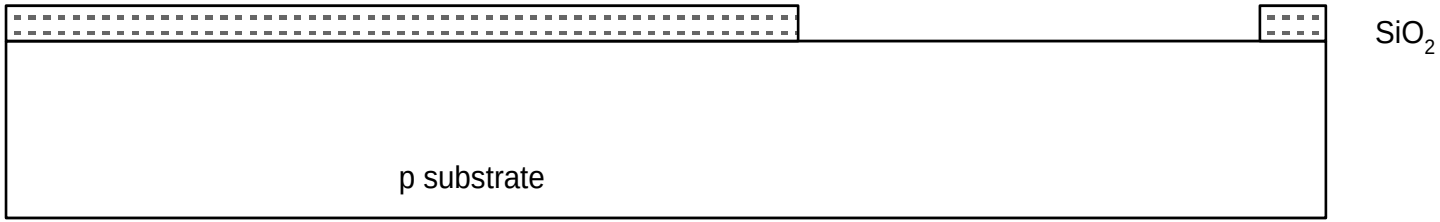
Etch

- Etch oxide with hydrofluoric acid (HF)
- Only attacks oxide where resist has been exposed



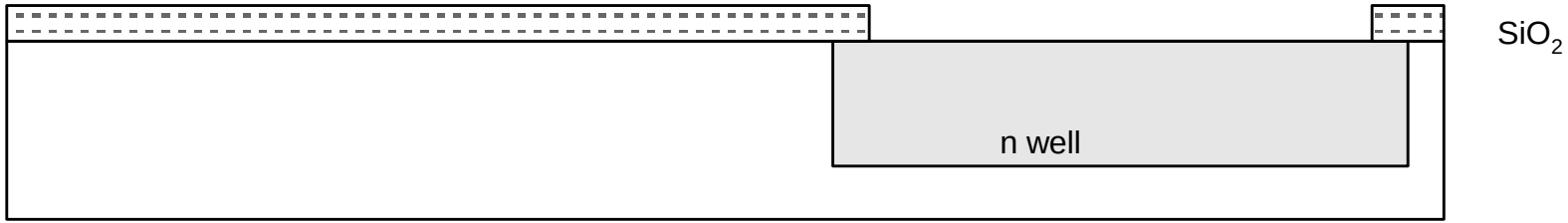
Strip Photoresist

- Strip off remaining photoresist
- Use mixture of acids
- Necessary so resist doesn't melt in next step



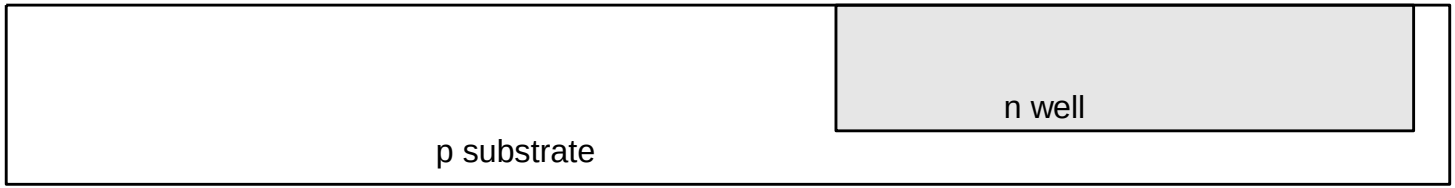
N-well

- N-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO2, only enter exposed Si



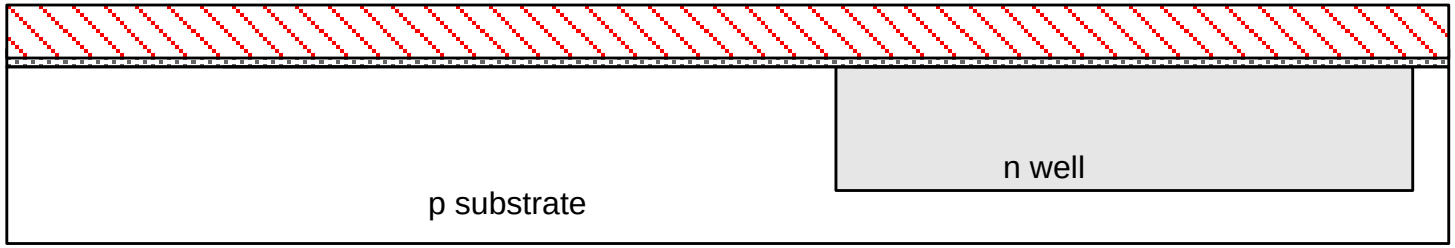
N-well

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



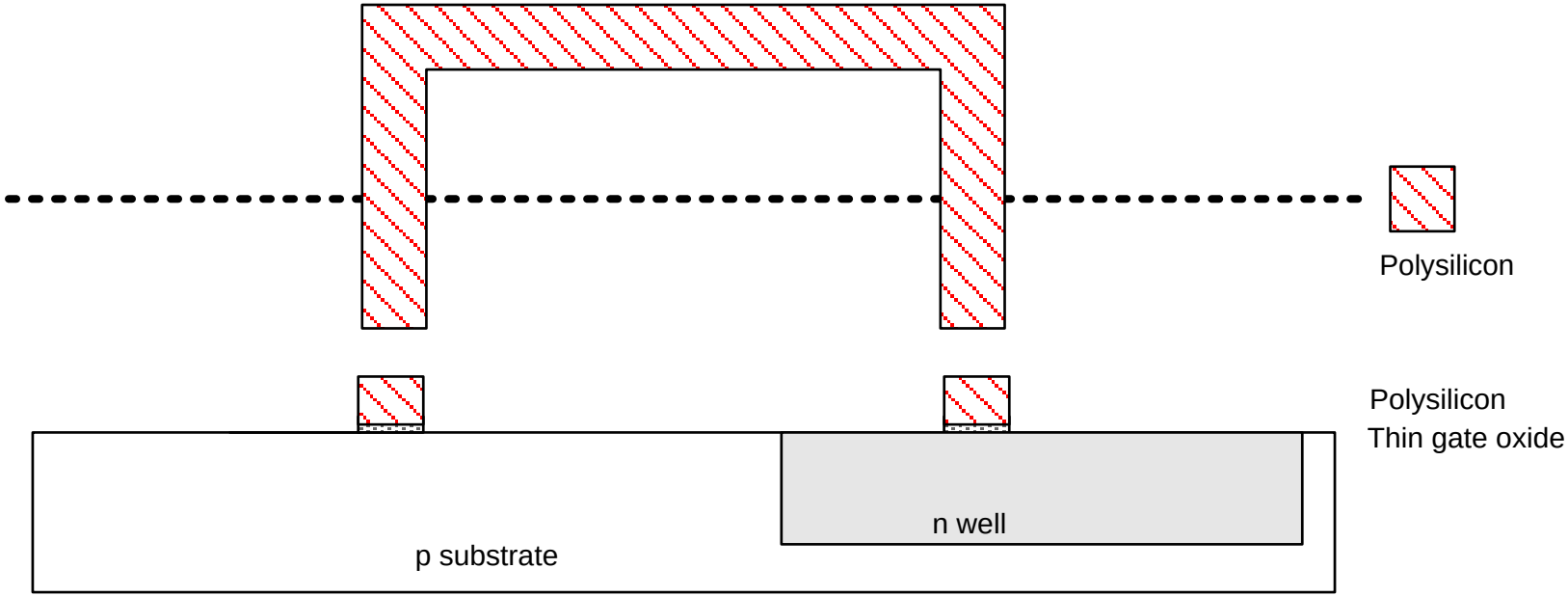
Polysilicon

- Deposit very thin layer of gate oxide (SiO_2)
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas (SiH_4)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



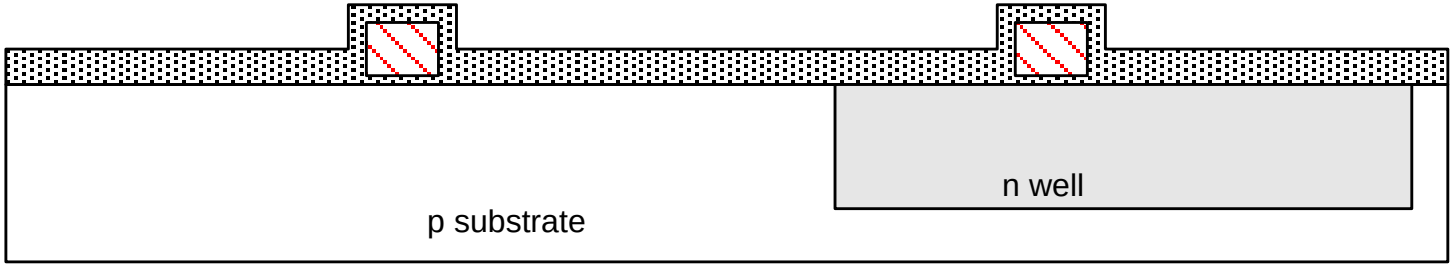
Polysilicon Patterning

- Use same lithography process to pattern polysilicon



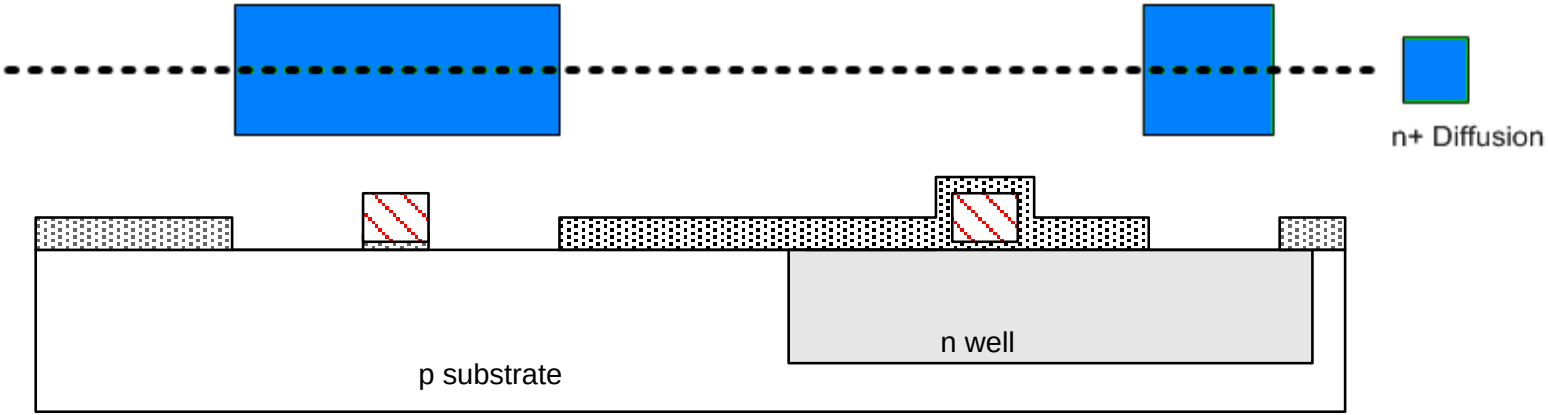
Self-Aligned Process

- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms NMOS source, drain, and n-well contact



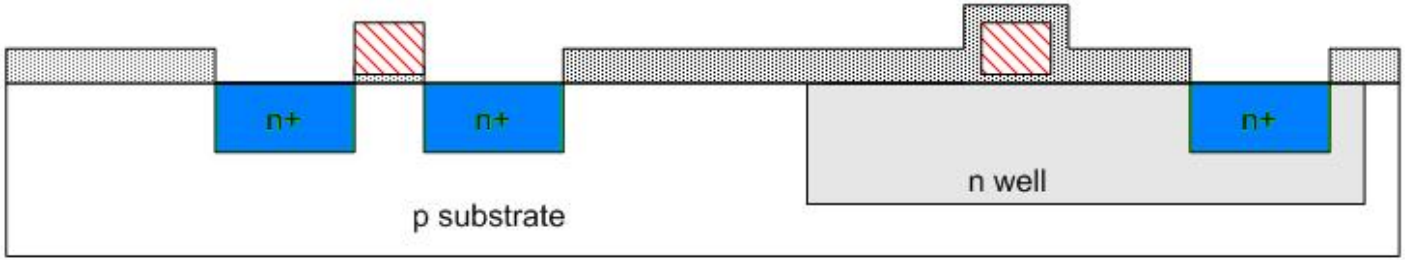
N-diffusion

- Pattern oxide and form n+ regions
- Self-aligned process where gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



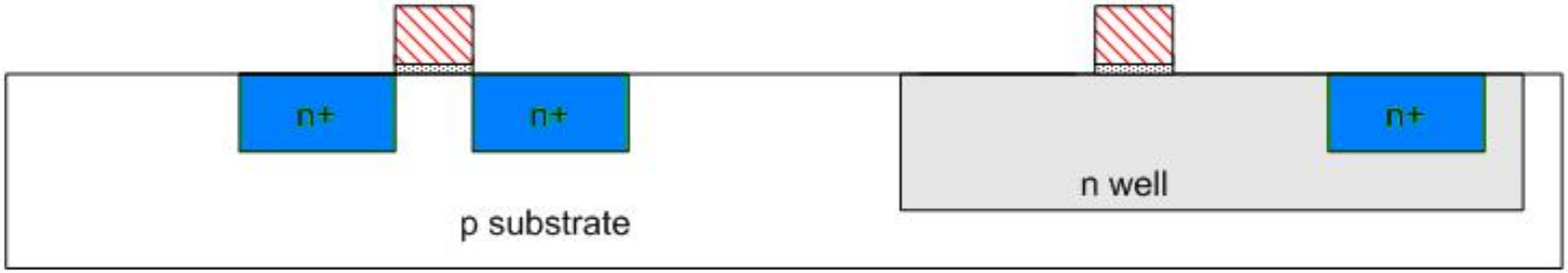
N-diffusion cont.

- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion



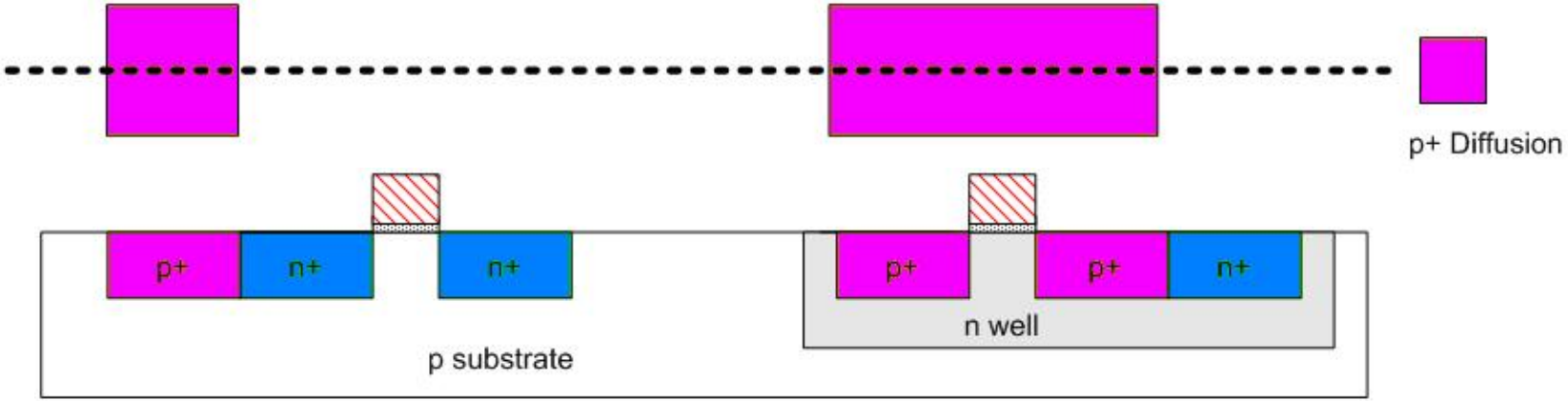
N-diffusion cont.

- Strip off oxide to complete patterning step



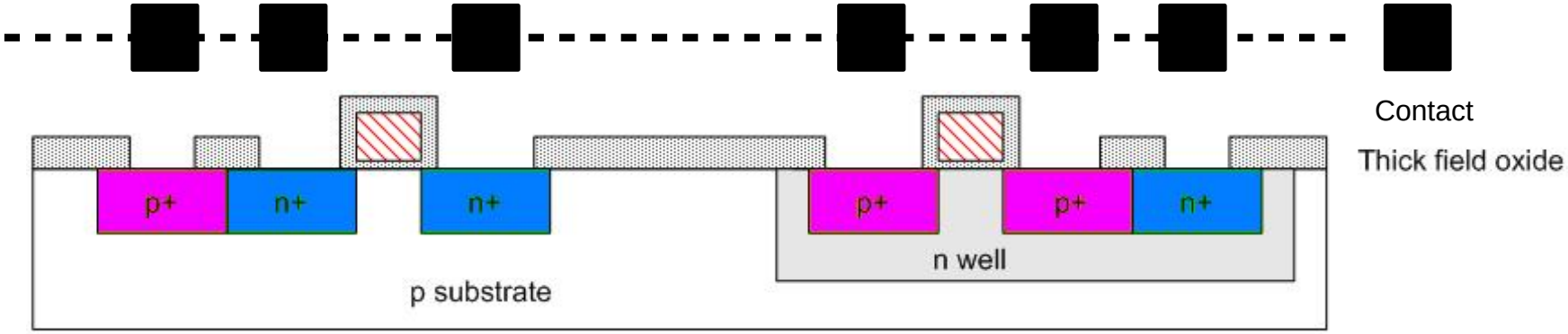
P-Diffusion

- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact



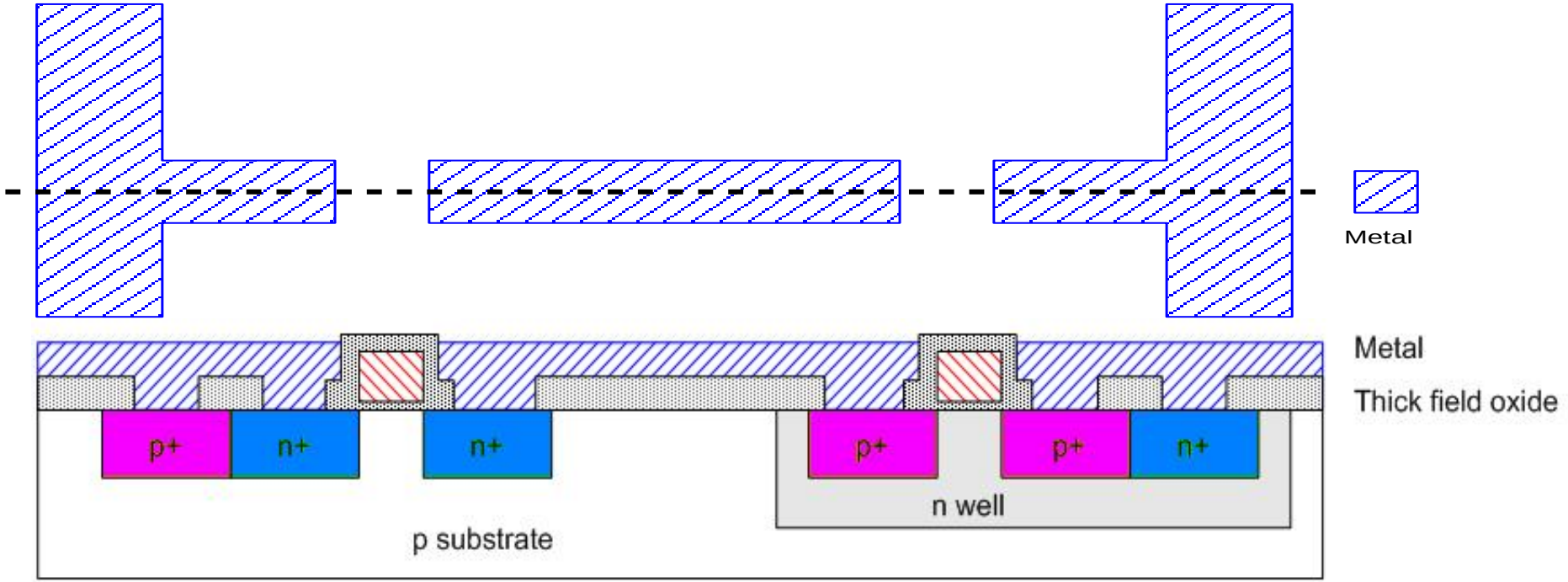
Contacts

- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed



Metallization

- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires



Thank You