IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

MICROELECTRONICS: DEVICES TO CIRCUITS

Logical Efforts- I

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Outline

- Introduction
- Basics of Logical effort
- Calculation of Logical Efforts for Logic Gates
- Multi Stage Logic Network
- Recapitulation

Introduction

- Designing a circuit to achieve the greatest speed or to meet a delay constraint presents a bewildering array of choices.
  - How large should a logic gate's transistors be to achieve least delay?
  - How many stages of logic should be used to obtain least delay?
- The **method of logical effort** is an easy way to minimize the delay in a Logic circuit. By comparing delay estimates of different logic structures, the fastest candidate can be selected or designed.
- Logical Effort also specifies the best no stages a logic path and the respective transistor sizes for the given load.

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Basics of Logical Effort

- The Logical effort model describes delays caused by the capacitive load that the logic gate drives and by the topology of the logic gate.
- The absolute delay of the gate can be expressed as:

$$d_{(abs)} = d\tau$$

✓ Where d is unit less delay of the gate and τ is the delay unit that characterizes by a given process. For 0.6µ process τ is about 50ps and 12ps for 0.18µ technology.

- Delay d of logic gate can be further divided into two components.

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Basics of Logical Effort Continue

- Delay ***d*** of logic gate can be written as :

$$d = f + p$$

Effort delay or stage effort

parasitic delay

- Effort delay further has two components,

$$f = g \times h$$

Electrical effort

logical effort

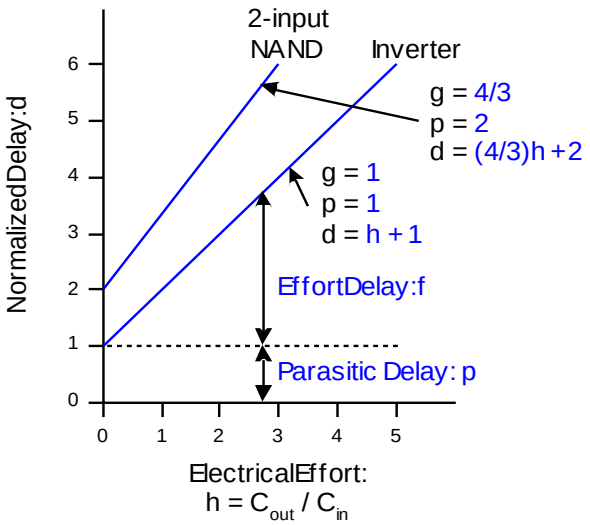
$$h = {C_{out}}/{C_{in}}$$; some times called fan-out

C_{out} and C_{in} are output and input capacitances respectively.

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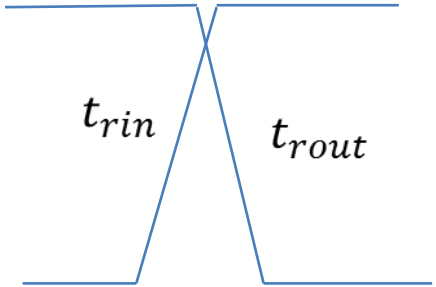
- The logical effort of a logic gate tells how much worse it is at producing output current than is an inverter, given that each of its inputs may contain only the same input capacitance as the inverter.

- Delay of the logic gate increases with electrical effort.
- More complex logic gates have more logical effort and parasitic delay.
  - Plots in the figure shows delay equation for an inverter and a two-input NAND gate.



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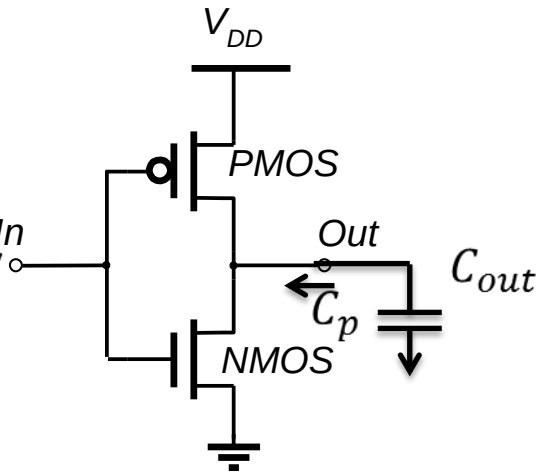
Inverter's Logical Effort

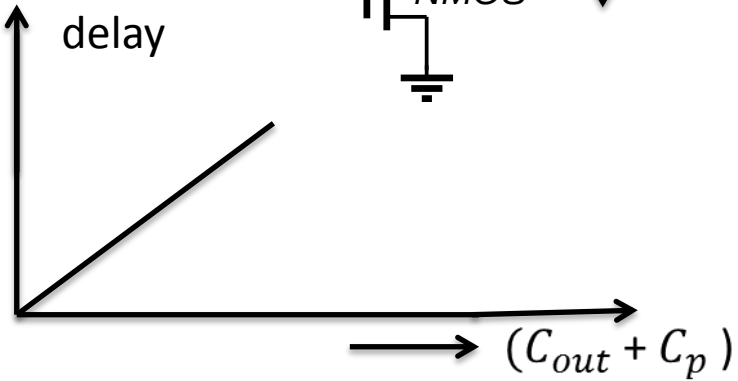


For $t_{rin} = t_{rout}$

$t_{rin} \propto (C_{out} + C_p) \rightarrow \beta.delay$

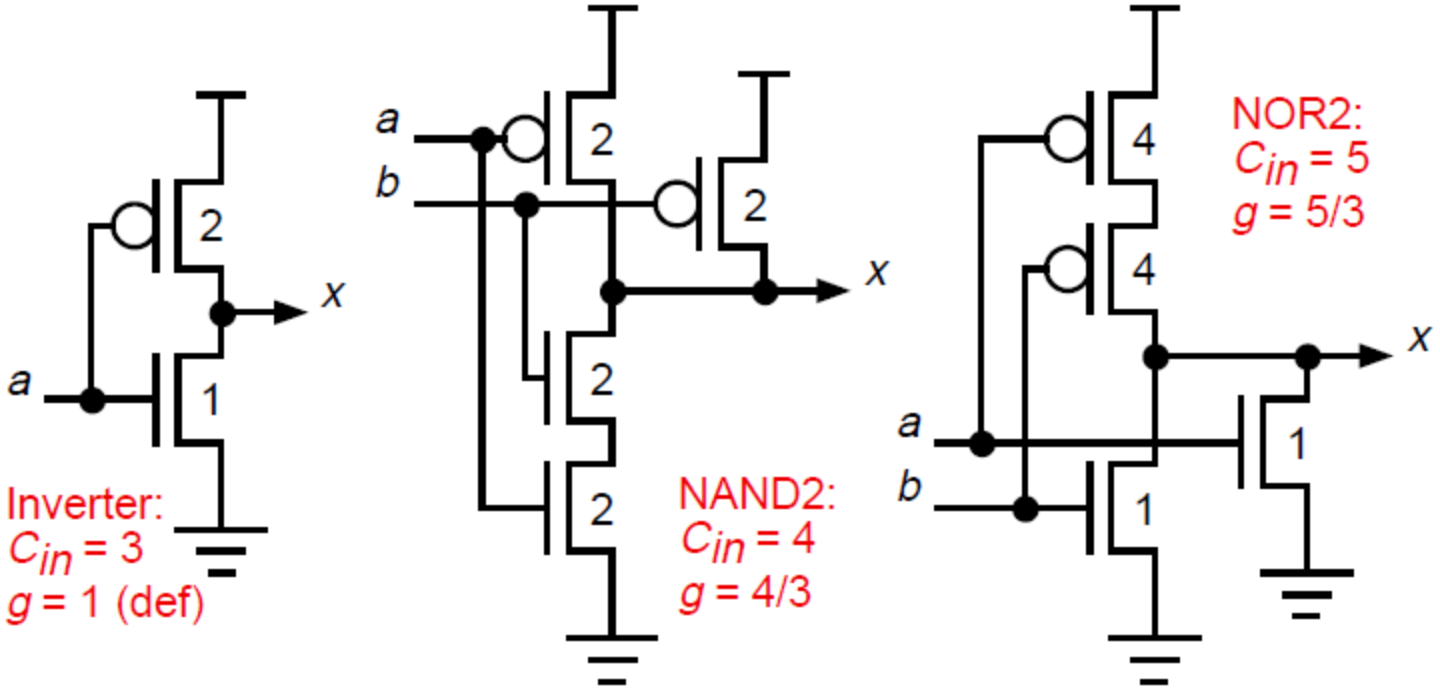
$\beta.\ t_{rin} \propto \beta.(C_{out} + C_p)$





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Logical effort calculation



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Logical effort & Parasitic delay of common Gates

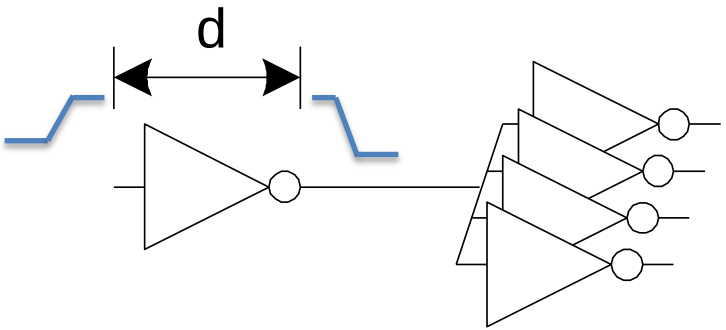
Logic Gate	No of Inputs				Parasitic Delay
	1	2	3	n	
Inverter	1	-	-	-	P_{inv}
NAND	-	4/3	5/3	(n+2)/3	nP_{inv}
NOR	-	5/3	7/3	(2n+1)/3	nP_{inv}
XOR(parity)	-	4	12		$4P_{inv}$
Multiplexer	-	2	2	2	$2nP_{inv}$

- Where n in parasitic delay Is no. of Inputs

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EXAMPLE 1 Fan-out 4 (FO4) Inverter Delay

- Calculate the delay for FO4 Inverter.



$f=g*h=1 \times 4$

$P_{inv} = 1$

$d= f + P_{inv}$

$d= 4 + 1= 5$

$d_{(abs)} = d\tau$

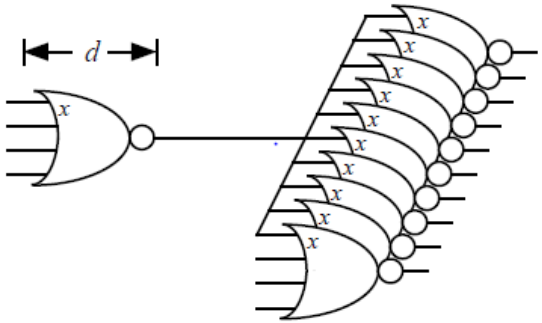
τ (typically) = 12ps for 180nm technology

$d_{(abs)} = 5 \times 12 = 60ps$

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EXAMPLE 2 Delay for 4 Input NOR Logic Gate

- Calculate the delay for 4 input NOR gate which drives 10, 4 Input NOR gates?



$f=g*h=9/3 \times 10 ; h= 10$

$P_{inv} = 4$

$d= f + P_{inv}$

$d= 30 + 4= 34$

$d_{(abs)} = d\tau$

τ (typically) = 12ps for 180nm technology

$d_{(abs)} = 34 \times 12 = 408ps$

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Logical Efforts Multi Stage Logic Networks

- ***Logical effort ensures to get least overall delay by balancing the delay among all stages.***
- ***The logical effort along a path compounds by multiplying the logical efforts of all the logic gates.***

$$\text{Path Logical effort } G = \prod g_i$$

$$\text{Path Electrical effort } H = {}^{C_{out}}/_{C_{in}}$$

$$\text{Branching effort } b = \frac{C_{onpath} + C_{offpath}}{C_{onpath}}$$

$$\text{Path Branching effort } B = \prod b_i$$

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$$\text{Path effort } F = GBH$$

$$BH = \frac{C_{out}}{C_{in}} \prod b_i = \prod h_i$$

- The delay of the path will be

$$D = \sum d_i = D_F + P$$

$$D_F = \sum g_i h_i$$

$$P = \sum p_i$$

- The path delay is least when each stage in the path bears the same stage effort.
- For a N stage Network ,stage effort for each stage will be

$$\hat{f} = g_i h_i = F^{\frac{1}{N}}$$

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The minimum achievable delay along a path will be,

$$\hat{D} = N * F^{\frac{1}{N}} + P$$

$$\hat{h}_i = F^{\frac{1}{N}} / g_i$$

$$\hat{h}_i = \frac{C_{out-i(total)}}{C_{in-i}}$$

The capacitance seen at the input of each stage will be,

$$C_{in-i} = C_{out-i(total)} / \hat{h}_i$$

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Recapitulation

Term	Stage	Path
Number of stages	1	N
Logical effort	g	$G = \prod g_i$
Electrical effort	$h = \frac{C_{out}}{C_{in}}$	$H = \frac{C_{out\text{-}path}}{C_{in\text{-}path}}$
Branching effort	$b = \frac{C_{on\text{-}path} + C_{off\text{-}path}}{C_{on\text{-}path}}$	$B = \prod b_i$
Effort	$f = gh$	$F = GBH$
Effort delay	f	$D_F = \sum f_i$
Parasitic delay	p	$P = \sum p_i$
Delay	$d = f + p$	$D = \sum d_i = D_F + P$

THANK YOU