IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

MICROELECTRONICS: DEVICES TO CIRCUITS

Power Analysis-I

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Metrics: Energy and Power

- Energy
  - Measured in Joules or kWh
  - “Measure of the ability of a system to do work or produce a change”
  - “No activity is possible without energy.”
- Power
  - Measured in Watts or kW
  - “Amount of energy required for a given unit of time.”
  - Average power
    - Average amount of energy consumed per unit time
    - Simplified to "power" in clear contexts
  - Instantaneous power
    - Energy consumed if time unit goes to zero

Metrics: Energy and Power cont'd

- Instantaneous Electrical Power P(t)
  - P(t) = v(t) * i(t)
  - v(t): Potential difference (or voltage drop) across component
  - i(t): Current through component
- Electrical Energy
  - E = P(t) * t = v(t) * i(t) * t
- Electrical Energy in CMOS circuits
  - Energy = Power * Delay
  - Why?

Power and Energy

- Power is drawn from a voltage source attached to the V_{DD} pin(s) of a chip.
- Instantaneous Power:

$$P(t) = i_{DD}(t)V_{DD}$$

- Energy:

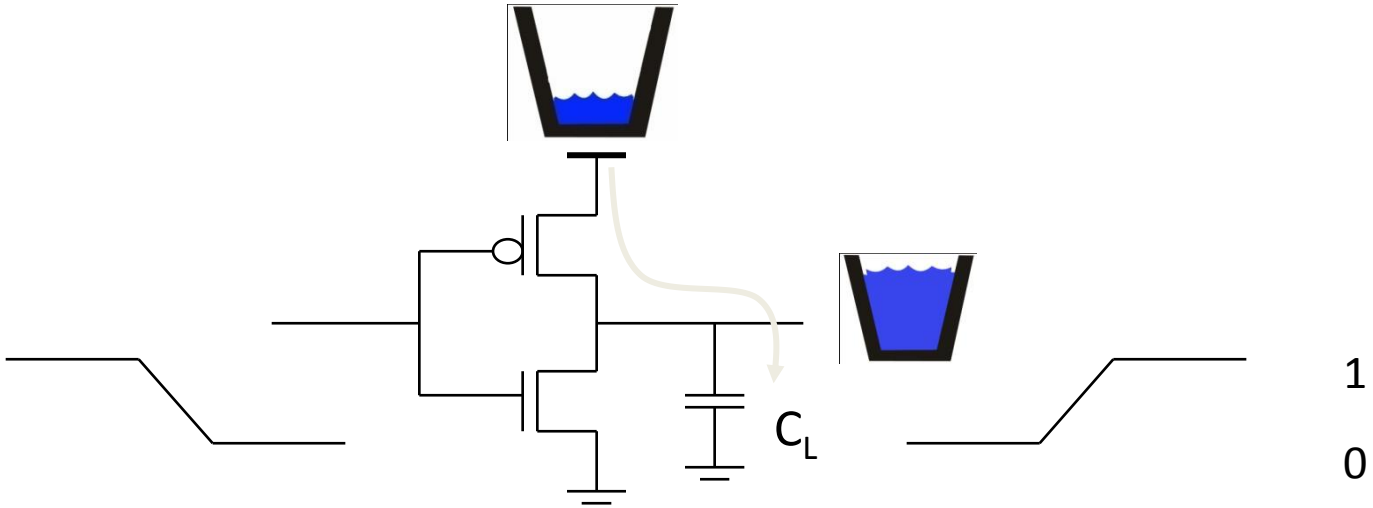
$$E = \int_0^T P(t)dt = \int_0^T i_{DD}(t)V_{DD}dt$$

- Average Power:

$$P_{\text{avg}} = \frac{E}{T} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}dt$$

Power Consumption in CMOS

- Voltage (Volt, V) — Water pressure (bar)
- Current (Ampere, A) — Water quantity per second (liter/s)
- Energy — Amount of Water



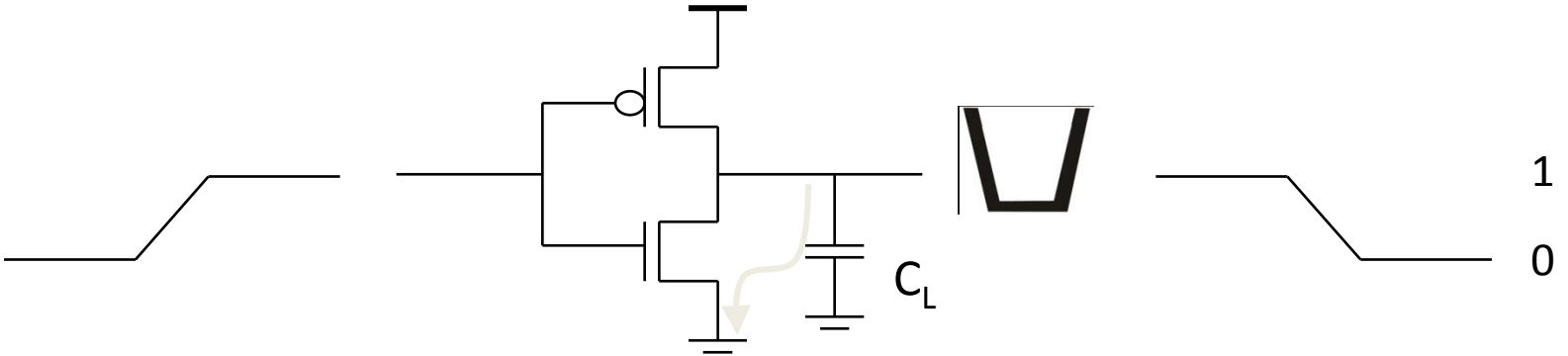
Energy consumption is proportional to capacitive load!

Consumption in CMOS cont'd

- Voltage (Volt, V)
- Current (Ampere, A)
- Energy



Water pressure (bar)
Water quantity per second (liter/s)
Amount of Water

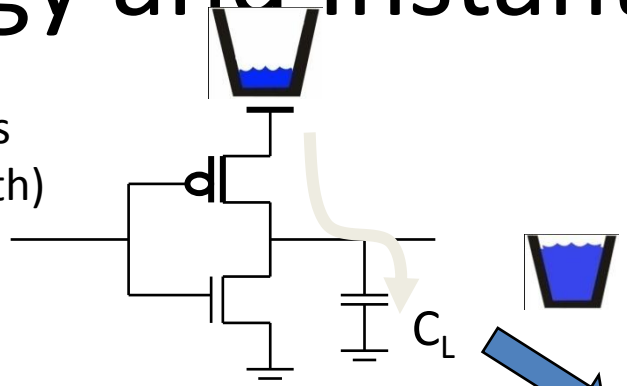




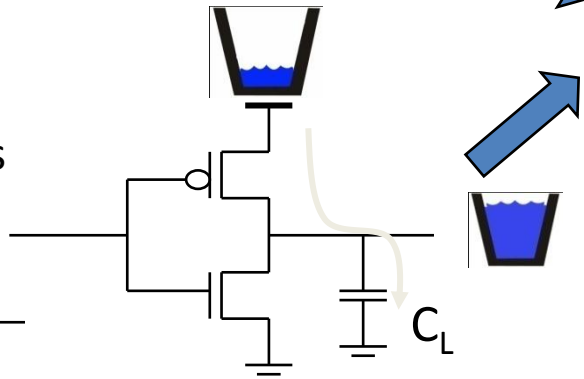
Energy for calculation only consumed at 0→1 at output

Energy and Instantaneous Power

INV1:
High instantaneous
Power (bigger width)

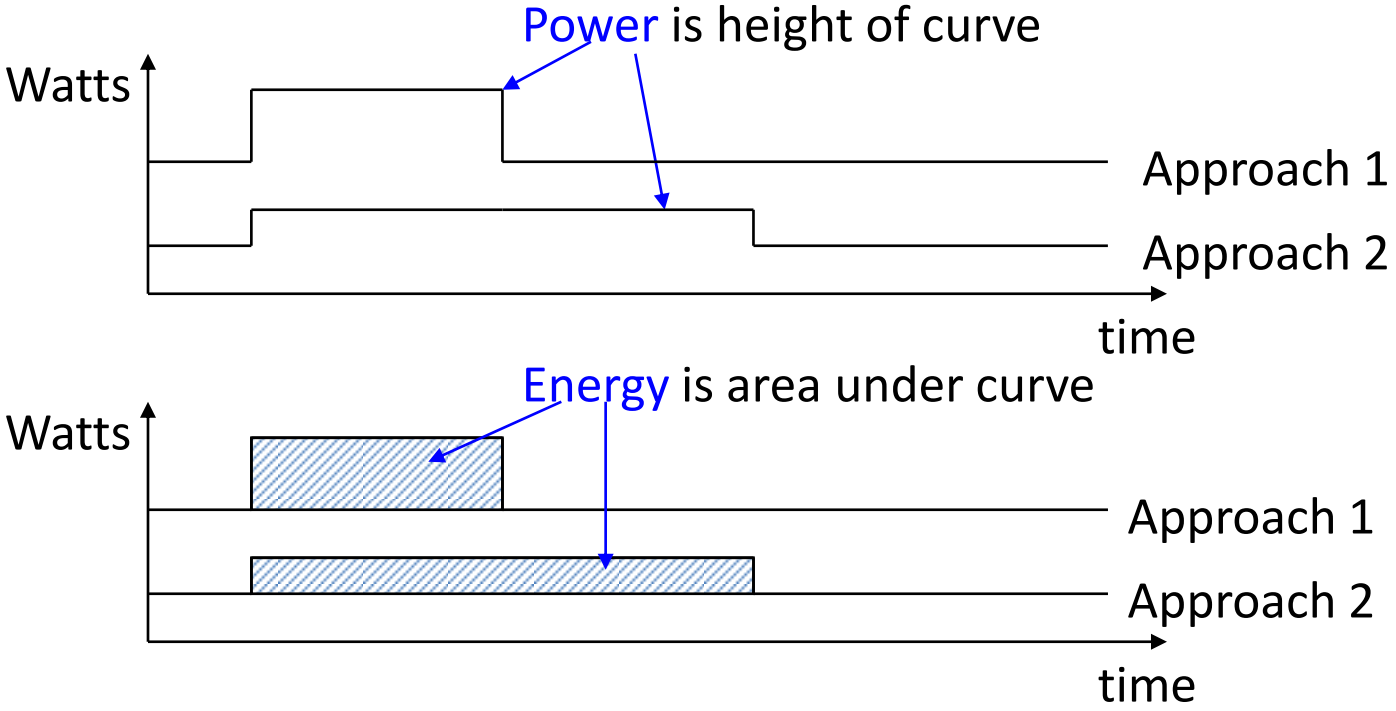


INV2:
Low instantaneous
power



- Same Energy (C_{in} ingnored)
- INV1 is faster

Metrics: Energy and Power cont'd



Energy = Power * time for calculation = Power * Delay

Metrics: Energy and Power cont'd

- Energy dissipation
  - Determines battery life in hours
  - Sets packaging limits
- Peak power
  - Determines power ground wiring designs
  - Impacts signal noise margin and reliability analysis

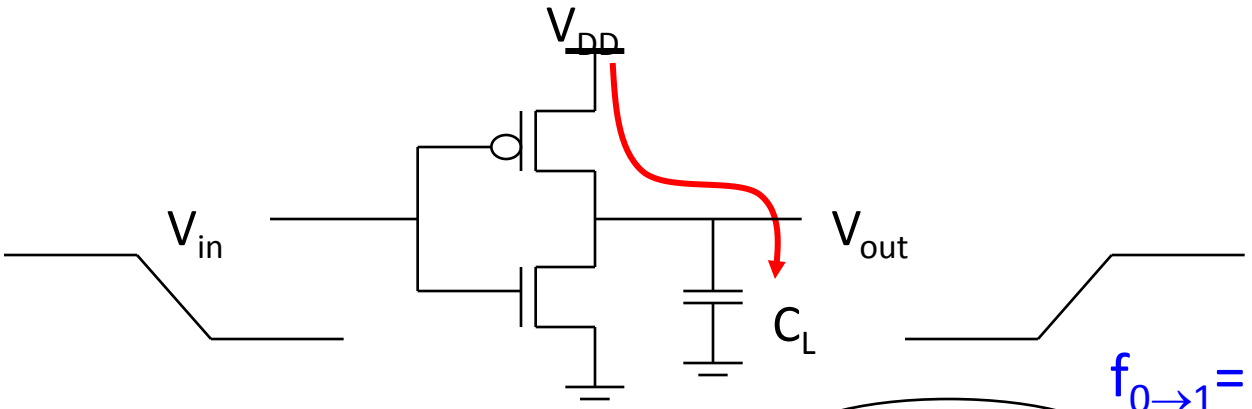
Metrics: PDP and EDP

- Power-Delay Product
  - Power P, delay t_p
  - Quality criterion PDP = P * t_p [J]
    - P and t_p have some weight
    - Two designs can have same PDP, even if t_p = 1 year
- Energy-Delay Product
  - EDP = PDP * t_p = P * t_p^2
  - Delay t_p has higher weight

Where Does Power Go in CMOS?

- Dynamic Power Consumption
  - Charging and Discharging Capacitors
- Short Circuit Currents
  - Short Circuit Path between Supply Rails during Switching
- Leakage
  - Leaking diodes and transistors

Dynamic Power Consumption



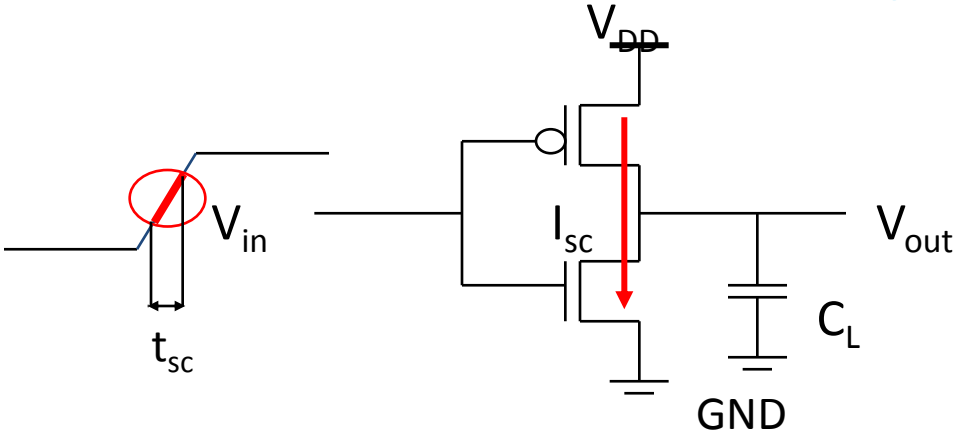
$P_{0\to1}$: probability for 0-to-1 switch of output

f : clock frequency

α : activity

Data dependent - a function of switching activity!

Short Circuit Power Consumption



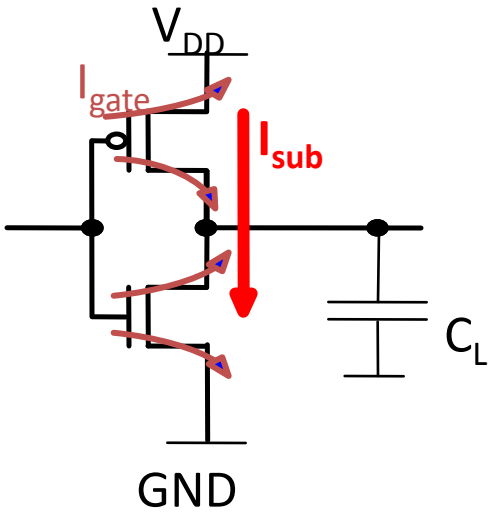
- Finite slope of input signal

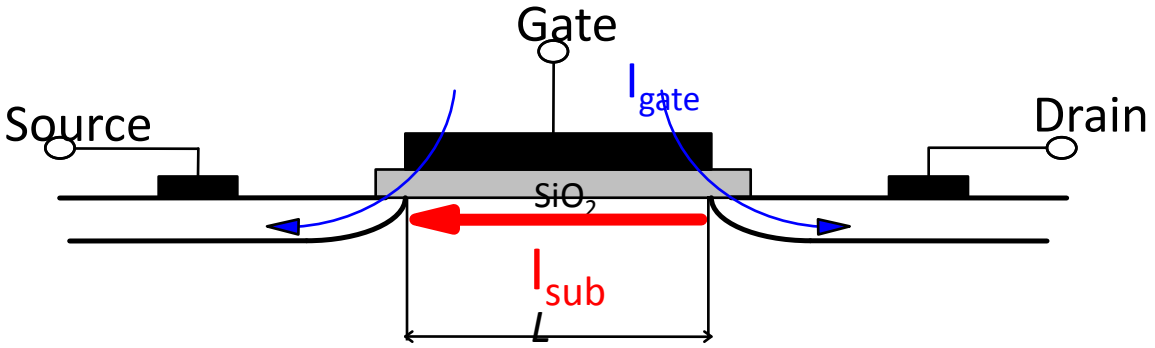
➔ During switching: NMOS and PMOS transistors are conducting for short period of time (t_{sc})

➔ Direct current path between VDD and GND

$$P_{sc} = V_{DD} * I_{sc} * (P_{0\rightarrow1} + P_{1\rightarrow0})$$

Leakage Power Consumption





- Most important Leakage currents:
  - Subthreshold Leakage I_{sub}
  - Gate Oxide Leakage I_{gate}
- $P_{leak} = I_{leak} * V_{DD} \approx (I_{sub} + I_{gate}) * V_{DD}$

Power Equations in CMOS

$$P = \alpha f C_L V_{DD}^2 + V_{DD} I_{peak} (P_{0\rightarrow1} + P_{1\rightarrow0}) + V_{DD} I_{leak}$$

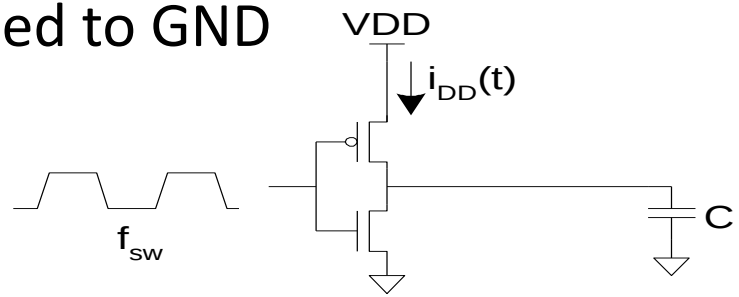
Dynamic power (≈ 40 - 70% today and decreasing relatively)

Short-circuit power (≈ 10 % today and decreasing absolutely)

Leakage power (≈ 20 – 50 % today and increasing)

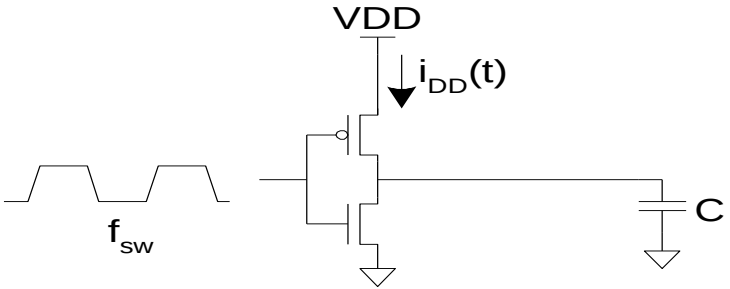
Dynamic Power

- Dynamic power is required to charge and discharge load capacitances when transistors switch.
- One cycle involves a rising and falling output.
- On rising output, charge $Q = CV_{DD}$ is required
- On falling output, charge is dumped to GND
- This repeats Tf_{sw} times over an interval of T



Dynamic Power Cont.

$$P_{\text{dynamic}} =$$



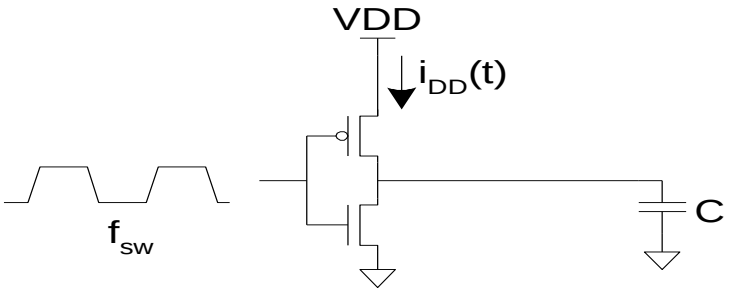
Dynamic Power Cont.

$$P_{\text{dynamic}} = \frac{1}{T}\int_0^T i_{DD}(t)V_{DD}\,dt$$

$$= \frac{V_{DD}}{T}\int_0^T i_{DD}(t)\,dt$$

$$= \frac{V_{DD}}{T}\left[Tf_{sw}CV_{DD}\right]$$

$$= CV_{DD}{}^2 f_{sw}$$



Activity Factor

- Suppose the system clock frequency = f
- Let $f_{sw} = \alpha f$, where α = activity factor

$$P_{\text{dynamic}} = \alpha C V_{DD}^{\ 2} f$$

  - If the signal is a clock, $\alpha = 1$
  - If the signal switches once per cycle, $\alpha = ½$
  - Dynamic gates:
    - Switch either 0 or 2 times per cycle, $\alpha = ½$
  - Static gates:
    - Depends on design, but typically $\alpha = 0.1$

Static Power

- Static power is consumed even when chip is quiescent.
  - Ratioed circuits burn power in fight between ON transistors
  - Leakage draws power from nominally OFF devices

$$I_{ds} = I_{ds0} e^{\frac{V_{gs} - V_t}{n v_T}} \left[1 - e^{\frac{-V_{ds}}{v_T}} \right]$$

$$V_t = V_{t0} - \eta V_{ds} + \gamma \left(\sqrt{\phi_s + V_{sb}} - \sqrt{\phi_s} \right)$$

Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C:
  - V_{DD}:
  - f:
- Reduce static power

Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C: small transistors (esp. on clock), short wires
  - V_{DD}:
  - f:
- Reduce static power

Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C: small transistors (esp. on clock), short wires
  - V_{DD}: lowest suitable voltage
  - f:
- Reduce static power

Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C: small transistors (esp. on clock), short wires
  - V_{DD}: lowest suitable voltage
  - f: lowest suitable frequency
- Reduce static power

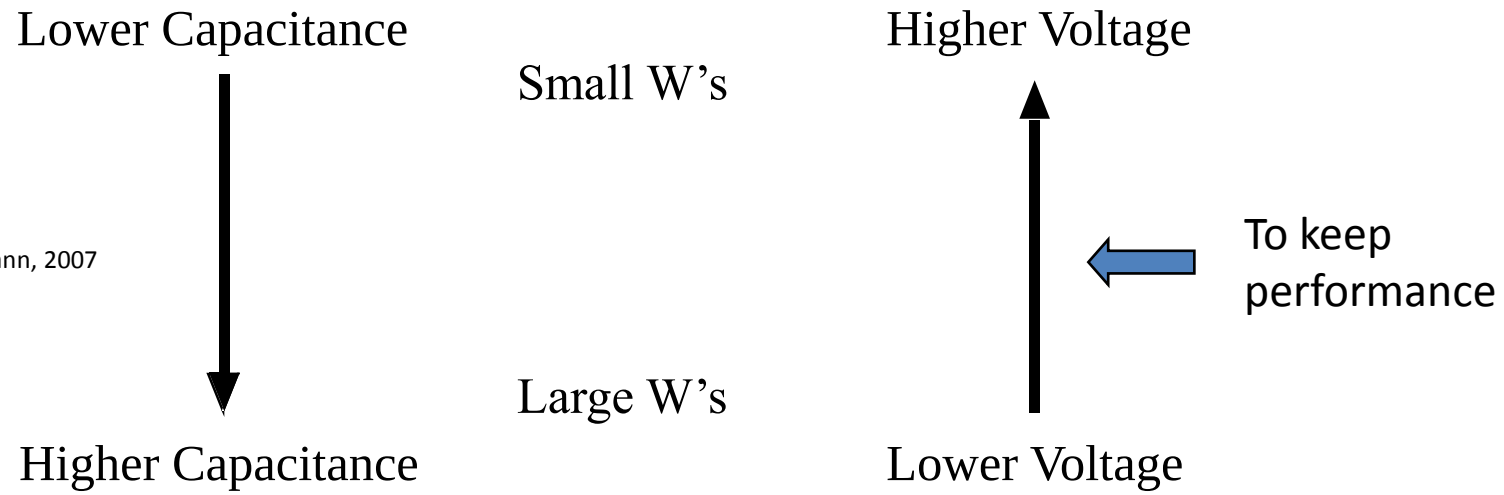
Low Power Design

- Reduce dynamic power
  - α: clock gating, sleep mode
  - C: small transistors (esp. on clock), short wires
  - V_{DD}: lowest suitable voltage
  - f: lowest suitable frequency
- Reduce static power
  - Selectively use ratioed circuits
  - Selectively use low V_t devices
  - Leakage reduction:
    stacked devices, body bias, low temperature

Lowering Dynamic Power

- Reducing V_{DD} has a quadratic effect!
  - Has a negative effect on performance especially as V_{DD} approaches $2V_T$
- Lowering C_L
  - Improves performance as well
  - Keep transistors minimum size
- Reducing the switching activity, $f_{0\rightarrow1} = P_{0\rightarrow1} * f$
  - A function of signal statistics and clock rate
  - Impacted by logic and architecture design decisions

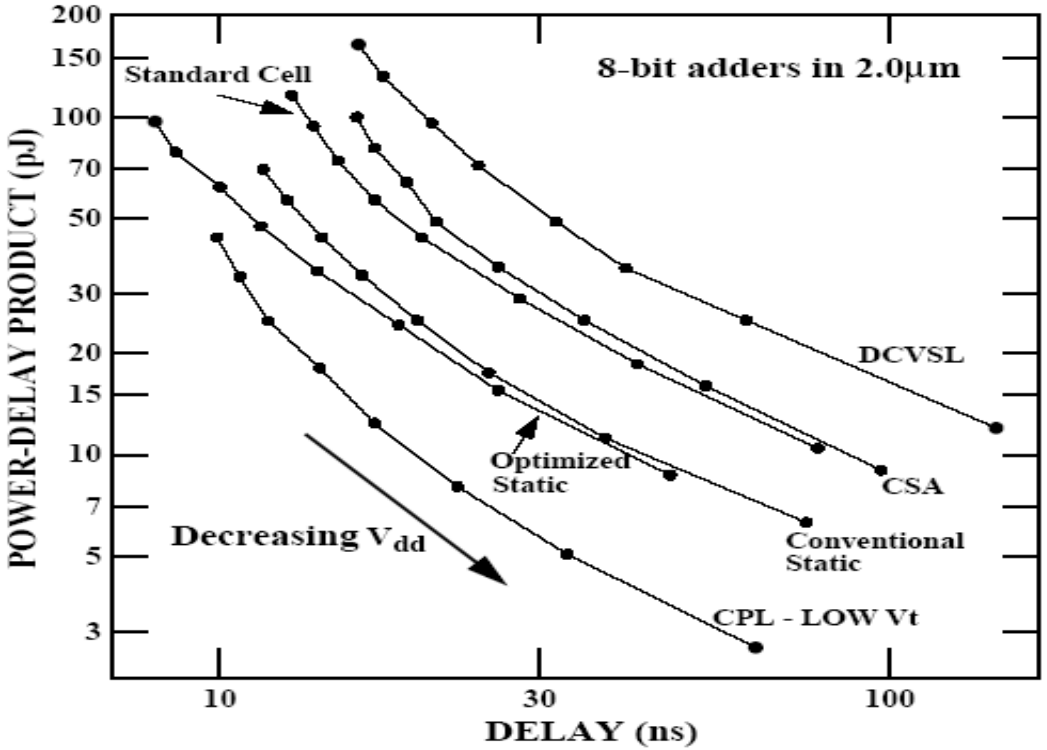
Transistor Sizing for Power Minimization



Source: Timmernann, 2007

- Larger sized devices: only useful only when interconnects dominate
- Minimum sized devices: usually optimal for low-power

Logic Style and Power Consumption



Source: Timmernann, 2007

- Voltage decreases: Power-delay product improves
- Best logic style minimizes power-delay for a given delay constraint

➔ New Logic style can reduced Power dissipation (if possible / available !)

Thank You