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NPTEL ONLINE CERTIFICATION COURSE

MICROELECTRONICS: DEVICES TO CIRCUITS

CMOS INVERTER BASICS - III

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Sizing of Inverter chain

The optimum size of each inverter is the geometric mean of its neighbors sizes :

$$C_{gin,j} = \sqrt{C_{gin,j-1} C_{gin,j+1}}$$

This means that each inverter is sized up by the factor f with respect to the preceding gate, has the same effective fan-out (f_j=f),

$$f = \sqrt[N]{C_L / C_{g,1}} = \sqrt[N]{F}$$

The minimum delay through the chain as

$$t_p = N t_{p0} (1 + \sqrt[N]{F} / \gamma)$$

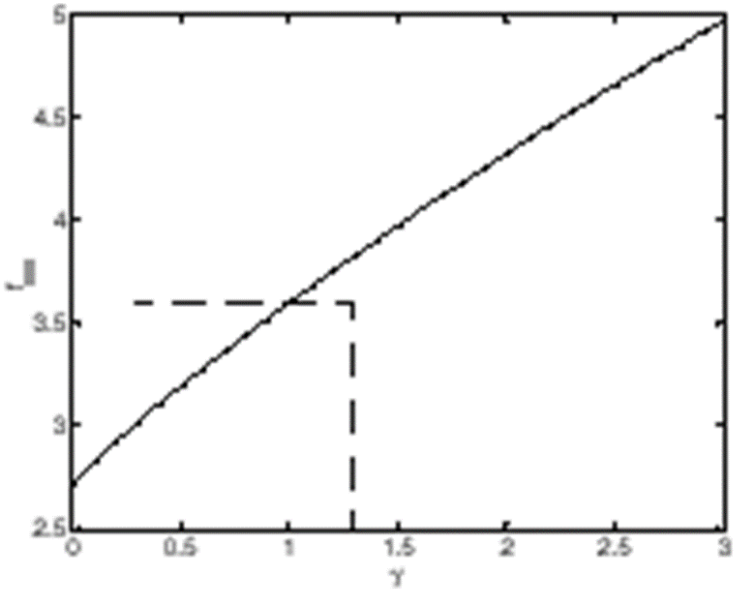
F represents the over all effective fan-out of the circuit.

Choosing right number of stages

The optimum value of right number of stages can be found by differentiating the minimum delay expression be the number of stages and setting the result to 0.

We get $\gamma + \sqrt[N]{F} - \frac{\sqrt[N]{F}}{N} = 0$

In common practice, optimum fan-out could be selected as 4



Source :Digital Integrated Circuits (2nd Edition)- Jan M. Rabaey

Power Dissipation –Dynamic power

- Power dissipation during switching activity
- Energy taken from supply voltage = E_{VDD}

$$E_{VDD} = \int_0^{\infty} i_{VDD}(t)\, V_{DD}\, dt = C_L V_{DD} \int_0^{VDD} dv_{out} = C_L V_{DD}^2$$

- Energy stored/removed on the load capacitor = E_C

$$E_C = \int_0^{\infty} i_{VDD}(t) v_{out} dt = C_L \int_0^{VDD} v_{out} dv_{out} = \frac{C_L V_{DD}^2}{2}$$

This is independent of transistor size.

If the switching activity is $f_{0\to1}$ times per second

$$P_{dyn} = C_L V_{DD}^2 f_{0\to1}$$

Power Dissipation – Direct path currents

- Finite value of rise time and fall time of input signal cause a direct path between V_{DD} and GND, while PMOS and NMOS are conducting simultaneously.

$$E_{dp} = V_{DD}\frac{I_{peak}t_{sc}}{2} + V_{DD}\frac{I_{peak}t_{sc}}{2} = t_{sc}V_{DD}I_{peak}$$

- Average power consumption

$$\boxed{P_{dp} = t_{sc}V_{DD}I_{peak}f}$$

Where, t_{sc}= time both devices are conducting

Power Dissipation – Static power dissipation

This is the steady state power dissipation, when no switching activity is present

$$P_{stat} = I_{stat} V_{DD}$$

Source of leakage current :

- Reverse bias diode junction of the transistors, located between source or drain and body. Thermally generated carriers may affect the junction leakage current.
- Sub-threshold leakage current when $V_{GS} < V_T$
- Choice of threshold voltage is a trade off between performance and static power consumption

$$P_{tot} = P_{dyn} + P_{dp} + P_{stat} = (C_L V_{DD}^2 + V_{DD} I_{peak} t_s) f_{0\rightarrow 1} + V_{DD} I_{leak}$$

Power Delay Product and Energy Delay Product

Power-delay Product : It represents the average energy consumption per switching events.

$$PDP = C_L V_{DD}^2 f_{max} t_p = \frac{C_L V_{DD}^2}{2}$$

Because, $f_{max} = \frac{1}{2t_p}$

This value can be arbitrary by changing the V_{DD} .

Energy-Delay Product : This performance matrix combines the performance and energy.

$$EDP = PDP \times t_p = \frac{C_L V_{DD}^2}{2} t_p$$

Techniques for Reducing Power Dissipation

- Reduce supply voltage
- Reduce switching activity
- Reduce physical capacitances

Recapitulation

- Propagation delay is the time to charge or discharge of the load capacitance.
- Optimum ratio of NMOS-to-PMOS is required to find out minimum propagation delay.
- The intrinsic delay is independent of transistor sizing and depends on the technology parameter and physical layout
- In very charging or discharging of inverter, only one half of the energy stored or removed in load capacitance respectively. Other half is dissipated by PMOS or NMOS.
- Power consumption is dissipated by the dynamic power during the switching period.

Thank You