IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

# MICROELECTRONICS: DEVICES TO CIRCUITS

## CMOS INVERTER BASICS - I

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# Outline

- Basic idea of CMOS inverter
- Switch model of inverter
- Static behavior
- Voltage transfer characteristics
- Switching threshold
- Noise margin
- Gain calculation

# CMOS INVERTER - Basic Idea

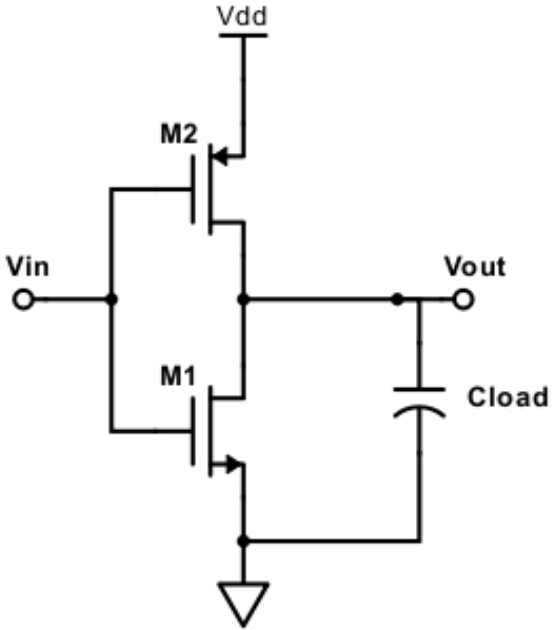
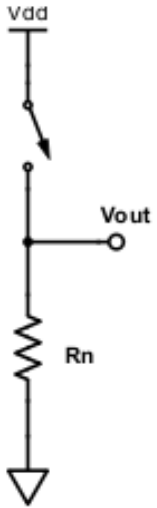


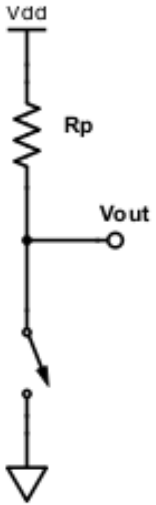

Figure : A static inverter with capacitive load

# CMOS INVERTER – switch model

When, Vin = Vdd,
NMOS is on,
PMOS is off,




When, Vin = 0,
NMOS is off,
PMOS is on,



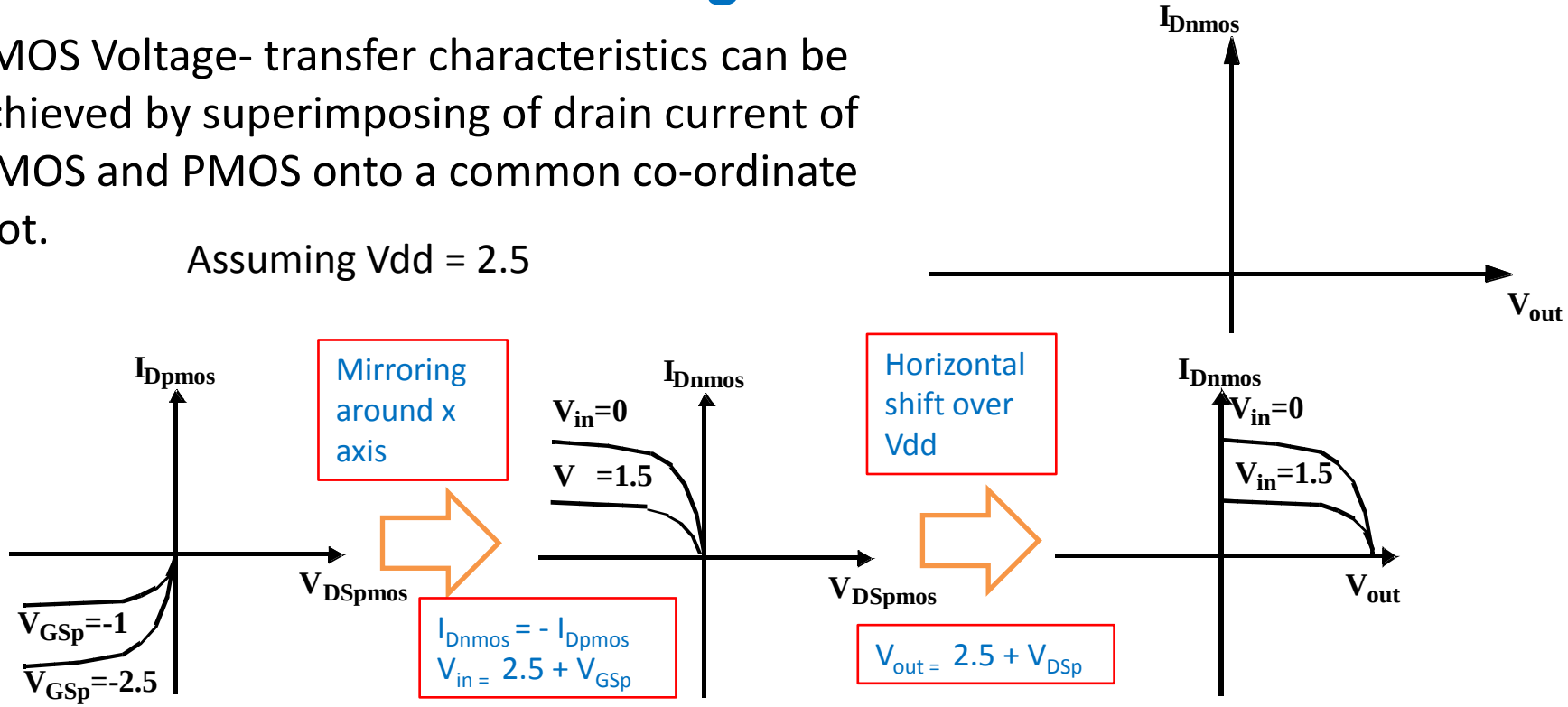
# CMOS INVERTER – static behavior

- High Noise margin, ideally equal to supply voltage
- Ratio-less logic level
- Low output impedance - less prone to noise
- High impedance - improve fanout
- No static power consumption

# CMOS INVERTER – voltage-transfer characteristics

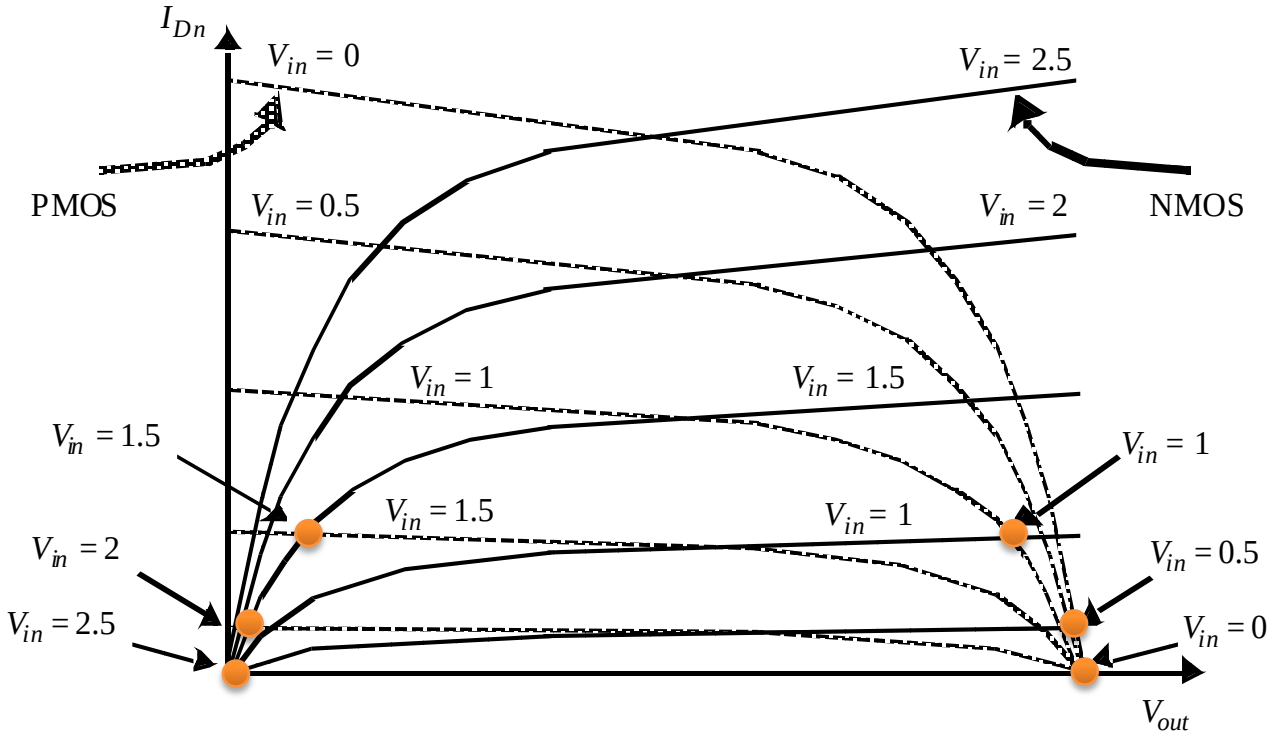
- CMOS Voltage- transfer characteristics can be achieved by superimposing of drain current of NMOS and PMOS onto a common co-ordinate plot.

Assuming Vdd = 2.5



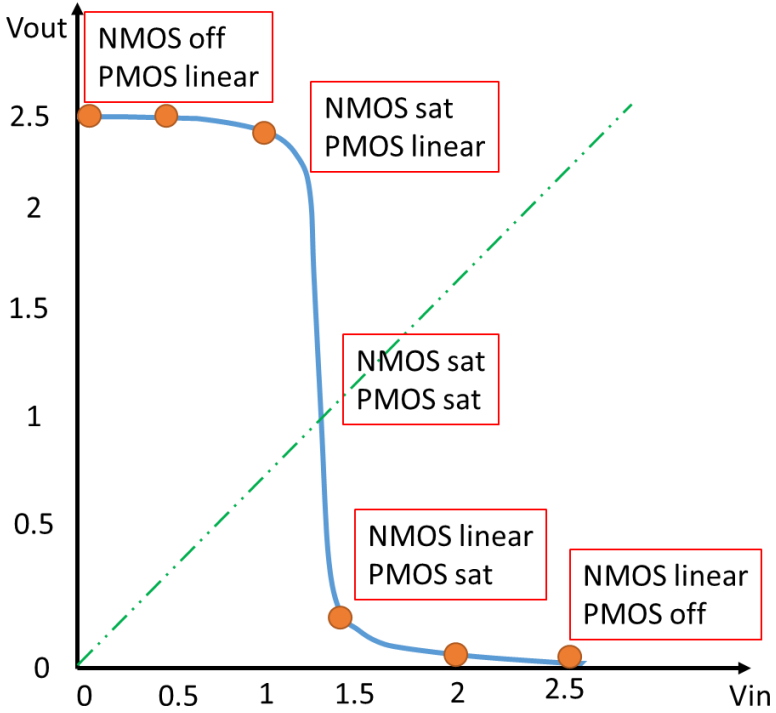

Transforming the PMOS I-V transfer characteristics onto same coordinate

# CMOS INVERTER – voltage-transfer characteristics




**Source: Digital Integrated Circuits (2nd Edition)- Jan M. Rabaey**

# CMOS INVERTER – voltage-transfer characteristics



# CMOS INVERTER – switching threshold

- Switching threshold $V_M$ can be obtained from the VTC graph, where $V_{in} = V_{out}$
- At this point both transistors are in saturation region.
- By ignoring channel length modulation, we can equate the transistor currents

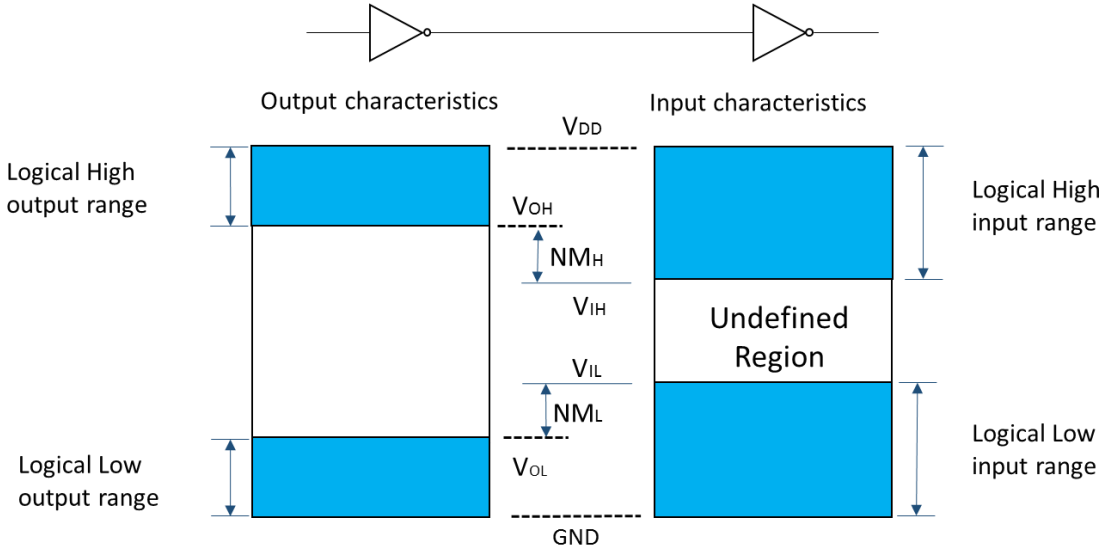
$$k_n V_{DSATn}\left(V_M - V_{Tn} - \frac{V_{DSATn}}{2}\right) + k_p V_{DSATp}\left(V_M - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right) = 0$$

$$V_M = \frac{\left(V_{Tn} + \frac{V_{DSATn}}{2}\right) + r\left(V_{DD} + V_{Tp} + \frac{V_{DSATp}}{2}\right)}{1 + r}$$

Where, $r = \frac{k_p V_{DSATp}}{k_n V_{DSATn}} = \frac{\upsilon_{satp} W_p}{\upsilon_{satn} W_n}$

# CMOS INVERTER – noise margin

- The characteristic of inverter which defines the allowable noise voltage on the input of gate so that output will not be affected.
- The noise margin of an inverter is defined by Noise Margin Low ($NM_L$) and Noise Margin High ($NM_H$).




$$NM_L = V_{IL} - V_{OL}$$
$$NM_H = V_{OH} - V_{IH}$$

In this case,

$$V_{OH} = V_{DD}$$
$$V_{OL} = 0$$

$$NM_L = V_{IL}$$
$$NM_H = V_{DD} - V_{IH}$$

# CMOS INVERTER – calculation of $V_{IL}$

By Definition, when $V_{in} = V_{IL}$, NMOS is in saturation region and PMOS is in linear region.

Also, $\frac{dV_{out}}{dV_{in}} = -1$ and $I_{Dn} = I_{Dp}$ So, $\frac{K_n}{2}(V_{GSn} - V_{Tn})^2 = \frac{K_p}{2}[2(V_{GSp} - V_{Tp})V_{DSp} - V_{DSp}^2]$

We know, $V_{GSp} = V_{in} - V_{DD}$ and $V_{DSp} = V_{out} - V_{DD}$

$$\frac{K_n}{2}(V_{in} - V_{Tn})^2 = \frac{K_p}{2}[2(V_{in} - V_{DD} - V_{Tp})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2]$$

Taking derivative w.r.t $V_{in}$ in both side to satisfy $V_{IL}$ condition.

$$\frac{K_n}{2}(V_{in} - V_{Tn}) = \frac{K_p}{2}[(V_{in} - V_{DD} - V_{Tp})(\frac{dV_{out}}{dV_{in}}) + (V_{out} - V_{DD}) - (V_{out} - V_{DD})(\frac{dV_{out}}{dV_{in}})]$$

# CMOS INVERTER – calculation of $V_{IL}$

$$\frac{K_n}{2}(V_{in} - V_{Tn}) = \frac{K_p}{2}[(V_{in} - V_{DD} - V_{Tp})(\frac{dV_{out}}{dV_{in}}) + (V_{out} - V_{DD}) - (V_{out} - V_{DD})(\frac{dV_{out}}{dV_{in}})]$$

Putting, $V_{in} = V_{IL}$ and $\frac{dV_{out}}{dV_{in}} = -1$

$$\frac{K_n}{2}(V_{IL} - V_{Tn}) = K_p(2V_{out} - V_{IL} + V_{Tp} - V_{DD})$$

$$V_{IL} = \frac{2V_{out} + V_{Tp} - V_{DD} + K_R V_{Tn})}{1 + K_R}$$

Where, $K_R = \frac{K_n}{K_p}$

# CMOS INVERTER – calculation of $V_{IH}$

Similarly, when $V_{in} = V_{IH}$ , NMOS is in linear region and PMOS is in saturation region.

$$\frac{K_p}{2}(V_{GSp} - V_{Tp})^2 = \frac{K_p}{2}[2(V_{GSn} - V_{Tn})V_{DSn} - V_{DSn}^2]$$

$$\frac{K_p}{2}(V_{in} - V_{DD} - V_{Tp})^2 = \frac{K_n}{2}[2(V_{in} - V_{Tn})V_{out} - V_{out}^2]$$

Taking derivative w.r.t $V_{in}$ in both side to satisfy $V_{IH}$ condition.

$$K_p(V_{in} - V_{DD} - V_{Tp}) = K_n[(V_{in} - V_{Tn})(\frac{dV_{out}}{dV_{in}}) + V_{out} - V_{out}(\frac{dV_{out}}{dV_{in}})]$$

# CMOS INVERTER – calculation of $V_{IH}$

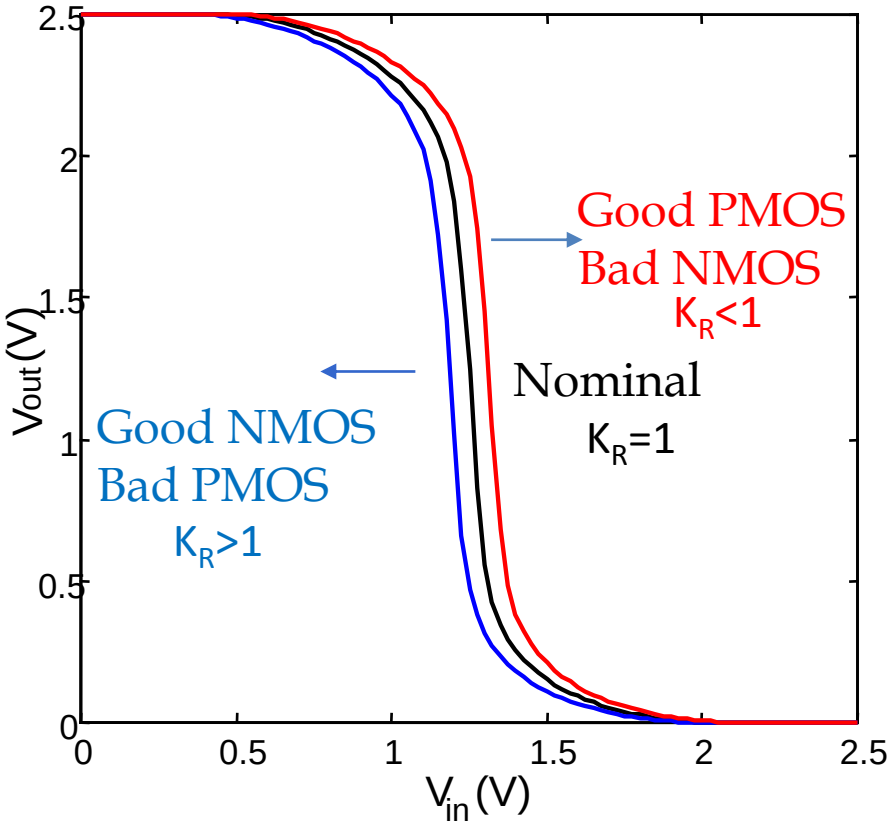
$$K_p(V_{in} - V_{DD} - V_{Tp}) = K_n[(V_{in} - V_{Tn})(\frac{dV_{out}}{dV_{in}}) + V_{out} - V_{out}(\frac{dV_{out}}{dV_{in}})]$$

Putting, $V_{in} = V_{IH}$ and $\frac{dV_{out}}{dV_{in}} = -1$

$$K_p(V_{IH} - V_{DD} - V_{Tp}) = K_n(-V_{IH} + V_{Tn} + 2V_{out})$$

$$V_{IH} = \frac{V_{DD} + V_{Tp} + K_R(2V_{out} + V_{Tn})}{1 + K_R}$$

# CMOS INVERTER – VTC w.r.t process variation parameter




Where, $K_R = \frac{K_n}{K_p}$

# CMOS INVERTER – voltage gain

- During transition region, both NMOS and PMOS are in saturation region.
- In order to calculate the gain in this region , channel length modulation can not be ignored.

$$K_n V_{DSATn}\left(V_{in} - V_{Tn} - \frac{V_{DSATn}}{2}\right)(1 + \lambda_n V_{out}) + K_p V_{DSATp}\left(V_{in} - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)$$
$$(1 + \lambda_p V_{out} - \lambda_p V_{DD}) = 0$$

Differentiating and solving for $dV_{out}/dV_{in}$

$$\frac{dV_{out}}{dV_{in}} = \frac{K_n V_{DSATn}(1 + \lambda_n V_{out}) + K_p V_{DSATp}(1 + \lambda_p V_{out} - \lambda_p V_{DD})}{\lambda_n K_n V_{DSATn}(V_{in} - V_{Tn} - \frac{V_{DSATn}}{2}) + \lambda_p K_p V_{DSATp}\left(V_{in} - V_{DD} - V_{Tp} - \frac{V_{DSATp}}{2}\right)}$$

# CMOS INVERTER – voltage gain

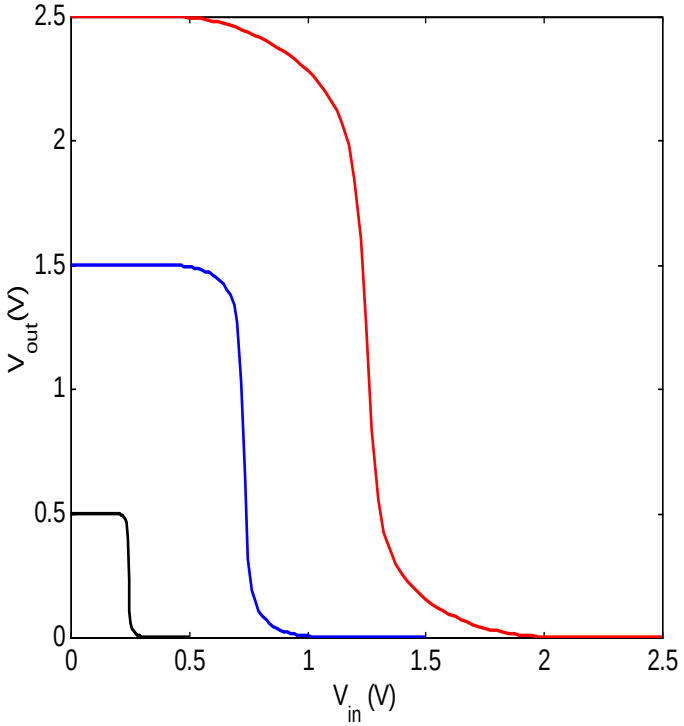
Ignoring second order term and setting $V_{in}=V_M$

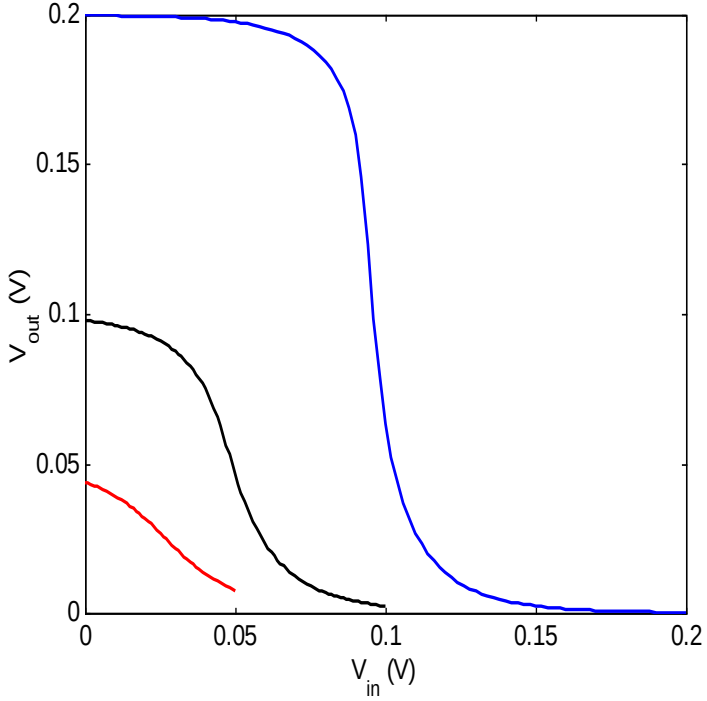
$$g = -\frac{1}{I_D(V_M)}\frac{K_n V_{DSATn} + K_p V_{DSATp}}{\lambda_n - \lambda_p}$$

$$\approx \frac{1+r}{(V_M - V_{Tn} - V_{DSATn}/2)(\lambda_n - \lambda_p)}$$

- Gain is almost purely determined by the technology parameter
- It is slightly depends on the transistor sizing ratio.

# CMOS INVERTER – voltage gain




Adapted from Digital Integrated Circuits (2nd Edition)- Jan M. Rabaey

# Recapitulation

- CMOS inverter consists of pull-up PMOS block and pull-down NMOS block.
- A ideal inverter exhibits high input impedance and low output impedance, typically in kilo ohm.
- The logic swing is equal to supply voltage and does not depends upon device relative device size.
- Gain of inverter is function of technology parameter.

# Thank You