IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

MICROELCTRONICS: DEVICES TO CIRCUITS

MOS Parasitics and SPICE Model

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Outline

- MOS Structure Capacitance
  - MOS Overlap Capacitance
  - Channel Capacitance
  - Junction Capacitance
- Source-Drain Resistance
- SPICE Model for MOS
- Equivalent Structure of SPICE Models
- Model Equations of LEVEL-1, LEVEL-2 and LEVEL-3
- Recapitulation

MOS Structure Capacitance

- The dynamic response of MOSFET is related to the time taken to (dis)charge its intrinsic capacitance and extra capacitance introduced by connecting wires and load.

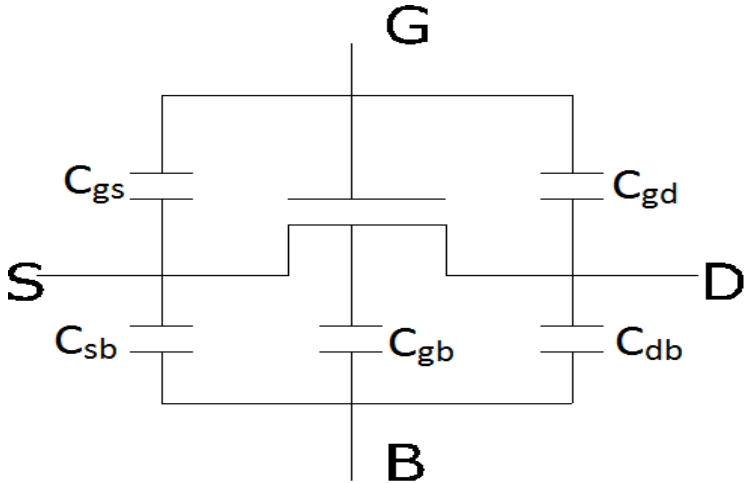
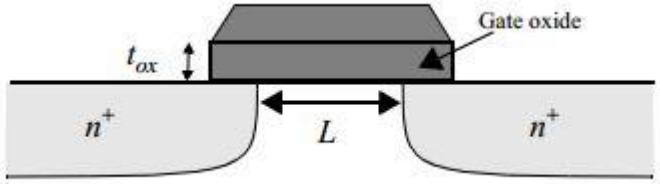
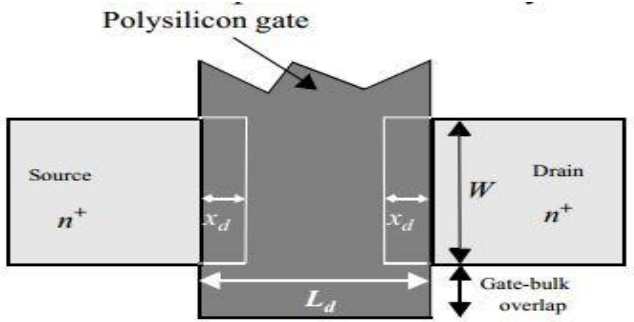


Figure :MOS Capacitance Model

MOS Overlap Capacitance





- Ideally, the source and drain diffusion takes place right at the edge of gate oxide, but practically it diffuses below the gate oxide with lateral diffusion of x_d.

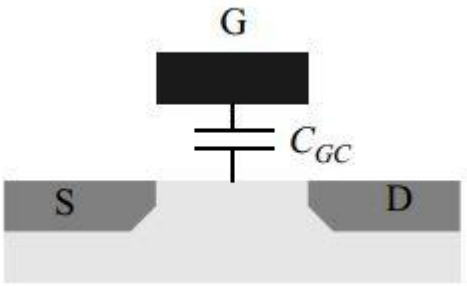
$$C_{gs0} = C_{gd0} = C_{ox} x_d W$$

where $C_{ox} = \varepsilon_{ox} / t_{ox}$ is a capacitance formed due to gate oxide.

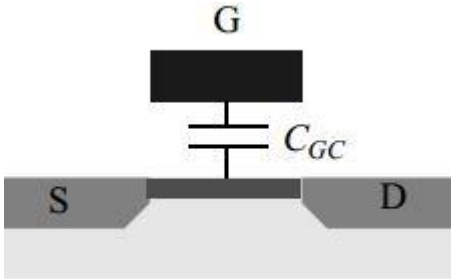
Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Channel Capacitance

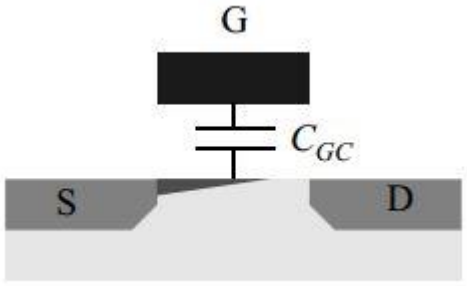
- The most significant parasitic MOS components are channel capacitance, which consists of C_{gcs} (gate-source), C_{gcd} (gate-drain) and C_{gcb}(gate-body).
- These capacitances are dependent on region of operation and applied terminal voltages.



Cut-off region



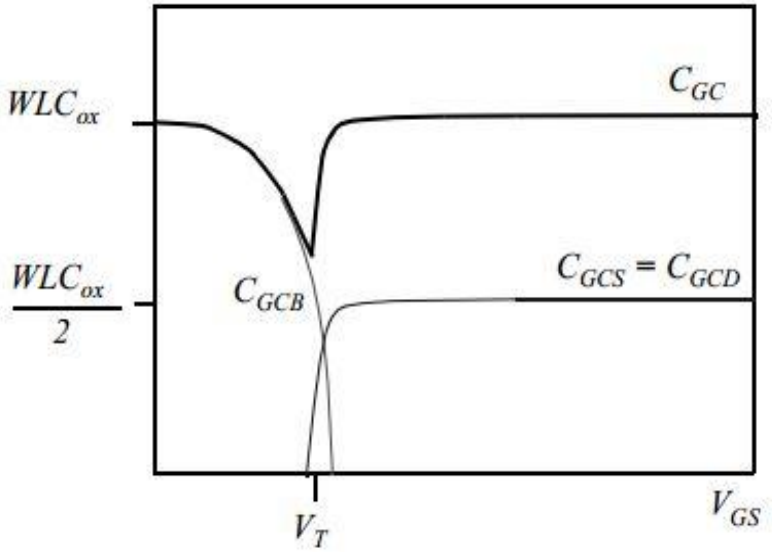
Resistive region



Saturation region

Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

- In cut-off region, there is no channel charge, hence total gate capacitance appears between gate and body.
- In resistive region, an inversion layer is formed, hence C_{gcb}=0. Therefore, total gate capacitance is distributed equally between source and drain.
- In saturation region, the pinch-off occurs at drain end, hence all the capacitance is due to gate and source.

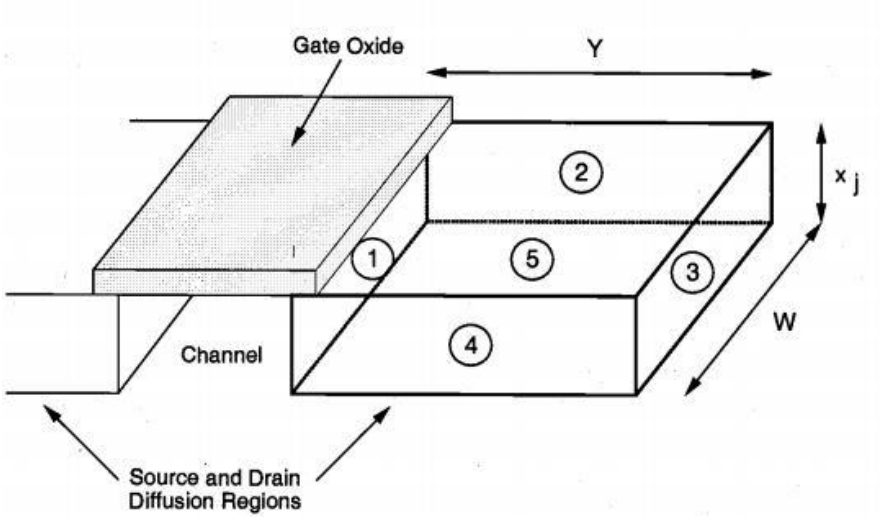


Channel Capacitance (C_{GC}) as a function of V_{GS} with V_{DS}=0.

Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Junction Capacitance

- Due to presence of depletion region at source and drain side, the junction capacitances come into picture.



Source: S. M. Kang and Y. Leblebici, “CMOS Digital Integrated Circuits,” McGraw Hill Pvt. Ltd., 2003.

- Various regions forming a p-n junction is contributing in total junction capacitance.
- Expression of Junction Capacitance-

$$C_j(V)=A\sqrt{\frac{\varepsilon q}{2}\left(\frac{N_a N_d}{N_a+N_d}\right)}\frac{1}{\sqrt{(\phi_0-V)}}$$

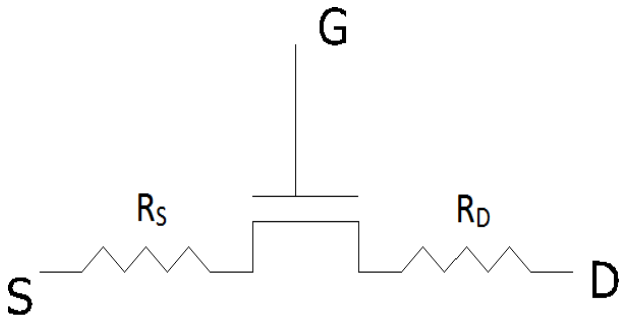
where N_a, N_d are doping concentration, ϕ_0 is built-in potential and V is applied bias

$$C_j(V)=\frac{AC_{jo}}{\left(1-\frac{V}{\phi_o}\right)^m}$$

Source-Drain Resistance

- Another parasitic component which affects the performance is the resistance in series with source and drain.
- This effect is more pronounced in smaller feature size.

$$R_{S,D} = \frac{L_{S,D}}{W} R_{sheet} + R_C$$



where R_{sheet} and R_C is the sheet and contact resistance respectively.

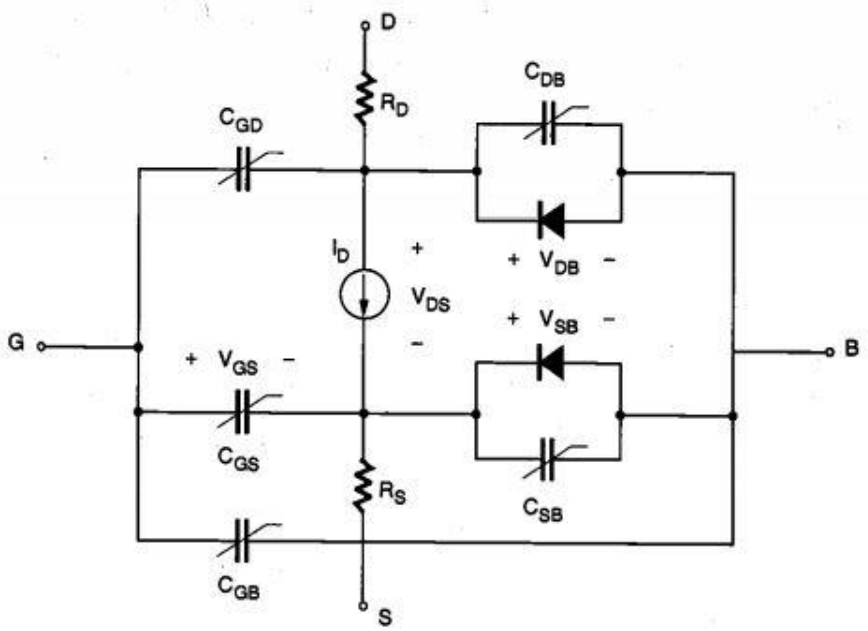
SPICE Model for MOS

- SPICE is a general purpose circuit simulator.
- SPICE has three built-in MOSFET models-

1. Level-1 (MOS1)-described by square law of I-V characteristics.
2. Level-2 (MOS2)-detailed analytical MOSEFT model
3. Level-3 (MOS3)-a semi-empirical model.

- Second order effects such as SCEs are included in MOS2 and MOS3 models.
- MOS models can be included by .MODEL statement in a particular simulation.

Equivalent structure of SPICE Models



- For PMOS the direction of current source, polarity of voltages and polarity of diodes must be reversed.

Source: S. M. Kang and Y. Leblebici, “CMOS Digital Integrated Circuits,” McGraw Hill Pvt. Ltd., 2003.

LEVEL-1 SPICE Model Equations

- In linear region- $I_D = \frac{k'}{2}\frac{W}{L_{eff}}[2(V_{GS}-V_T)V_{DS}-V_{DS}^2](1+\lambda V_{DS})$

- In Saturation region- $I_D = \frac{k'}{2}\frac{W}{L_{eff}}(V_{GS}-V_T)^2(1+\lambda V_{DS})$

To maintain the continuity at the linear-saturation region boundary, $(1+\lambda V_{DS})$ term is included in both the equation.

- Five electrical parameters i.e. k', V_T, λ, V_{TH} and Φ completely characterizes this model.

LEVEL-2 SPICE Model Equations

- To obtain more accurate current equation the voltage dependent bulk charge must be taken into account.

$$I_D = \frac{k'}{(1-\lambda V_{DS})}\frac{W}{L_{eff}}\left\{\left(V_{GS}-V_{FB}-|2\Phi_F|-\frac{V_{DS}}{2}\right)V_{DS}-\frac{2}{3}\gamma\left[V_{DS}-V_{BS}+|2\Phi_F|\right]^{3/2}-\left(-V_{BS}+|2\Phi_F|\right)^{3/2}\right\}$$

- The saturation voltage is given by-

$$V_{DSAT}=V_{GS}-V_{FB}-|2\Phi_F|+\gamma^2\left[1-\sqrt{1+\frac{2}{\gamma^2}(V_{GS}-V_{FB})}\right]$$

- The saturation current is given by- $I_D = I_{DSAT}\left(1/(1-\lambda V_{DS})\right)$

LEVEL-3 SPICE Model Equations

- This level precisely includes the short channel effects. The majority of the equation of Level-3 are empirical.
- The current equation in linear region is expanded using Taylor series-

$$I_D = \mu_s C_{ox} \frac{W}{L_{eff}} \left(V_{GS} - V_T - \frac{1+F_B}{2} V_{DS} \right) V_{DS}$$

where $\left[F_B = \frac{\gamma F_S}{4\sqrt{|2\Phi_F| + V_{SB}}} + F_n \right]$ shows the dependence of bulk charge on the geometry and F_n includes the narrow channel effects.

Recapitulation

- The dynamic behaviour of MOSFET can be analyzed by the knowledge of its capacitance.
- SPICE is a general purpose circuit simulator.
- Three levels of MOS models are basically used in SPICE for simulating the MOSFET structure.
- LEVEL-2 and Level-3 models have includes the second order effect in it.

Thank You