IIT ROORKEE

NPTEL ONLINE CERTIFICATION COURSE

Microelectronics: Devices to Circuits

MOS TRANSISTOR BASICS - III

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Outline

- **Short Channel Effects**
- **Second Order Effects**
  - Body Effect
  - Channel Length Modulation
- **Types of Device Scaling**
  - Velocity Saturation
  - Drain Induced Barrier Lowering
  - Punchthrough
- **Model for manual analysis**
- **Basic Equations to be remembered**
- **Recapitulation**

Short Channel Effects

- What if the device dimension is reduced?

- **Moore's Law**-In 1965, Gordon **Moore** postulated that the number of transistors per unit area on integrated circuits will double every 18 months. **Moore's law** predicts that this trend will continue into the foreseeable future.

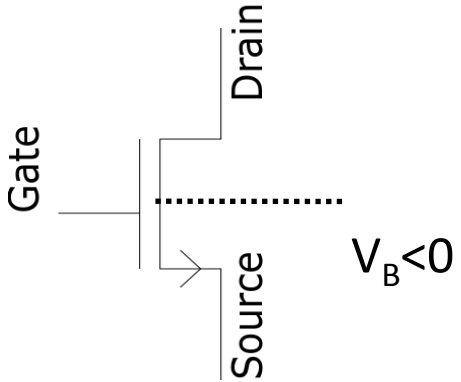
- What beyond the Moore's law?

Body Effect

- What happen if the body bias is applied?

➢ To keep the source and drain junctions remain reverse biased, we applied body voltage $V_B<0$.

○ This decreases the impact of gate-bias and hence increases the threshold voltage.



$$V_T = V_{TH} + \gamma\left(\sqrt{\left|2\Phi_F + V_{SB}\right|} - \sqrt{\left|2\Phi_F\right|}\right)$$

where $\gamma = \frac{\sqrt{2\varepsilon q N_{sub}}}{C_{ox}}$ is body coefficient and V_{SB} is source-body potential.

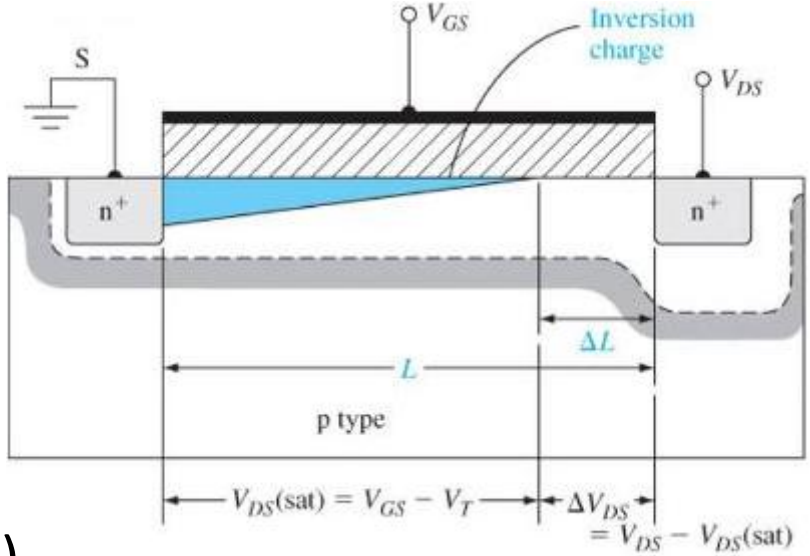
Channel Length Modulation (CLM)

- Does really MOSFET acts as a constant current source in its saturation region?

  - The effective channel length gets modulated by V_{DS}.
  - Drain current is given by-

$$I_D = \mu_n C_{OX} \frac{W}{2L} (V_{GS} - V_{TH})^2 (1 + \lambda V_{DS})$$

where λ is CLM parameter (empirical).



Source: Google Images

Types of Device Scaling

- Scaling of the device does not only mean the reduction of the Channel Length. It includes the proper scaling of all other device dimensions.

1. **Constant Field Scaling**-It yields the reduction in the power-delay product of the transistor. Hence, it requires the reduction in power supply for reduced feature size.
2. **Constant Voltage Scaling**-This is a preferred scaling technique as it provides voltage compatibility with other technologies. Due to this electric field gets higher in smaller devices which causes mobility degradation, velocity saturation etc.

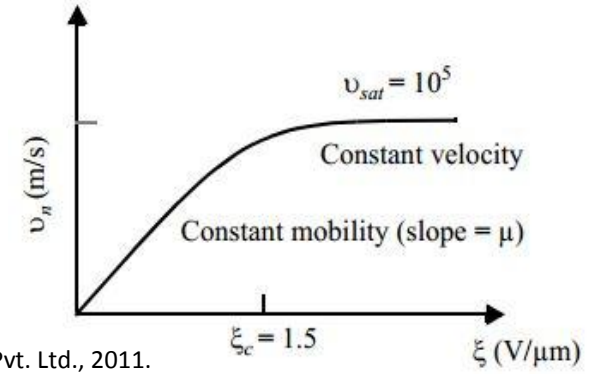
Velocity Saturation

- The velocity of the charge carriers is proportional to the electric field, independent of the value of that field (for Silicon). $V_d = \mu E$
- However, for short channel length, the horizontal field gets higher and this linear relationship is no longer valid. The velocity of the carriers gets saturated after reaching a critical field E_C.

$$V_d = \frac{\mu E}{1 + \frac{E}{E_c}} \qquad \text{for } E \le E_c$$

$$V_d = V_{sat} \qquad \text{for } E > E_c$$

where $E = V_{DS}/L$



Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

- The continuity between two regions dictates that $E_c = 2V_{sat}/\mu$. If we re-evaluate the drain current then-

$$I_D = \frac{\mu_n C_{OX}}{1+(V_{DS}/E_C L)} \frac{W}{L}\left[(V_{GS}-V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right] \quad \text{in resistive region}$$

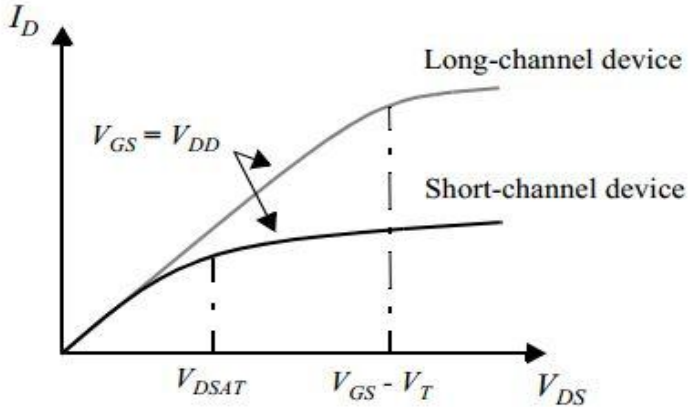
$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS}-V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]\kappa(V_{DS}) \quad \because \kappa(V_{DS}) = \frac{1}{1+(V_{DS}/E_C L)}$$

- For longer channel or smaller V_{DS}, κ approaches to 1.

- When V_{DS} increases then device entered into saturation region, so in the current equation V_{DS} get replaced by V_{DSAT}

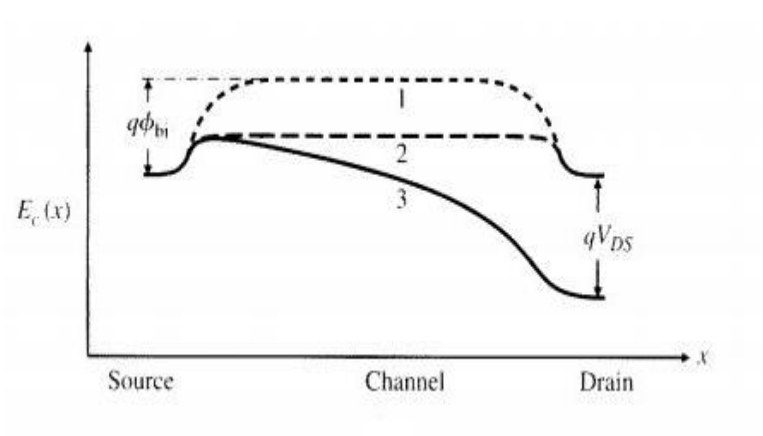
$$I_D = v_{sat} C_{ox} W(V_{GS} - V_{TH} - V_{DSAT})$$

$$I_D = \kappa(V_{DSAT}) \mu_n C_{OX} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$$

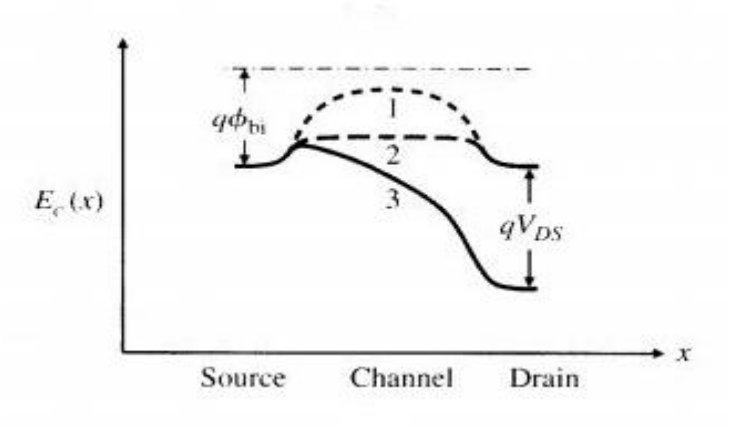


Source: J. M. Rabaey, A. Chandrakasan and B. Nikolic, "Digital Integrated Circuit," PHI Learning Pvt. Ltd., 2011.

Drain Induced Barrier Lowering (DIBL)



Long Channel Device

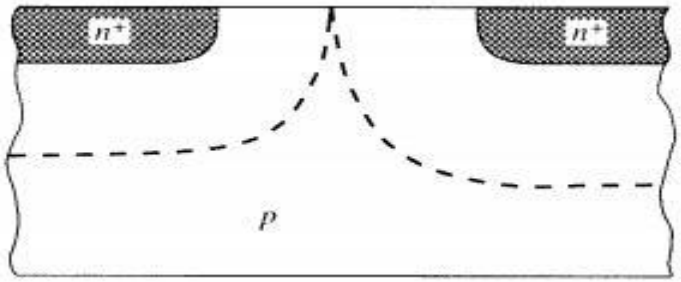


Short Channel Device

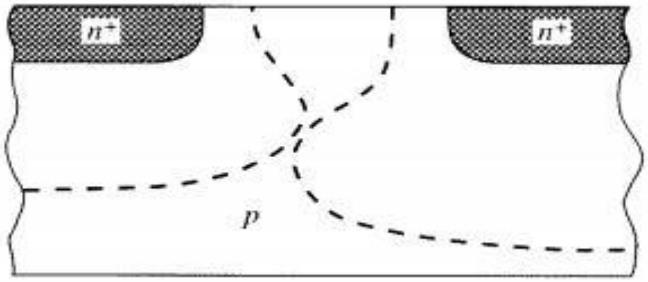
- Threshold voltage gets lower and become a function of $V_{DS.}$
- Even if CLM is ignored, the I_D does not get saturated due to DIBL as V_{DS} affects the charge distribution.

Source: Y. Tsividis and C. McAndrew, "The MOS Transistor," Oxford University Press, 2013.

Punch-through



Surface Punch-through



Bulk Punch-through

- The charge carrier flows directly from source to drain.
- The slope of $\log(I_D)$ gets higher by decreasing the channel length (L) to be too small. This does not allow the device to turned off even if V_{DS} is decreased significantly.

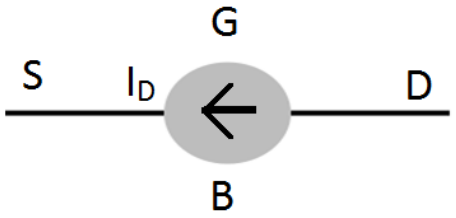
Source: Y. Tsividis and C. McAndrew, "The MOS Transistor," Oxford University Press, 2013.

Model for Manual Analysis

- All the second order effects influenced the device analysis, so to make it simpler we need simple and tangible analytical model.
- Let, this model considers the MOS device as a current source-

$$I_D = 0 \qquad \text{for } V_{GS} - V_T \le 0$$

$$I_D = k' \frac{W}{L} \left[(V_{GS} - V_T) V_{min} - \frac{V_{min}^2}{2} \right] (1 + \lambda V_{DS})$$



$$\text{with } V_{min} = \min[(V_{GS} - V_T), V_{DS}, V_{DSAT}]$$

Besides being a function of voltages, the current is also a function of process dependent parameters like k, λ, γ, V_{DSAT} and V_{TH}

Basic Equations to be remembered

- In Resistive Region, the drain current due to velocity saturation-

$$I_D = \mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DS} - \frac{V_{DS}^2}{2}\right]\kappa(V_{DS}) \qquad \because \kappa(V_{DS}) = \frac{1}{1+(V_{DS}/E_C L)}$$

- In Saturation Region, the drain current due to velocity saturation-

$$I_D = \kappa(V_{DSAT})\mu_n C_{OX} \frac{W}{L}\left[(V_{GS} - V_{TH})V_{DSAT} - \frac{V_{DSAT}^2}{2}\right]$$

$$I_D = v_{sat} C_{OX} W\left[V_{GS} - V_{TH} - \frac{V_{DSAT}}{2}\right]$$

Recapitulation

- The body bias plays a significant role in device analysis.
- The miniaturization leads to a several second order effects which increases the complexity of device analysis.
- Due to carrier velocity saturation, the drain current becomes the linear function of V_{GS}.
- What beyond the Moore's law? This is a vivid industry problem.

Thank You