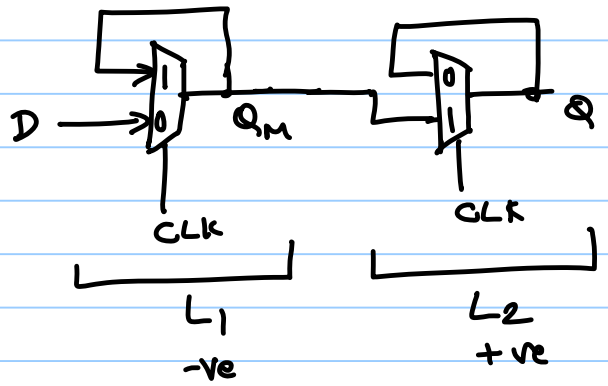
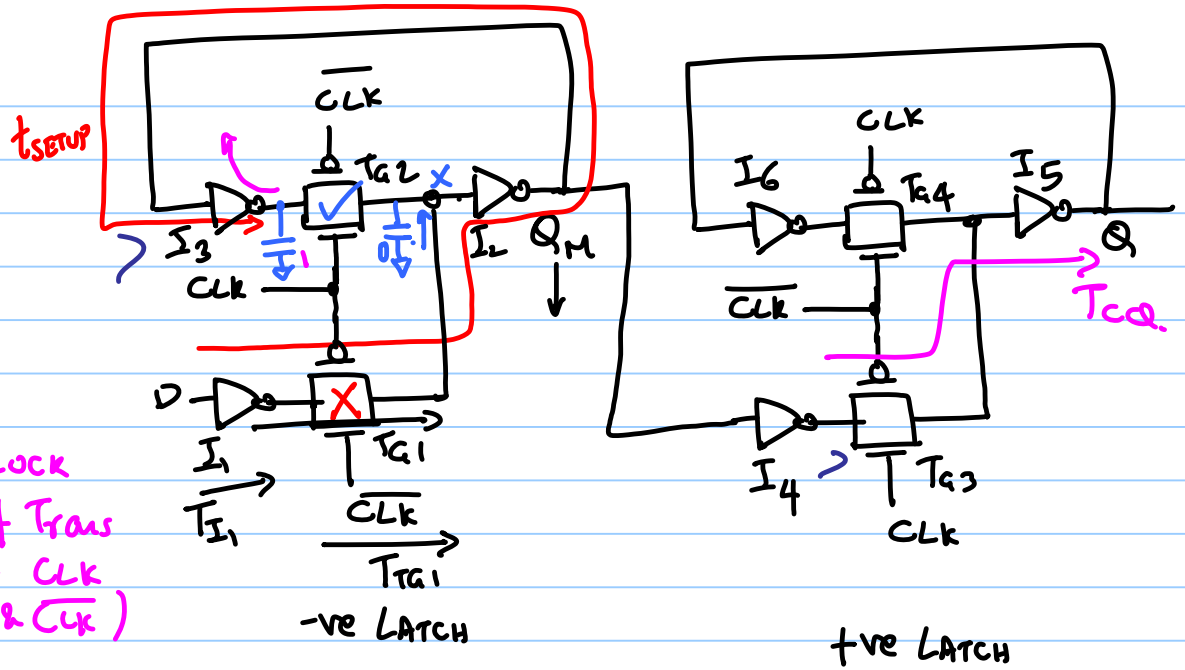
4/1/2019

EE5311

MODULE-5 - SEQUENTIAL CIRCUITS

+ve EDGE TRIG FLOP





PROBLEM:

LARGE CLOCK LOAD (4 Trans per CLK & $\overline{CLK}$)

$$T_{SETUP} = T_{I_1} + T_{TG1} + T_{I_2} + T_{I_3}$$

$$T_{CQ} = T_{TG3} + T_{I_5}$$

$$T_{HOLD} = 0 \quad (-T_{I_1})$$

DELAY ANALYSIS

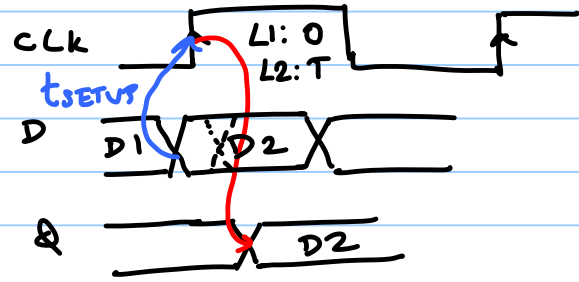
t_{SETUP} =

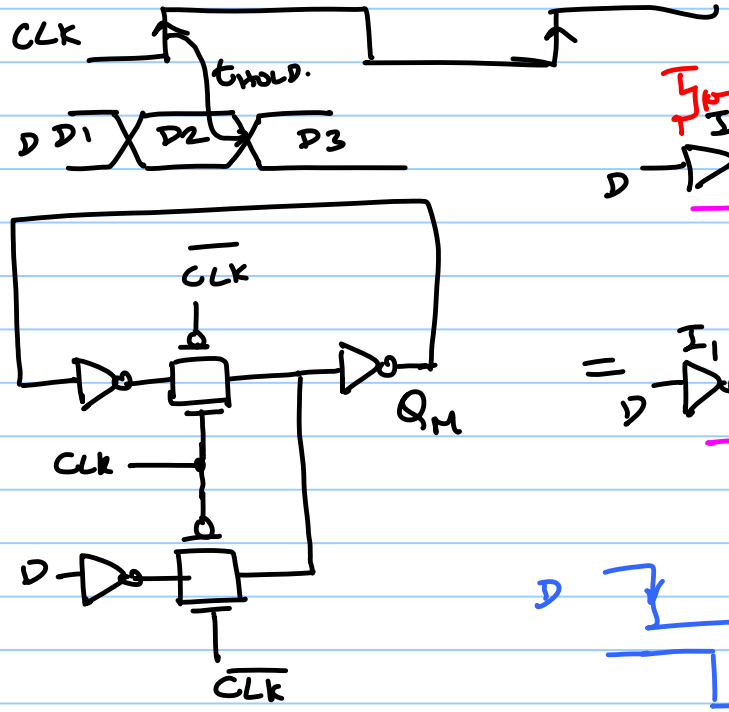
t_{HOLD} =

t_{CQ} =

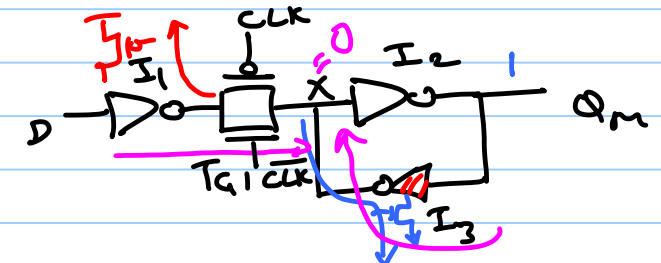
ASSUMPTION

1) CLK IS IDEAL
   ⇒ ZERO RISE & FALL TIME
2) NO CLK SKEW



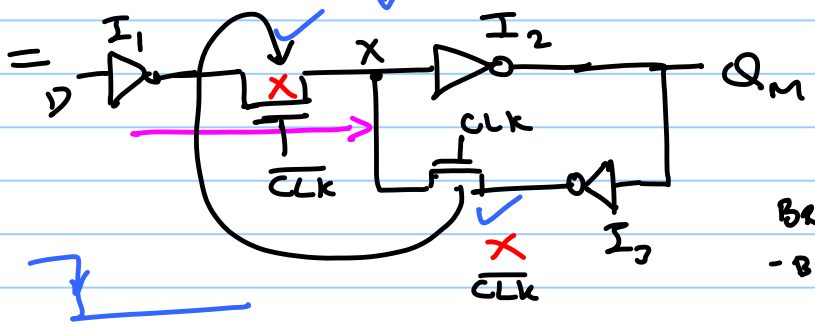


-ve LATCH



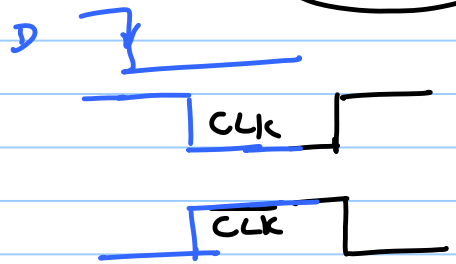
C2

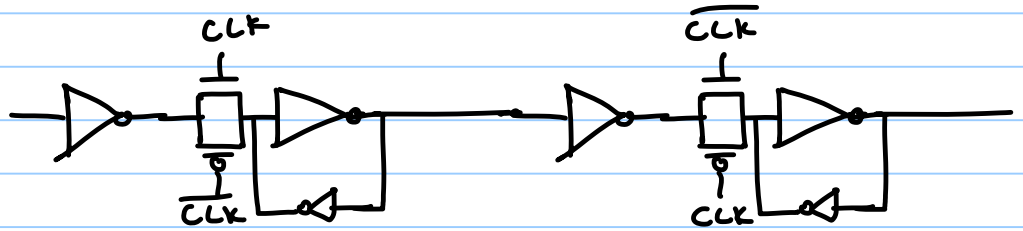
NOT BREAKING FB PATH

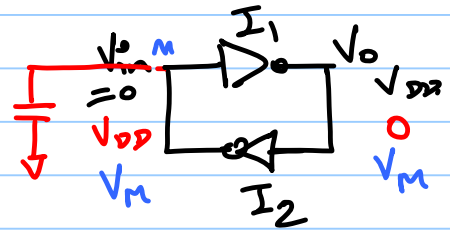


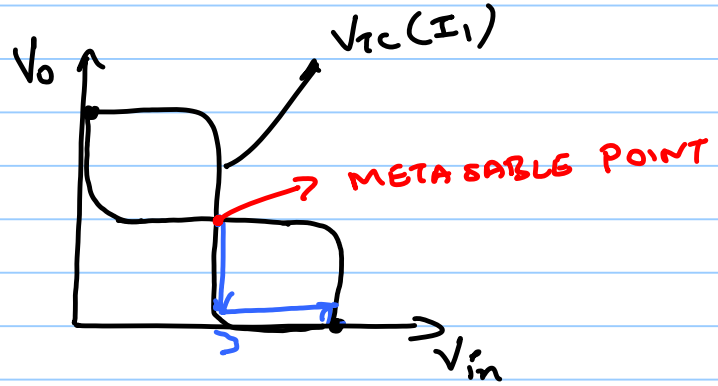
C1

BREAKING FEED-BACK PATH




CLK
CLK
CLK
CLK


M
I_1
V_o
V_{in}
=0
V_{DD}
V_M
0
V_M
I_2


V_o
$V_{TC}(I_1)$
METASABLE POINT
V_{in}