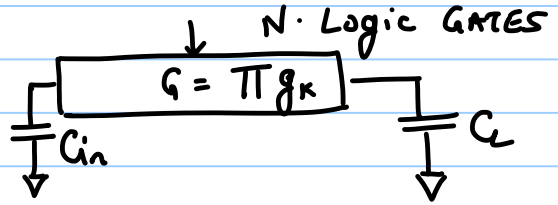
04/10/2019

EE5311

MODULE-4- COMBINATIONAL CIRCUITS

GATE SIZING:

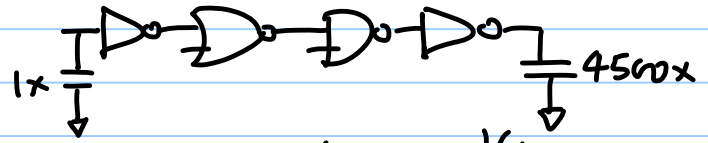


$$H = \frac{C_L}{C_{in}} = \Pi h_K.$$

$$F = GH$$

$$\text{OPTIMAL } f_K = F^{1/N}$$

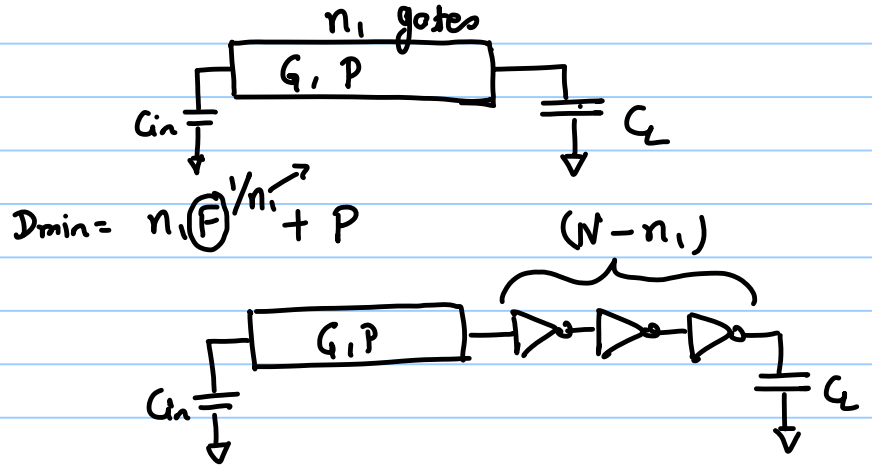
$$D_{min} = NF^{1/N} + P \rightarrow \Sigma p_i$$



$$f_{OPT} = (10000)^{1/4} = 10$$

$$D_{min} = 46.$$

Buffer Insertion



$D_{min} = n_1 F^{1/n_1} + P$

G, H, P

$F = G \cdot H$

$\hat{G}$ = New path Logical effort $= G \cdot \Pi g_{inv} = G$

$\hat{H}$ = New path electrical $\sim = H$

$$\hat{D}_{min} = N(\hat{G}\hat{H})^{1/N} + P + (N-n_1)p_{inv}$$

$$= N(F)^{1/N} + P + (N-n_1)p_{inv}$$

$\hat{P}$ = New parasitic effort $= P + (N-n_1)p_{inv}$

p_{inv} = Parasitic effort of inv $(=1)$

$\hat{F} = \hat{G}\hat{H} = GH = F$

$$\frac{\partial \hat{D}_{min}}{\partial N} = 0$$

$$\hat{D}_{min} = N F^{1/N} + (N - n_1) p_{inv} + P$$

$$\frac{\partial \hat{D}_{min}}{\partial N} = F^{1/N}(1) + N F^{1/N}\left(\frac{-1}{N^2}\right)\ln(F) + p_{inv}$$

$$\Rightarrow \left(F^{1/N}\right)\left(1 - \ln(F^{1/N})\right) + p_{inv} = 0$$

Let OPTIMAL STAGE EFFORT = $P = F^{1/N}$

$$\Rightarrow P(1 - \ln(P)) + p_{inv} = 0$$

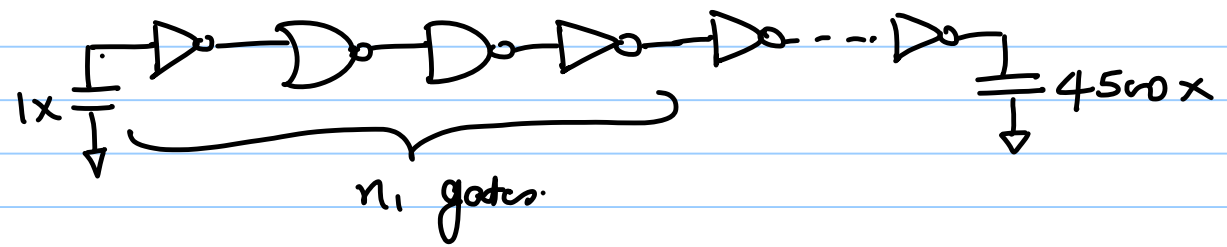
$$P(1 - \ln(P)) + 1 = 0$$

When $P = 3.59$

$\rho_{opt} = 3.59 \sim 4$

$\rho_{opt} = (F^{1/N}) \Rightarrow \quad 1 = \frac{1}{N} \log_{\rho_{opt}}(F)$

$\Rightarrow \quad \underline{N = \log_4(F)}$



$F = 10^4 = (20/9) \times 4500$

$N = \log_4(10^4) = 6.64$

POST BUFFERING: $N_{opt} = 6/7 \rightarrow 6$

$$D_{min} = 6 \times (10^4)^{1/6} + 6 + 2 \times 1$$

$$= 35.8$$