EE5311

MODULE - 4 - COMBINATONAL CIRCUITS

SYNTHESIS
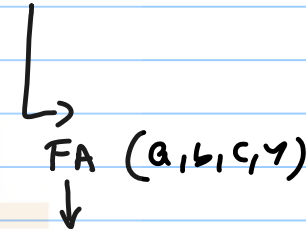
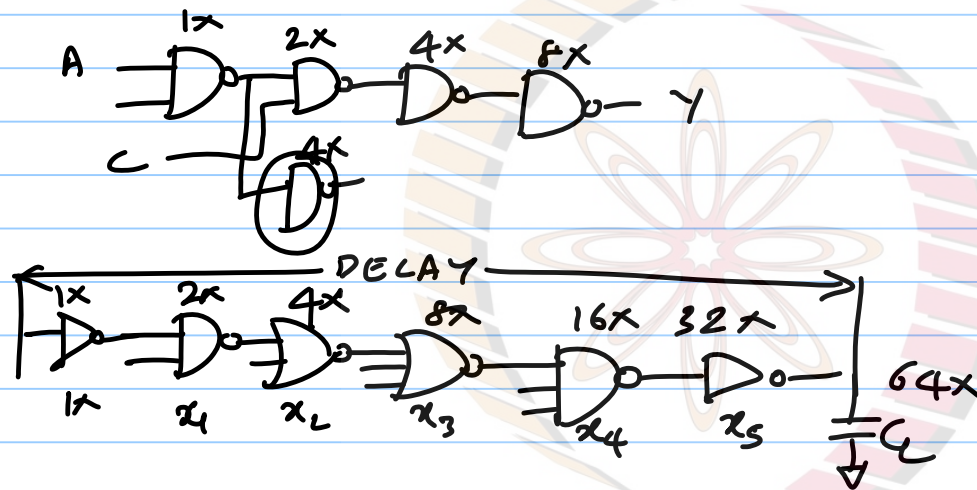module (a , b , c , y)

$y = a + b + c;$

VERILOG

STD CELL LIB

SYNTH
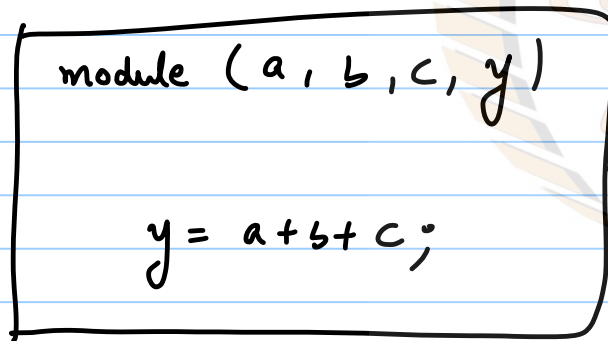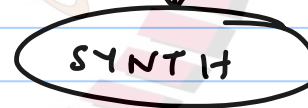
SPICE NETLIST

NAND2 (   )

NAND2 (   )

FA (a,b,c,y)   ⋮

NAND2 (   )

ESTIMATING GATE DELAY

ESTIMATING PATH DELAY

A
1x
2x
4x
8x
Y

C
4x

1x
2x
4x
8x
16x
32x
DELAY
1x
x_1
x_2
x_3
x_4
x_5
64x
C_L

1x

$32\lambda/2\lambda$

$16\lambda/2\lambda$

$16\lambda/2\lambda$

$8\lambda/2\lambda$
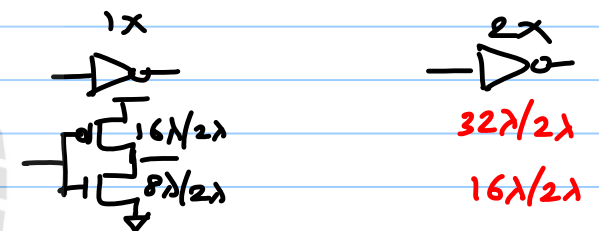
GATE DELAY OPTIMIZATION

1x
4096x
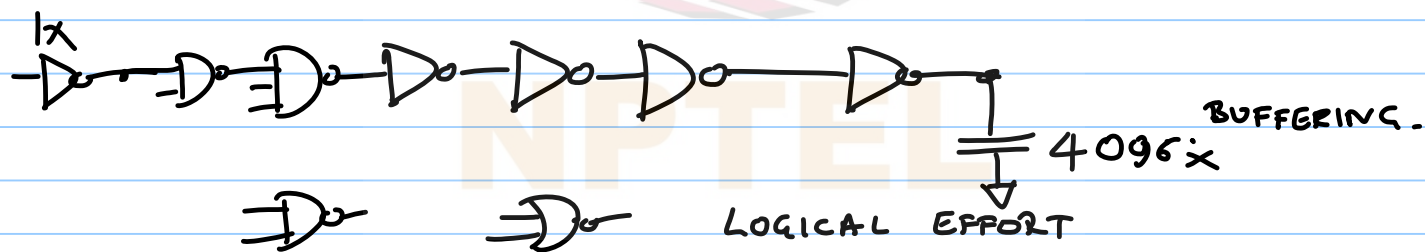
BUFFERING.

LOGICAL EFFORT

BASICS
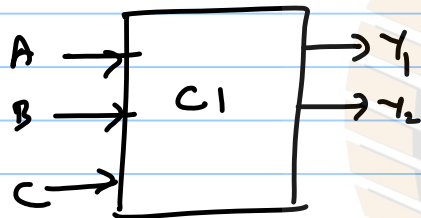
A	B	C	Y_1	Y_2
0	0	0	0	0
0	0	1	0	1
0	1	0	1	1
$\vdots$	$\vdots$			
1	1	1	1	0

$$Y_1 = \sum m(0,3,5) \;-\!\!?\;\Bigg\}$$

$$Y_2 = \sum m(1,2,7) \;-\;$$

SUM OF PRODUCTS.

$$Y_1 = \overset{0}{\overline{A}\,\overline{B}\,\overline{C}} + \overset{3}{\overline{A}BC} + \overset{5}{A\overline{B}C}$$

OR

ACTIVE HIGH SWITCHES

X —⊓_⊓_⊓— Y
    T   T
    A   B

$$Y = AB \cdot X$$

X_1 ⊓‾⊓
    T A
        — Y
X_2 ⊔_⊔
    T
    B
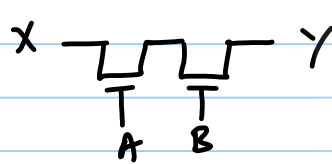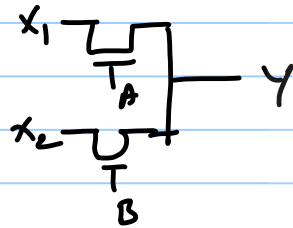
$$Y = AX_1 + BX_2$$

ACTIVE LOW SWITCHES

X —⊔‾⊔‾⊔— Y
    ◌   ◌
    A   B

$$Y = \bar{A}\bar{B} X$$

X_1 ⊓‾⊓
    ◌ A
        — $Y = \bar{A}X_1 + \bar{B}X_2$
X_2 ⊔_⊔
    ◌
    B