07/11/2019

MODULE-5- SEQUENTIAL CIRCUITS

$$t_{DQ} = t_{DC} + t_{CQ}$$

$\overline{CLK}$

D

X_M

I_1

CLK

Q_M

I_2

$\overline{CLK}$

X

Q.

$\overline{CLK}$

Q_M & Q.

CLK

$\overline{CLK}$

D.

Q.
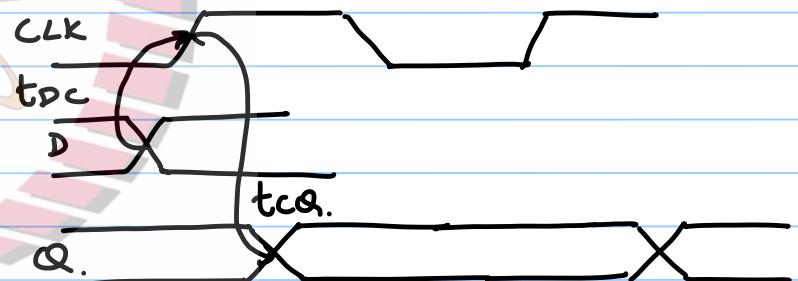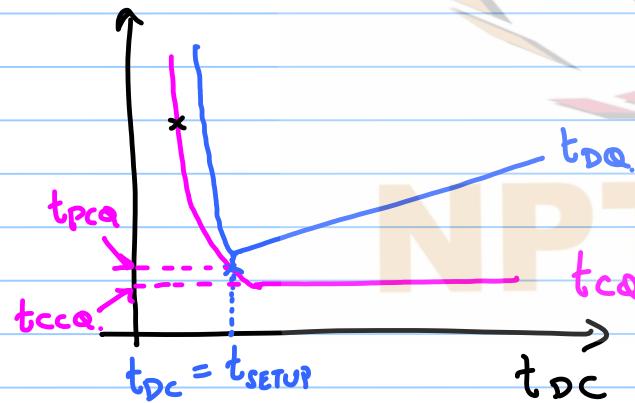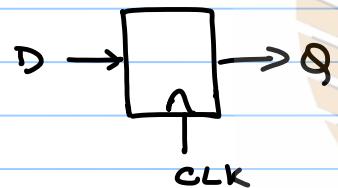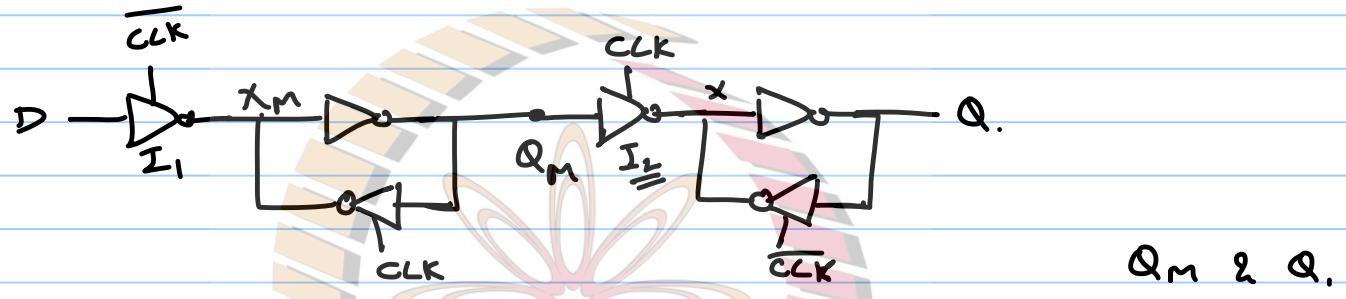
T_{CQ}
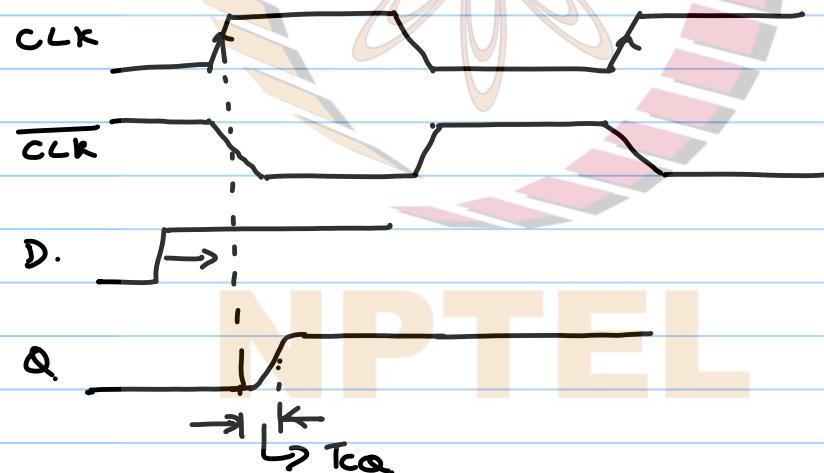
COMB BLOCKS $\rightarrow$ t_{CD}, t_{PD}.

SEQ ELEMENTS $\rightarrow$ t_{CCQ}, t_{PCQ}, t_{SETUP}, t_{HOLD}.

SYSTEM DELAY CONSTRAINTS

D_1 — F1 — Q_1 — t_{PD}, t_{CD} — D_2 — F2 — Q_2

ϕ

T_c

ϕ

t_{PCQ}

T_{SKEW}

D_1 ①

t_{CCQ}

Q_1 ①

t_{PD}

t_{SKEW}

t_{SETUP} t_{SETUP}

D_2 x t_{CD} ①

MAX DELAY CONSTRAINT

$$T_c \geqslant t_{PCQ} + t_{PD} + t_{SETUP} + t_{SKEW}$$

$$\Rightarrow \quad t_{PD} \leq T_c - (t_{PCQ} + t_{SETUP} + t_{SKEW})$$

SEQUENCING OVERHEAD

D1 →

Q1

t_{CD}, t_{PD} → D2

Q2

∅
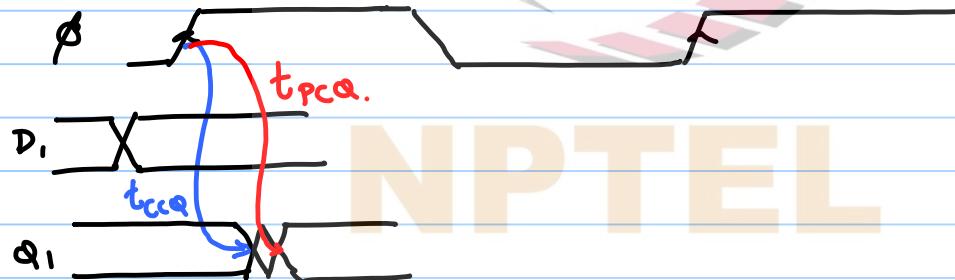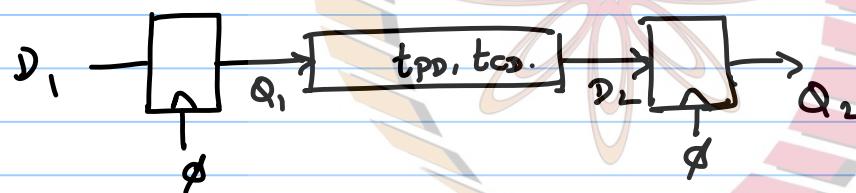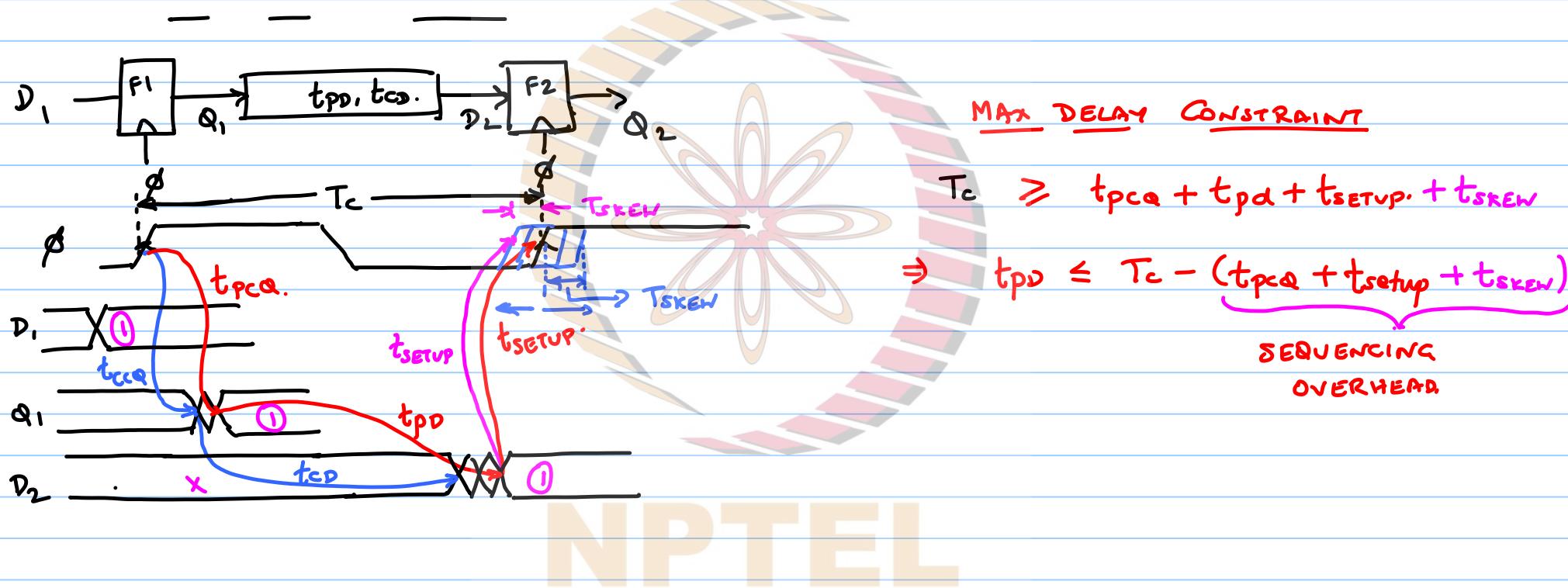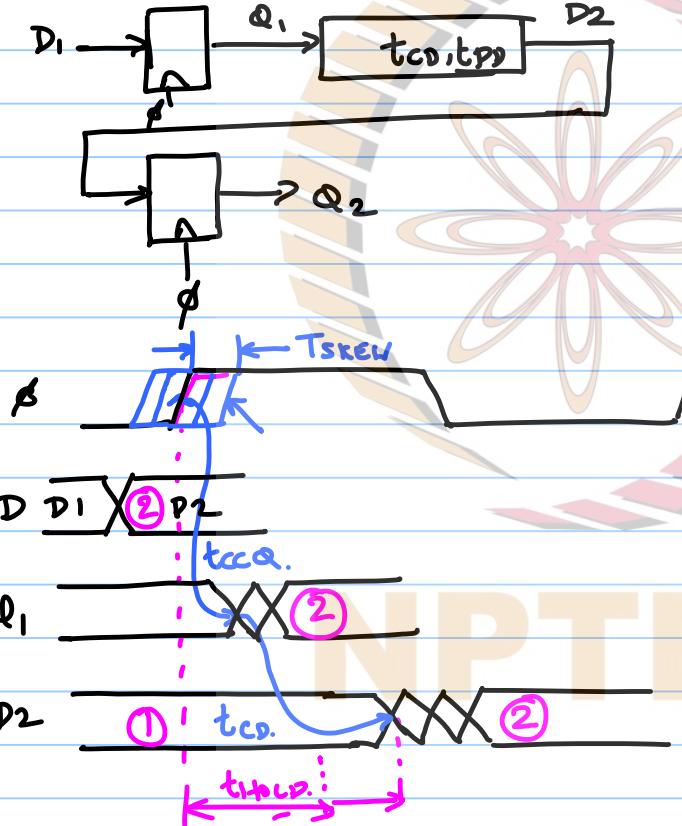
MIN DELAY CONSTRAINT

$$t_{SKEW} + t_{HOLD} \leq t_{CCQ} + t_{CD} \quad — ①$$

$$\Rightarrow \quad t_{CD} \geq t_{HOLD} - t_{CCQ} + t_{SKEW} \quad — ②$$

∅ → T_{SKEW}

D D1 ② D2

t_{CCQ}

Q1 ②

D2 ① t_{CD} ②

t_{HOLD}