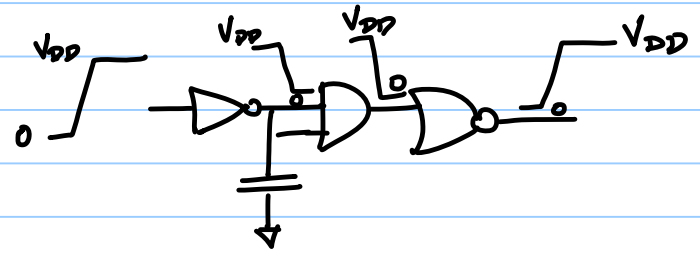
26/08/2019

EE5311

MODULE-3 – THE INVERTER

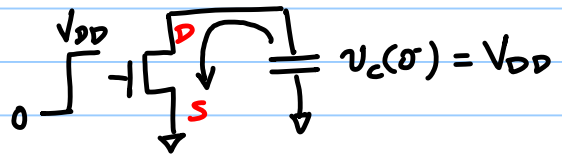


CHARGING / DISCHARGING A CAPACITANCE

NMOS CH
PMOS DIS

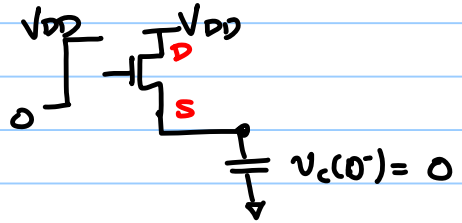
NMOS : DRAIN → SOURCE CURRENT FLOW
(IDEAL ⇒ NO LEAKAGE)

DISCHARGING



$V_{GS}(t) = V_{DD} > V_T \quad \forall\, t$

CHARGING:



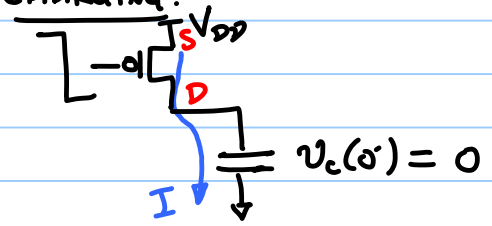
$V_{GS}(t) = V_{DD} - V_c(t) > V_T$

$V_c(t) < V_{DD} - V_T$ (MAX VALUE THAT AN NMOS CAN PASS)

★ VERY SLOW CHARGING

PMOS : S→D CURRENT FLOW

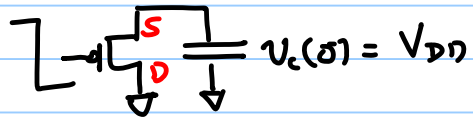
CHARGING:



$V_{GS}(t) = -V_{DD} < V_{Tp}$

CAP CAN CHARGE TO V_{DD}

DISCHARGING:



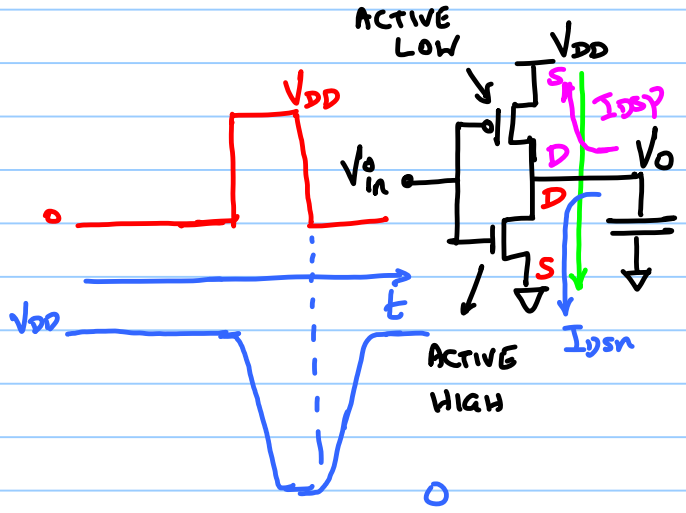
$V_{GS}(t) = -V_c(t) < V_{Tp}$

OR $V_c(t) > |V_{Tp}|$

⇒ PMOS CAN PASS ONLY UNTIL $|V_{Tp}|$

NMOS : DISCHARGING

PMOS : CHARGING



CMOS GATE (INVERTER)

	V_{GS}	V_{DS}
NMOS	V_{in}	V_O
PMOS	$V_{in}-V_{DD}$	V_O-V_{DD}

$$\boxed{I_{DSn} = -I_{DSp}} \quad \forall t$$

If $V_{in} = 0 \Rightarrow V_{GSn} = 0 \quad (< V_{Tn})$

$\Rightarrow I_{DSn} = 0 \Rightarrow I_{DSp} = 0$

$\Rightarrow V_{DSp} = 0 \Rightarrow V_O - V_{DD} = 0$

$\therefore V_O = V_{DD}$

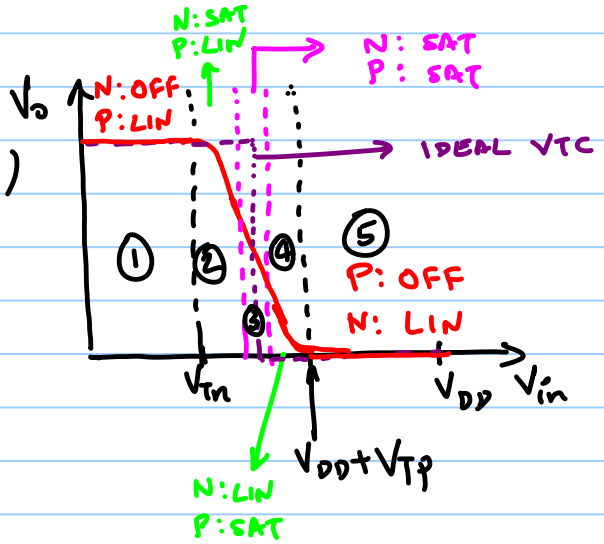
If $V_{in} = V_{DD} \Rightarrow V_{GSp} = V_{in} - V_{DD} = 0 \quad (> V_{Tp})$

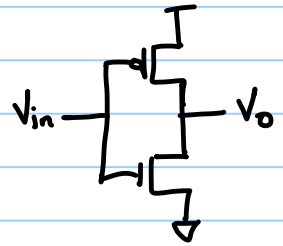
$\Rightarrow I_{DSp} = 0 \Rightarrow I_{DSn} = 0$

$\therefore V_{DSn} = 0 \Rightarrow V_o = 0$

VOLTAGE TRANSFER CHAR (VTC)

1) NMOS TURNS ON IN SATURATION (PMOS: LIN)





$V_{GSn} = V_{in} \quad V_{GSp} = V_{in} - V_{DD}$

$V_{DSn} = V_o \quad V_{DSp} = V_o - V_{DD}$

$I_{DSn} = -I_{DSp}$.

$V_{GSp} < V_{Tp}$

$\Rightarrow V_{in} - V_{DD} < V_{Tp}$

$\Rightarrow V_{in} < V_{DD} + V_{Tp}$