MODULE-4 : COMBINTIONAL CIRCUITS

SHARED
CONTACTED
DIFFUSION

SHARED UNCONTACTED DIFFUSION

6C

2C

D1

D2

NOR3

$$Y = \overline{A+B+C}$$

$$\frac{2R}{6} = \frac{R}{3}$$

Labels on the figure: 6, Y, 6C, B 6, A 6, 6C, C, B, A, 9C
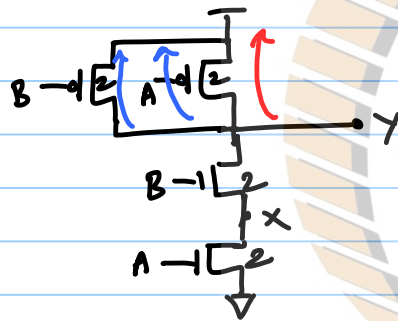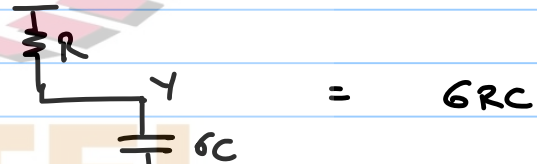
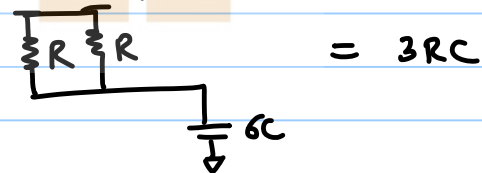# DELAY OF LOGIC GATES

RISE DELAY =

FALL DELAY =

PROPAGATION DELAY = WORST CASE DELAY

CONTAMINATION DELAY = BEST ~ ~

RISE PROP DELAY :

= 6RC
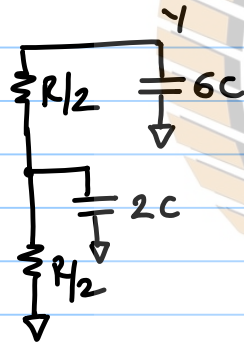
RISE CONT DELAY :

= 3RC

FALL DELAY (PROP):
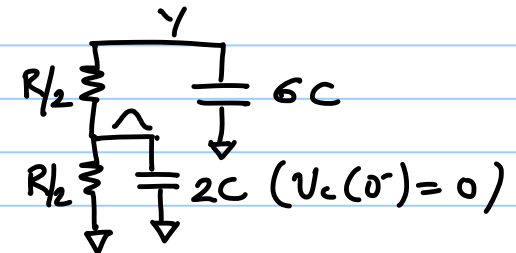
BOTH X & Y NEED TO DISCHARGE TO GND
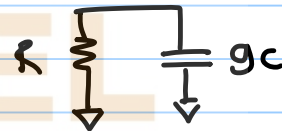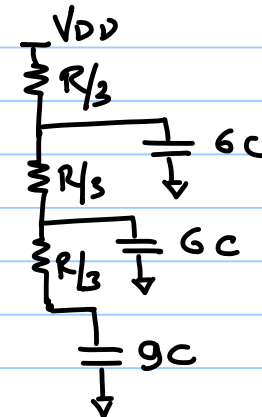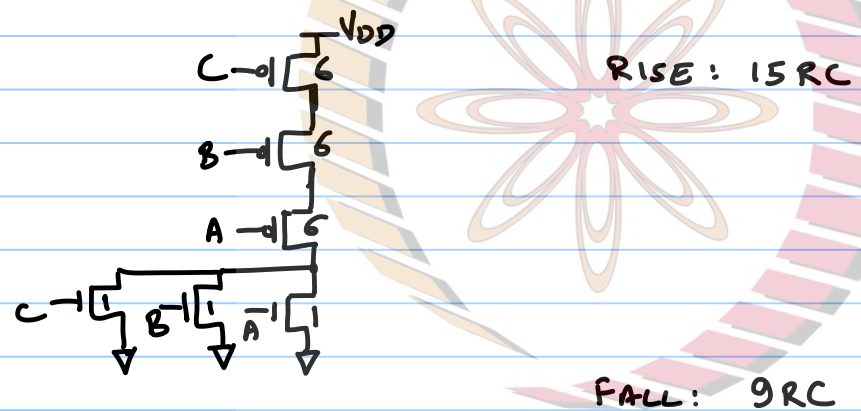

delay = 7RC

FALL CONT DELAY:

INPUT A IS HIGH FOR LONG. DISCHARGED NODE X TO GND.

$\Rightarrow$ delay = $6C(R/2 + R/2)$
$= 6RC$

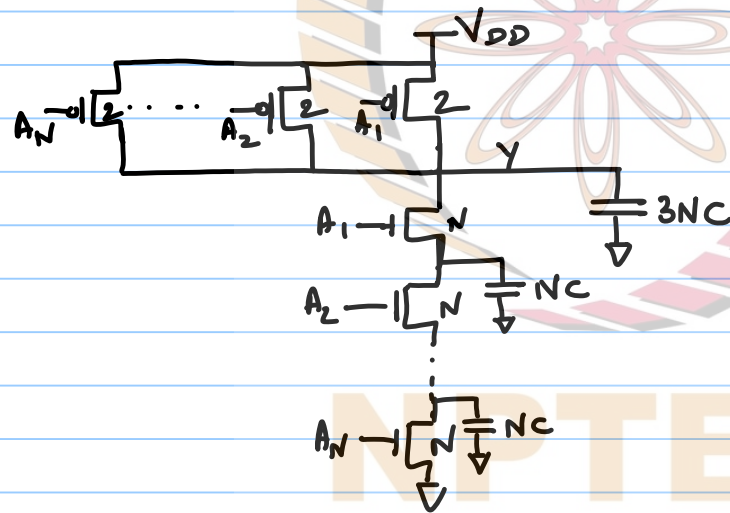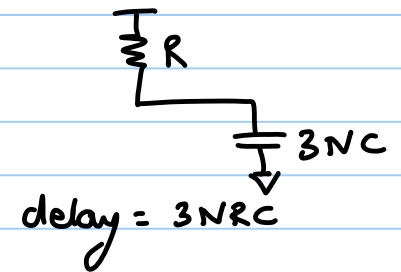# NOR3 GATE: PROP DELAYS:

RISE: $15RC$

FALL: $9RC$

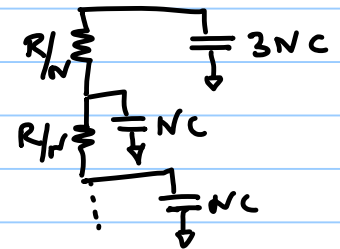# N-INPUT NAND GATE (PROP DELAY)

$$Y = \overline{A_1 A_2 \cdots A_N}$$

RISE :

delay = $3NRC$
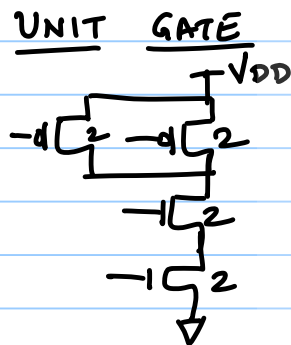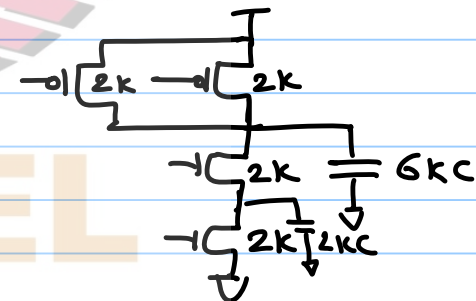
FALL :

$$\text{FALL DELAY} = 3NC(R) + NC\frac{(N-1)R}{N} + NC\frac{(N-2)R}{N} + \dots + NC \cdot \frac{R}{N}$$

$$= \frac{N(N+5)}{2} RC$$

$$\propto N^2$$
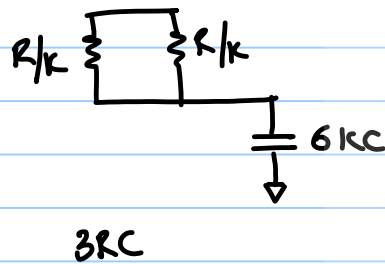
$$\Rightarrow \underline{DO \cdot NOT \ STACK \ MORE \ THAN \ 4 \ TRANSISTORS}$$

UNIT GATE

UNIT NAND2 GATE

RISE   FALL

CONT

R/k R/k $R/2k$ $6kC$

          $6kC$ $R/2k$ $2kC \; (v_c(0^-) = 0)$

3RC   6RC
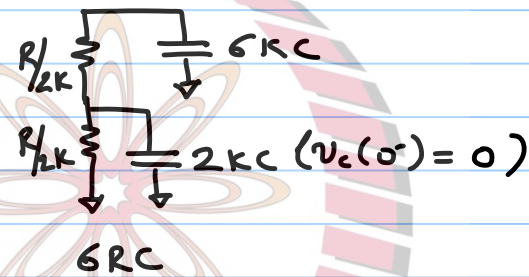
PARASITIC DELAY
IS INDEPENDENT
OF DRIVE STRENGTH

PROP

R/k $R/2k$ $6kC$

       $6kC$ $R/2k$ $2kC$

6RC   7RC
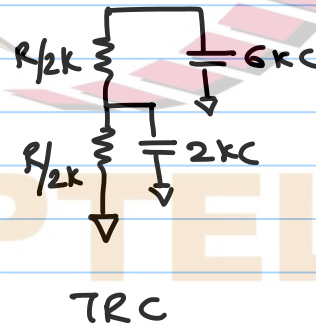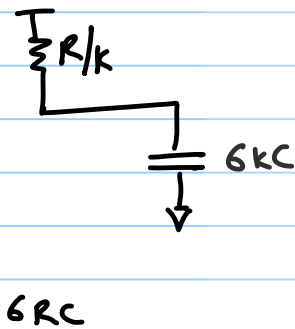
Parasitic Delay Approximation

Count the O/P diff cap and normalize to cap of a ref inv :

$$\frac{9C}{3C} = 3.$$

For NAND2: $\frac{6C}{3C} = 2$