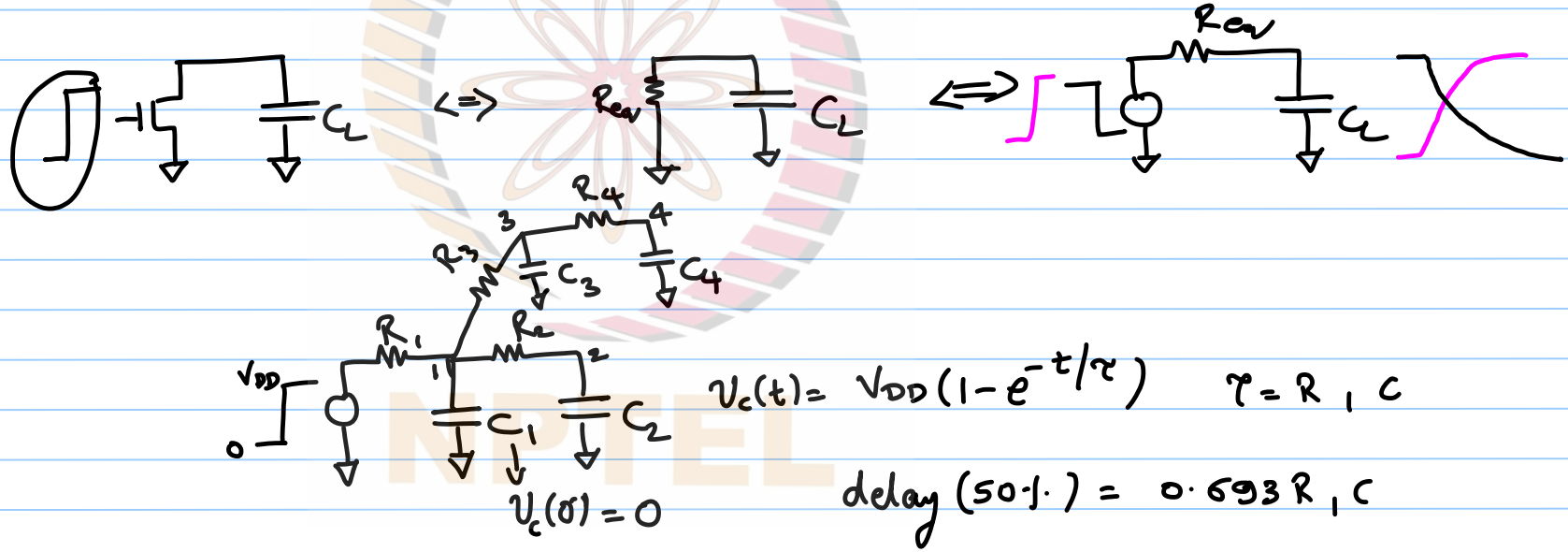
22/08/2019

EE5311

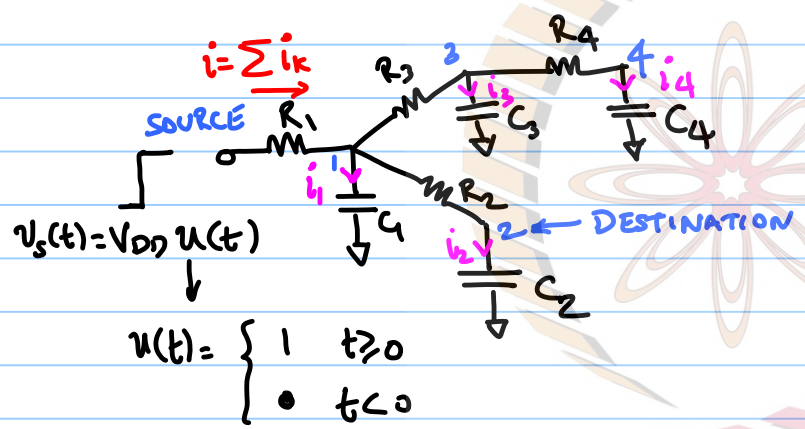
MODULE -2 - INTERCONNECTS



$V_c(t) = V_{DD}(1 - e^{-t/\tau})$ $\quad \tau = R_1 C$

delay (50%) $= 0.693 R_1 C$

ELMORE DELAY MODEL



$$u(t) = \begin{cases} 1 & t \geq 0 \\ \bullet & t < 0 \end{cases}$$

$v_K(t) = v_{CK}(t)$ = Voltage across cap C_K

$\tau_{s2} = \tau_2$

OBSERVATION:

1) $\lim_{t \to \infty} v_{c_K}(t) = V_{DD}$.

2) Majority: τ_2 not dep on C_3 or C_4
   τ_2 " " " R_3 or R_4

$$i_K(t) = C_K \frac{dv_K}{dt}$$

$$v_s(t) - v_2(t) = \left(\sum i_k\right) R_1 + i_2 R_2$$

ASSUMPTION:

1) SOURCE is $V_{DD}u(t)$
2) RC TREE
3) All CAPACITORS ARE BETWEEN nodes & GND
4) $v_k(t) = V_{DD}(1 - e^{-t/\tau_k})$

$\tau_2 \rightarrow$ TIME CONSTANT OF node 2

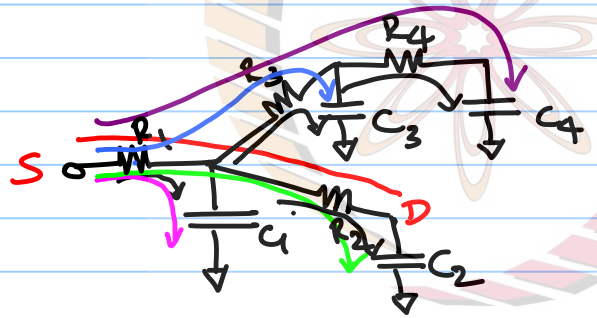
$$\left(V_{DD}u(t) - V_{DD}(1-e^{-t/\tau_2})u(t)\right) = R_1 \sum C_k \frac{dv_k}{dt} + R_2 C_2 \frac{dv_2}{dt}$$

$$\Rightarrow \int_0^\infty V_{DD} e^{-t/\tau_2} u(t)\,dt = \int_0^{V_{DD}} R_1 \sum C_k dv_k + \int_0^{V_{DD}} R_2 C_2 dv_2$$

$$= V_{DD}\cdot\tau_2 = R_1\left(\sum C_k\right)V_{DD} + R_2 C_2 V_{DD}$$

$$\Rightarrow \quad \tau_2 = R_1 \sum_{K=1}^{4} C_K + R_2 C_2$$

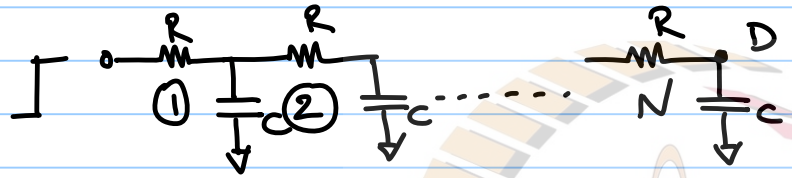
1) DOES NOT DEPEND ON R_3 & R_4
2) DEPENDS ON EVERY CAP IN THE CIRCUIT



$$\tau_2 = R_1 C_1 + (R_1 + R_2) C_2 + R_1 C_3 + R_1 C_4$$

$$\tau_3 = R_1 C_1 + R_1 C_2 + (R_1 + R_3) C_3 + (R_1 + R_3) C_4$$

$$\tau_4 = R_1 C_1 + R_1 C_2 + (R_1 + R_3) C_3 + \underbrace{(R_1 + R_3 + R_4)}_{\downarrow} C_4$$



$$\tau = RC + 2RC + 3RC + \cdots + NRC$$

$$= \frac{N(N+1)}{2} RC.$$

$$v_k(0^-) = a_k$$

$$\tau_2 = R_1 \sum C_k + R_2 C_2$$

$$\Rightarrow \quad V_{DD}\tau_2 = R_1 \sum C_k (V_{DD} - a_k) + R_2 C_2 (V_{DD} - a_k)$$

NPTEL

D_K = DELAY (50%.) = $0.693\,\tau_K$

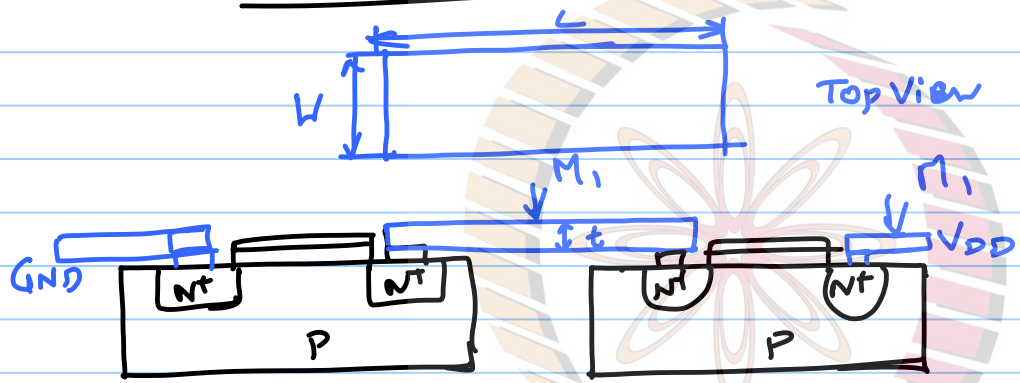
↓

(DROP)

Delay = τ_K

NPTEL

INTERCONNECT

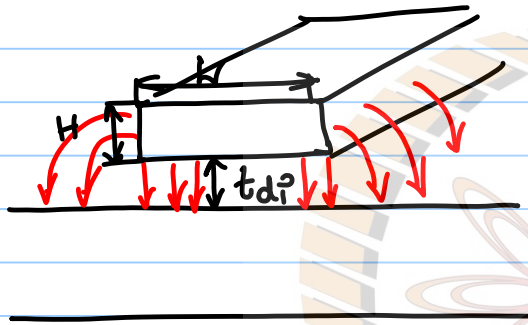


L → DESIGN PARAM

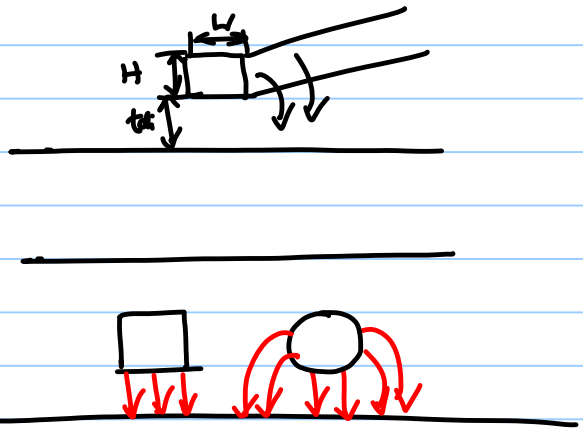
t → Tech PARAM

W → SEMI (DESIGN/TECH)

NPTEL



$$\text{CAPACITANCE} = \frac{\varepsilon_{ox} W L}{t_{di}}$$



$$C_{\parallel} = \frac{\varepsilon_{ox} W L}{t_{di}} =$$

$$C_{CYL} = \frac{2\pi \varepsilon_{ox}}{\log\left(t_{di}/H\right)}$$

NPTEL