06/11/2019

## MODULE-5 — SEQUENTIAL CIRCUITS
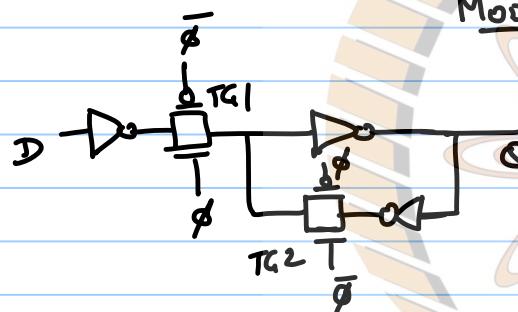
BREAKING THE FEEDBACK
  PATH

* Transistor sizes don't matter
  for functionality.
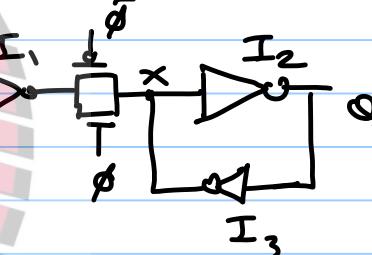
OVER POWERING FEEDBACK

* Tran sizes matter
  $I_1 \gg I_3$.

ASSUMPTIONS: CLOCK $\longrightarrow$ * IDEAL EDGES (RISE/FALL TIME = 0)
* CLK (ϕ) & $\overline{CLK}$ $(\overline{\phi})$ HAVE NO SKEW

IF CLK & $\overline{CLK}$ HAVE OVERLAP/DELAY

CLK

L1:T | L1:0
L2:0 | L2:T

$\overline{CLK}$

D | D1 | D2 | D3 | D4 | D5. |

→ INVALID U/6 CASE
↳ 1-1 OVERLAP (NON-SAMPLING EDGE)

Q
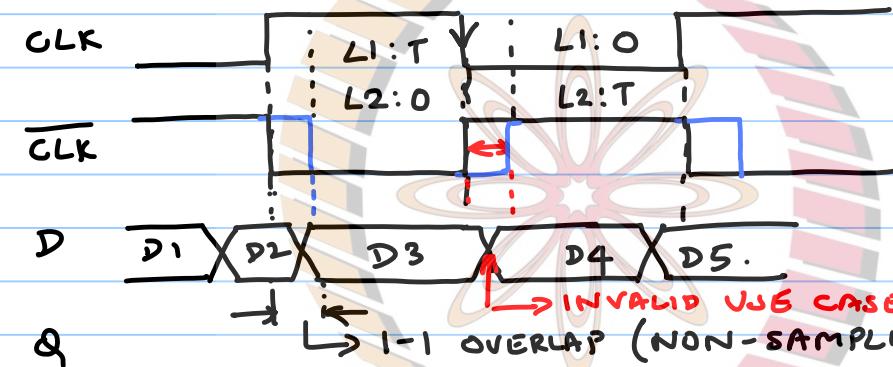
→ $t_{ov-1-1} < t_{I_1} + t_{N_1} + t_{I_2} + t_{I_4}$

t_{ov-0-0} → NO PROBLEM
↳ $t_{HOLD} > t_{ov-0-0}$

→ RACE CONDITION

CLK

$\overline{CLK}$

D —▷— I_1 — N1 ⊗ —▷— I_2 — Q_M — I_4 —▷— N3 X — I_5 —▷— Q.

N2 $\overline{CLK}$ I_3 N4 CLK. I_6

(L1: +ve   L2: -ve) → ve edge FLOP

D → [inverter] → [transmission gate, ϕ top, ϕ̄ bottom] → Q

⟱

D → [CMOS transmission gate: ϕ̄ and ϕ] → Q

D → [inverter, ϕ] → Y
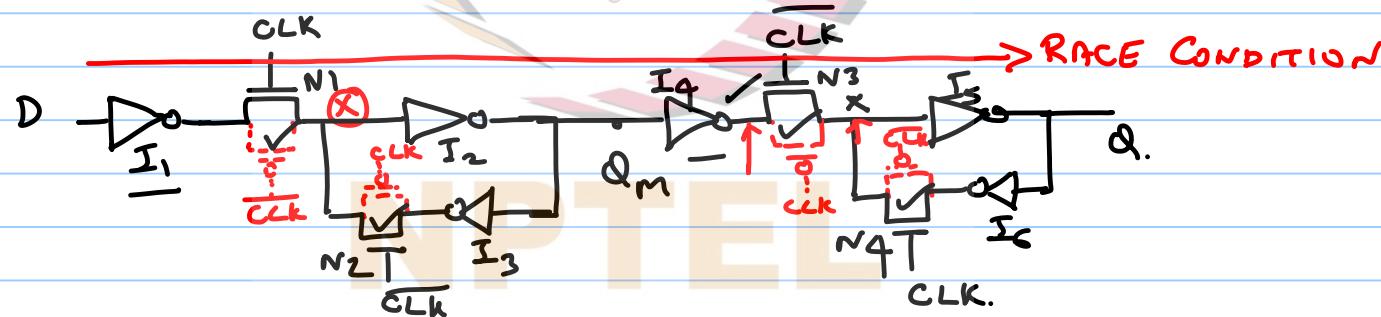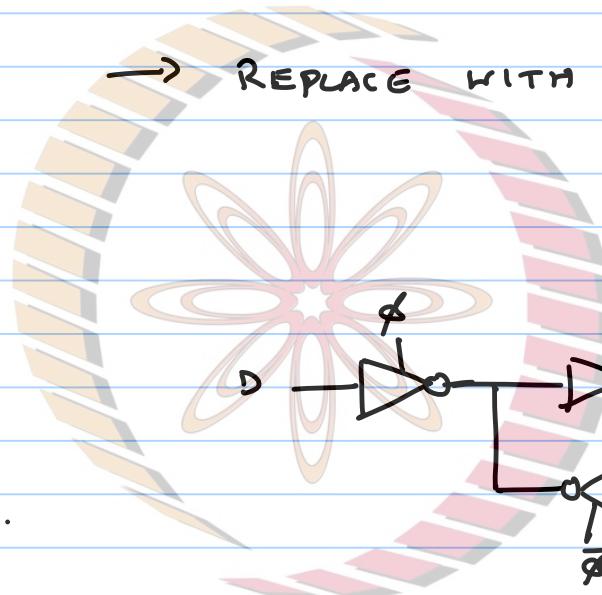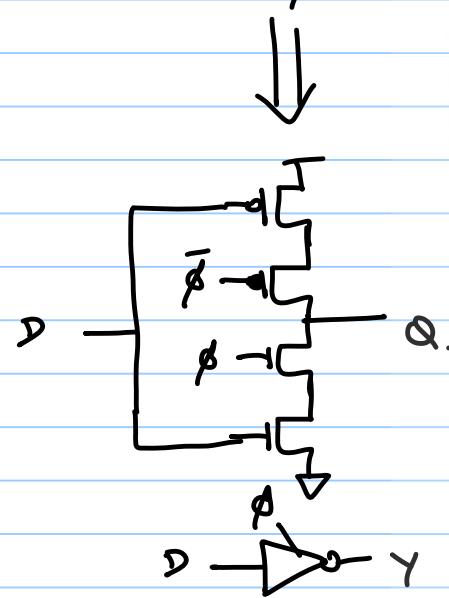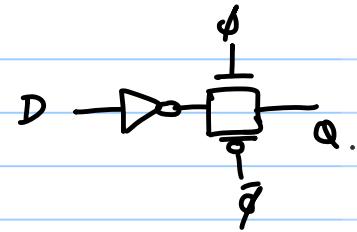
→ REPLACE WITH TRISTATE INV

FLOP WITH ISOLATION

→ Q.M

D → [tristate inv, ϕ] → [tristate inv, ϕ̄] → Q_M → [tristate inv, ϕ̄] → [tristate inv] →
with feedback tristate inv ϕ̄ and ϕ

Itanium 2 Latch

STATIC LATCH

DYNAMIC LATCH

$$V_c(0^+)$$
$$C_X = V_{DD}$$

$$Q$$

$$V_c(0^-) = 0$$
$$C_L$$

$$L : T$$ $$L : 0$$

$$\phi$$

$$D$$

$$Q$$

$$\gtrless 0$$
$$\lesssim V_{DD}$$

ϕ — P2

ϕ — P1

D

Q_M

N1

L1

−ve

$\bar{\phi}$ — P4

$\bar{\phi}$ — P3

Q

N3

L2

+ve

tve EDGE FLOP (DYNAMIC)

ϕ

$\bar{\phi}$

1-1   0-0

D

Q_M

ϕ

$\bar{\phi}$

ϕ

$\bar{\phi}$
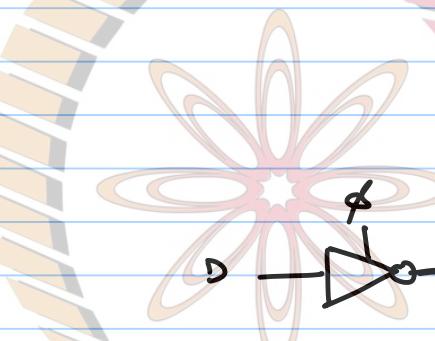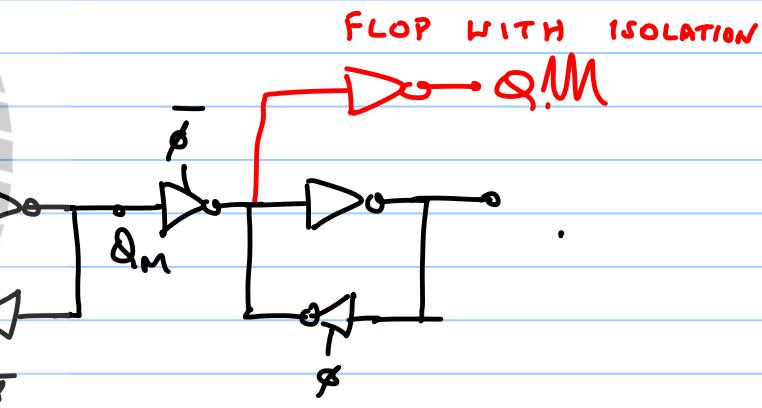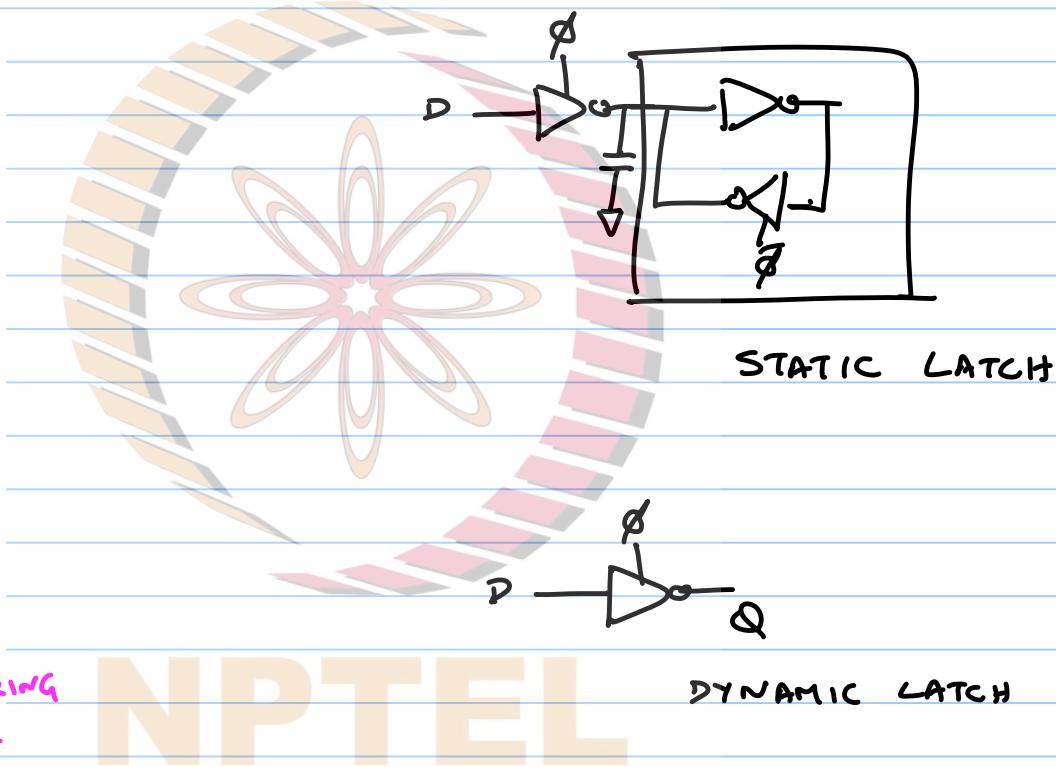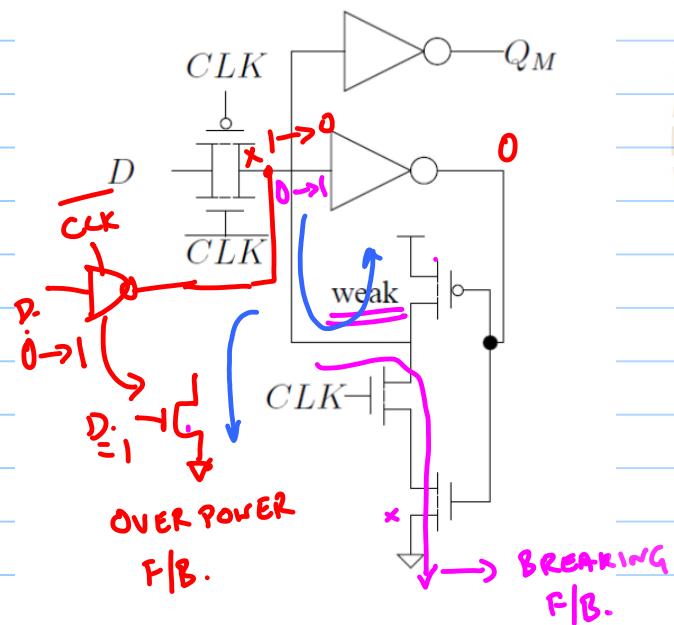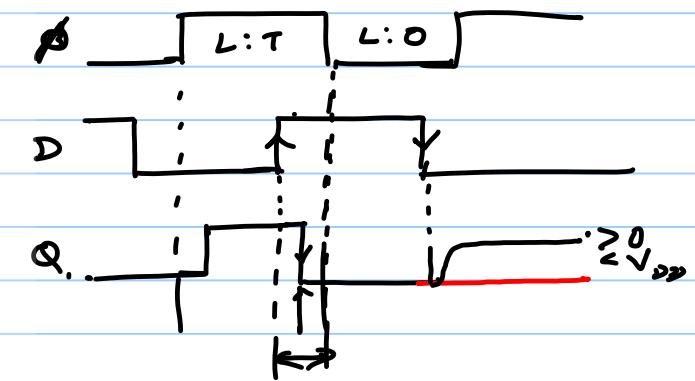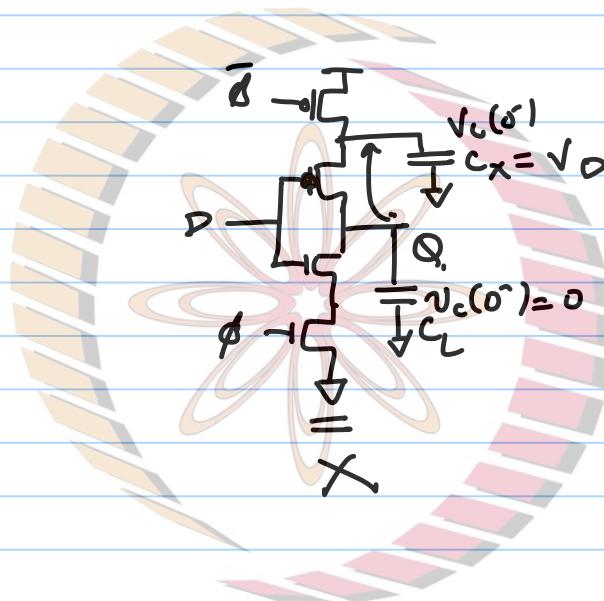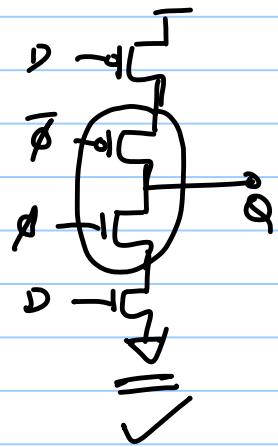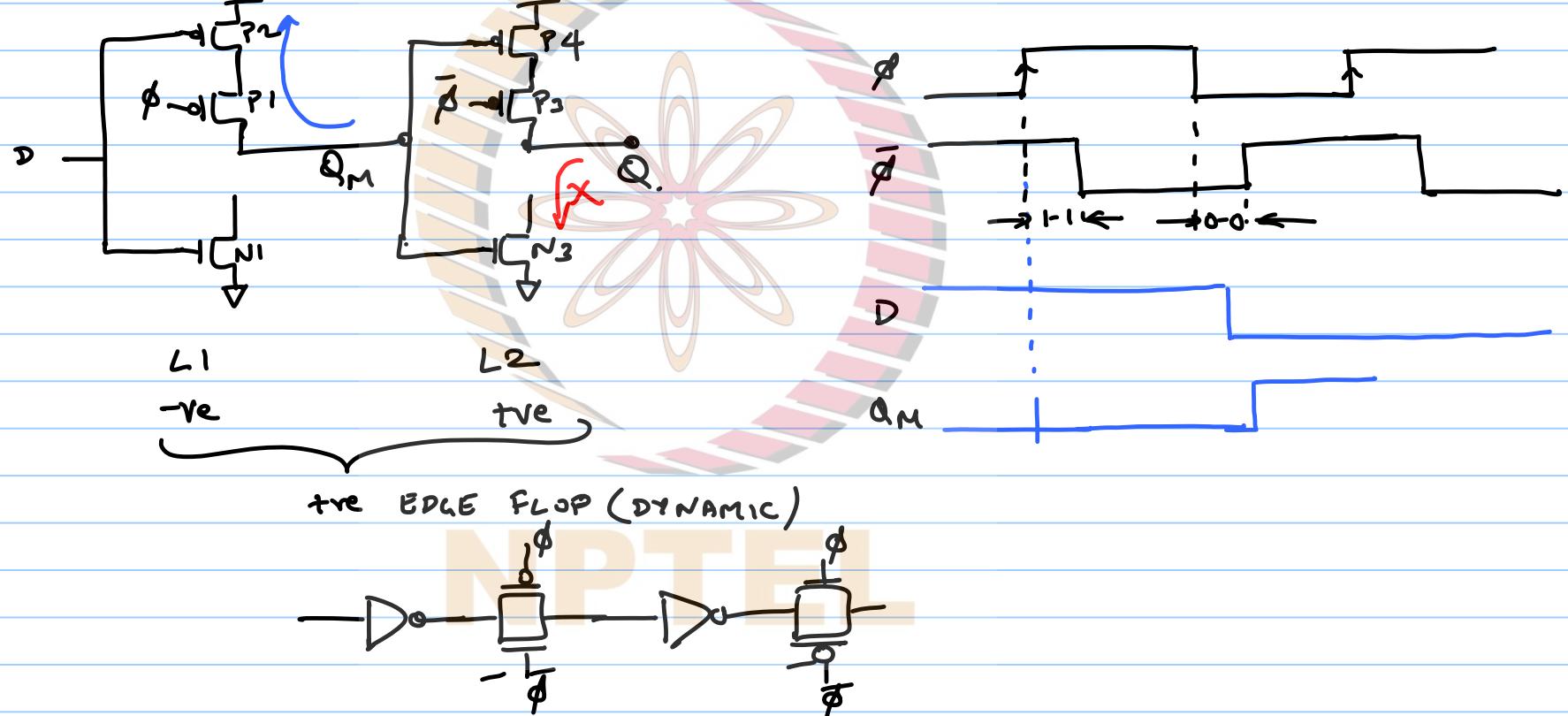
C²MOS FLOP/LATCH
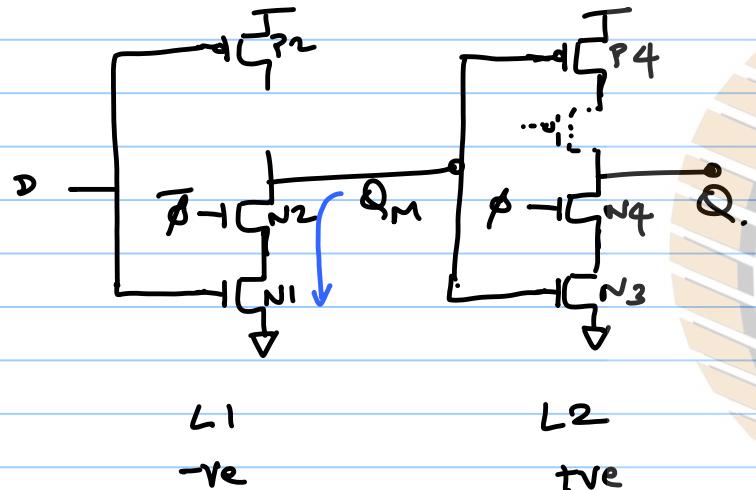
$t_{HOLD} > t_{OV-1-1}$

$t_{SETUP} = t_{TRI-STATE-L1}$

$t_{CQ} = t_{TRI-STATE-L2}$
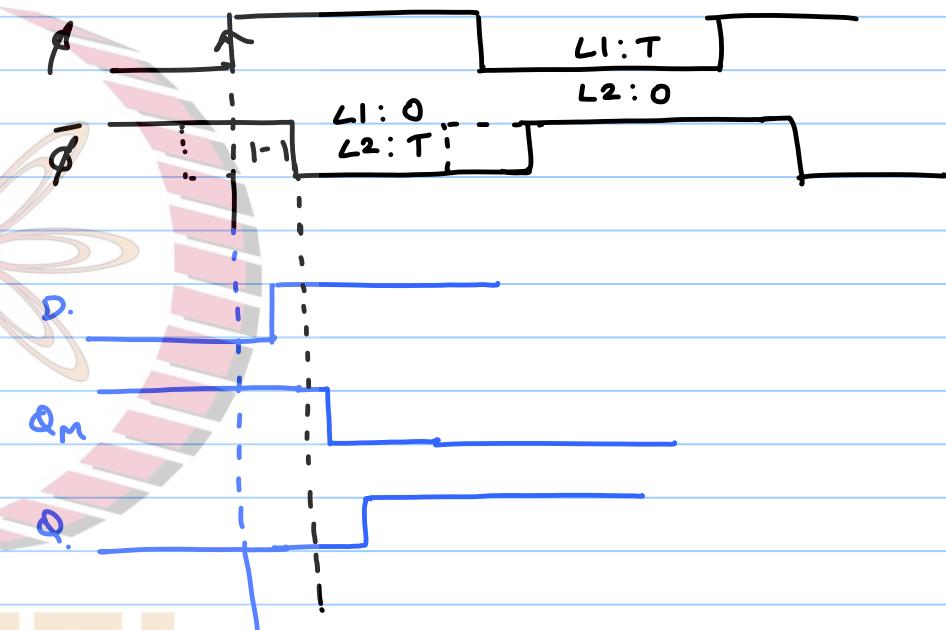
* CLOCK EDGES ARE NOT INSTANTANEOUS.

$$t_{DQ} = t_{DC} + t_{CQ}.$$

CORRECT

WRONG

t_{DQ}
t_{CQ}.

$t_{DQ} = t_{DC} + t_{CQ}$