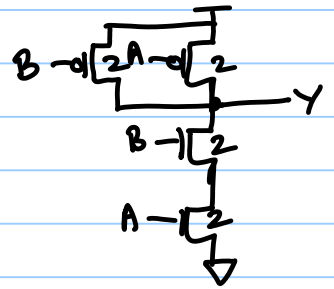
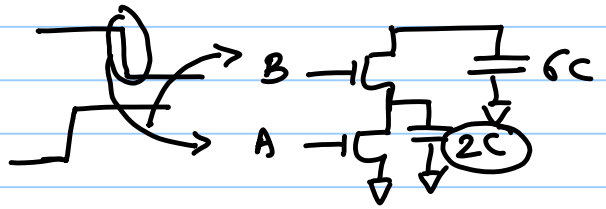
10/10/2019

# EE5311

## MODULE - 4 - COMBINATIONAL CIRCUITS



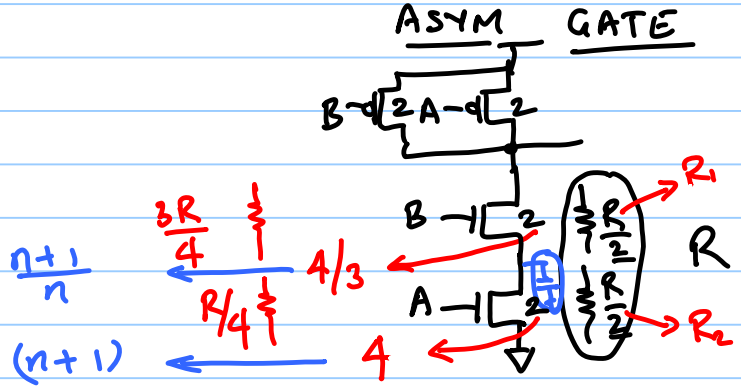



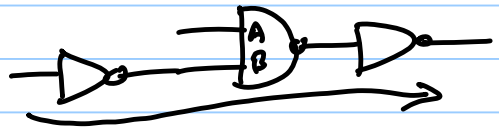

$\tau_{pd} = 7RC$

$\tau_{cd} = 6RC$

SIGNAL (INPUT) THAT ARRIVES LAST SHOULD BE CONNECTED TO THE TRANSISTOR CLOSEST TO THE OUTPUT

INPUT ORDERING.



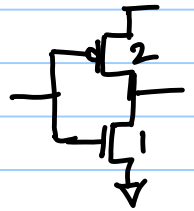

$g_A = (4+2)/3 = 2 > (4/3)$

$g_B = \frac{(4/3)+2}{3} = \frac{10}{9} < \left(\frac{4}{3}\right)$

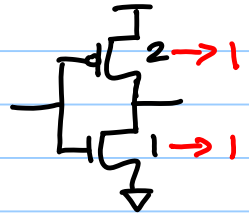
$R_1 + R_2 = R$ FIXED

$g_B = \frac{C_{NMOS} + C_{PMOS}}{3C}$

## SKEWED GATE




LO - SKEW



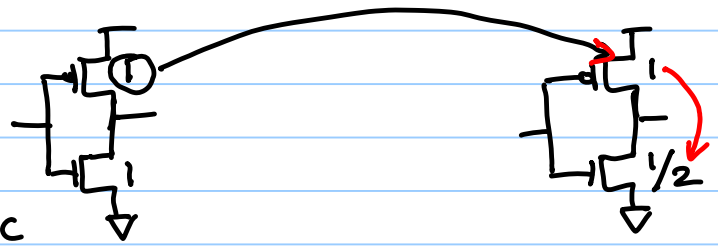

$$g = \frac{C_N + C_P}{3C}$$

$g_{PD}$ = PULL DOWN LOGICAL EFFORT

REF STATIC CMOS INV

$g_A = 2/3$

$g_{PU}$ = PULL UP LOGICAL EFFORT



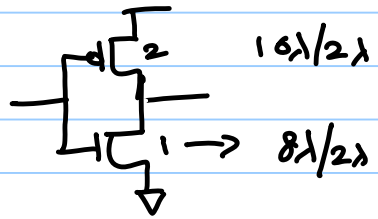

$C_A = 2C$

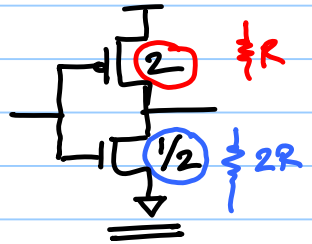
$C_A' = \frac{3}{2}C$

REF STATIC CMOS INV

$\therefore \quad g_{PU} = \frac{2}{(3/2)} = \frac{4}{3} > 1$

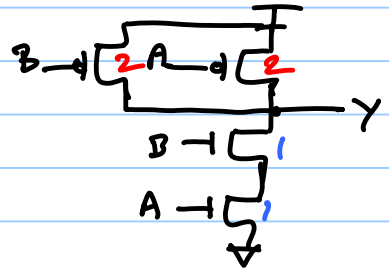
HI SKEW INV



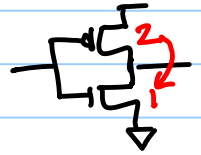

$C_A = \frac{5}{2}C$

HI SKEW NAND2



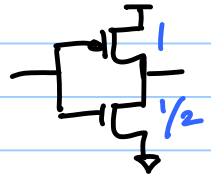

REF STATIC SYM INV

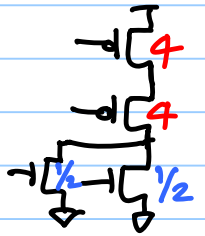
$g_{PU}$




$C_A' = 3C \Rightarrow g_{PU} = 5/6 < 1$

$g_{PD}$




$C_A' = \frac{3}{2}C \Rightarrow g_{PD} = 5/3 > 1$

NOR