

~~3/10/2019~~

EE5311

MODULE-5 - SEQUENTIAL CIRCUITS

10 steps.

Total time = 1000 units

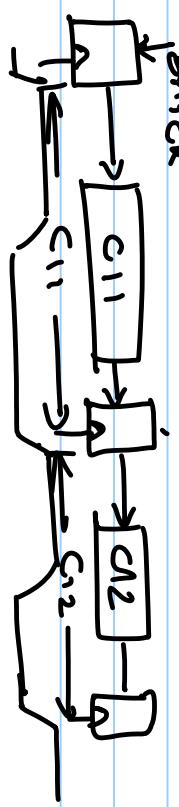
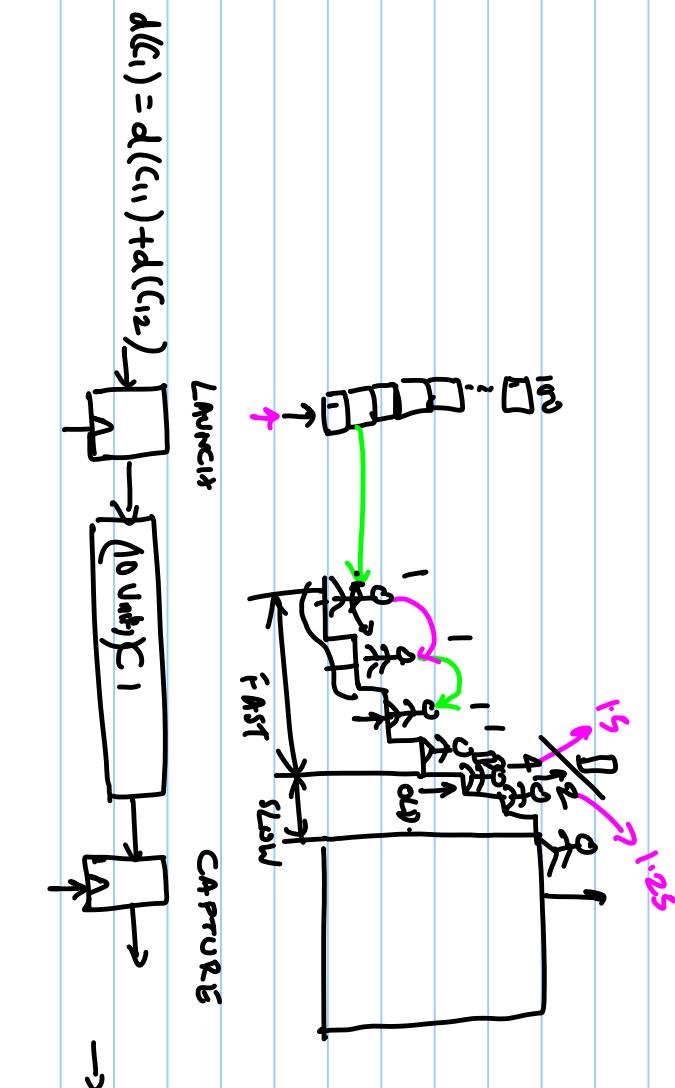
Pipeline

Total time = 110 units. ↵

Every 6.5 units we can feed a

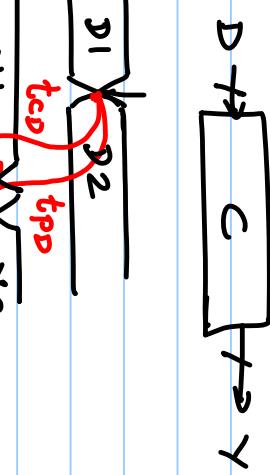
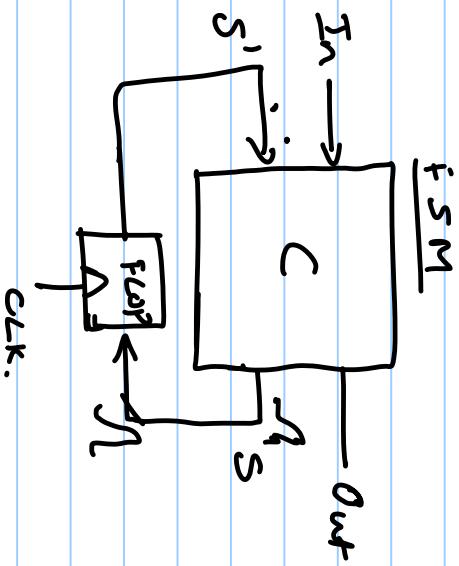
LATCH

CAPTURE

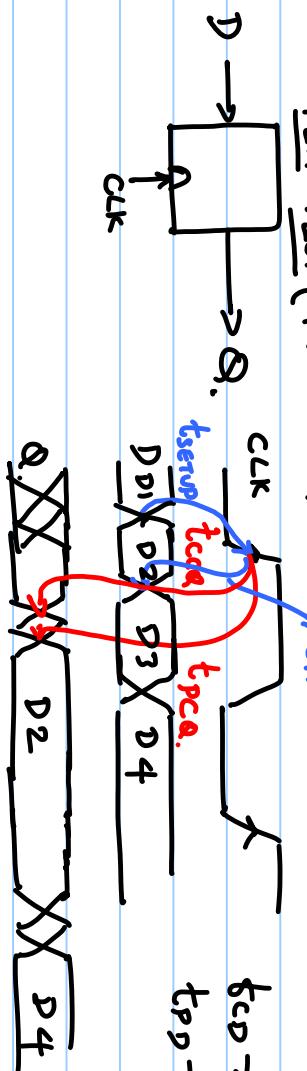


$$d(c_1) = d(c_{11}) + d(c_{12}) \rightarrow$$

FSM



FLIP FLOP (+ve EDGE)



$t_{cpd} \rightarrow$  CONTAMINATION DELAY  
 $t_{ppd} \rightarrow$  PROPAGATION DELAY.

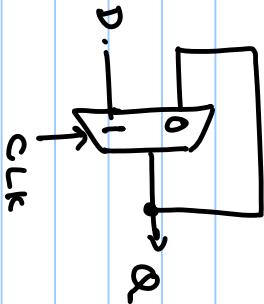
LATCH (+ve LATCH)

CLK

IF CLK == 1

二〇

If  $C_k = \emptyset$   
hold Q.



The diagram illustrates the timing sequence for a 4-bit pipeline register. The vertical axis represents time, and the horizontal axis represents the four stages of the pipeline (D1, D2, D3, D4).

- Clock Edges:** The clock signal (CLK) is shown as a series of steps occurring at regular intervals.
- Setup Time ( $t_{setup}$ ):** A red arrow indicates the time required for data to stabilize before the rising edge of the clock. It is labeled  $t_{setup}$  near the top of the diagram.
- Hold Time ( $t_{hold}$ ):** A blue arrow indicates the minimum time data must remain valid after the falling edge of the clock. It is labeled  $t_{hold}$  near the bottom of the diagram.
- Clock-to-Q Times:**
  - $t_{CQA}$ :** The time from the rising edge of the clock to the output becoming valid. It is labeled  $t_{CQA}$  with arrows pointing to the outputs of D2 and D3.
  - $t_{PQA}$ :** The time from the falling edge of the clock to the output becoming opaque. It is labeled  $t_{PQA}$  with arrows pointing to the outputs of D2 and D3.

$t_{\text{CDA}}$ ,  $t_{\text{PDA}}$

1

1

1

t

DQ

10

10

1

1

1

1

1

1

1