MODULE-5 — SEQUENTIAL CIRCUITS
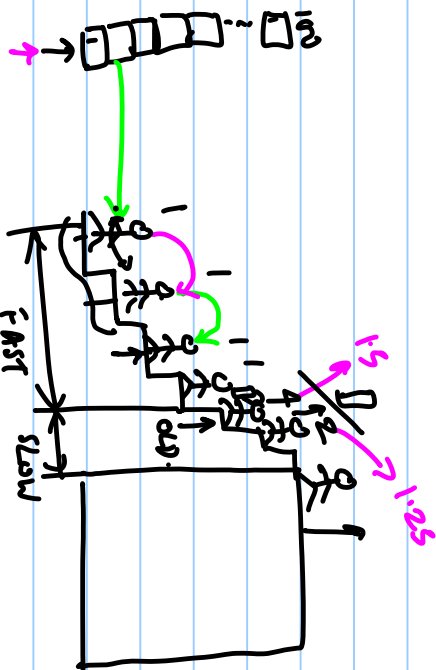
10 Steps.

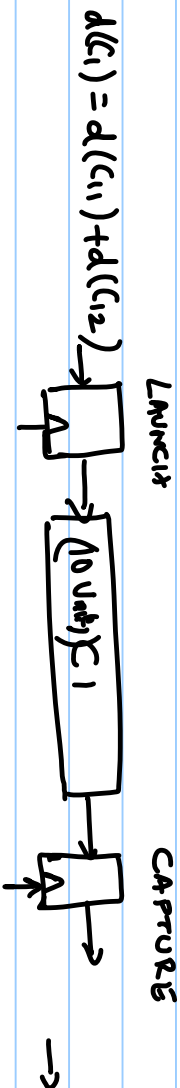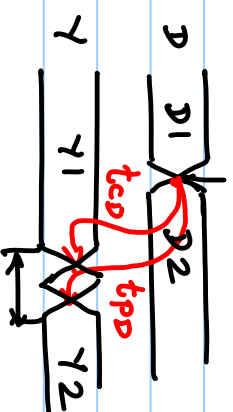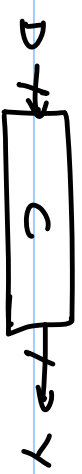Total time = 1000 units

Pipeline
Total time = 110 units. ←

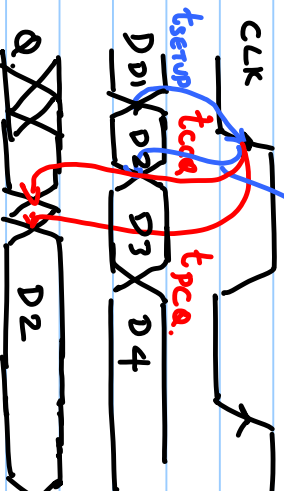Every 6.5 Units we can feed a
d(c_i) = d(c_{i1}) + d(c_{i2})

FSM

In → [C] → Out

S' ↘ ... ↗ S

[FLOP] ← CLK

FLIP FLOP (+ve EDGE)

D → [▷] → Q
CLK ↗

D → [C] → Y
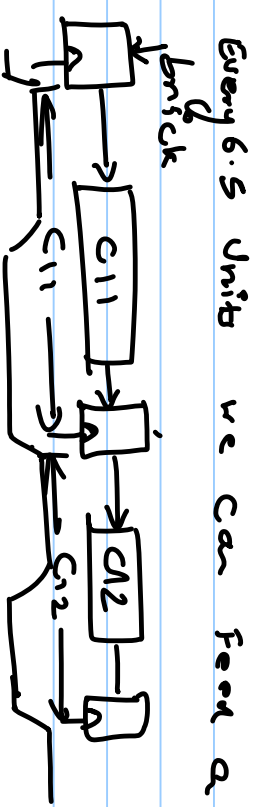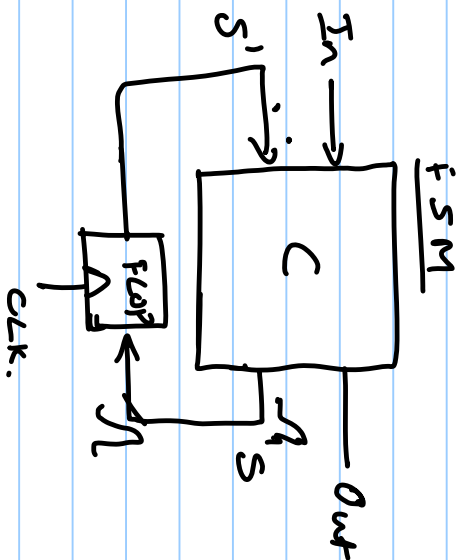
t_{CD} → CONTAMINATION DELAY
t_{PD} → PROPAGATION DELAY.

D: D1 | D2
Y: Y1 | Y2
t_{CD}, t_{PD}

CLK
DD1 D3 | D4
D2

t_{setup} t_{CCQ} t_{PCQ} t_{HOLD}
Q

LATCH (+ve LATCH)

D → [L] → Q
CLK →

IF CLK == 1
⇒ Q = D.

If CLK == 0
HOLD Q.

D
CLK → [transistor circuit] → Q

CLK

D: D1 | D2 | D3 | D4

Q: D1 | D2 | D3 | D4

t_{setup} t_{hold}

L→ Trans   L→Opaque   L→T

t_{ccq} t_{pcq}

t_{cdq} t_{pdq}