09/10/2019

MODULE-4- COMBINATIONAL CIRCUITS

### GATE SIZING:

N. Logic GATES

$G = \Pi g_k$

C_{in} C_L

$H = \dfrac{C_L}{C_{in}} = \Pi h_k$

$F = GH$

OPTIMAL $f_k = F^{1/N}$

$D_{min} = \underline{N F^{1/N}} + P \Rightarrow \Sigma p_i$

1x 4600x
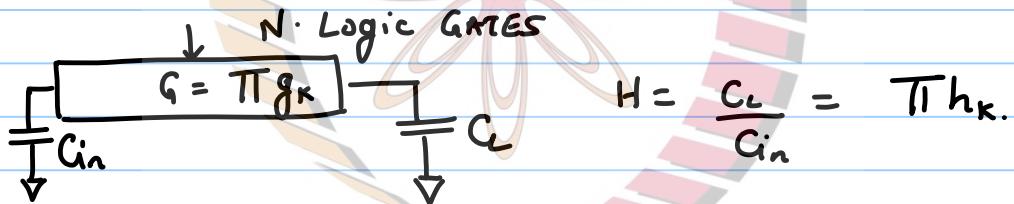
$f_{OPT} = (10000)^{1/4} = 10$

$D_{min} = \boxed{46.}$

BUFFER INSERTION

$$D_{min} = n_1 \, (F)^{1/n_1} + P$$

$$\widehat{D}_{min} = N \left(\hat{G} \hat{H} \right)^{1/N} + P + (N - n_1)\, p_{inv}$$

$$= N \, (F)^{1/N} + P + (N - n_1)\, p_{inv}$$

G, H, P

$F = G \cdot H$
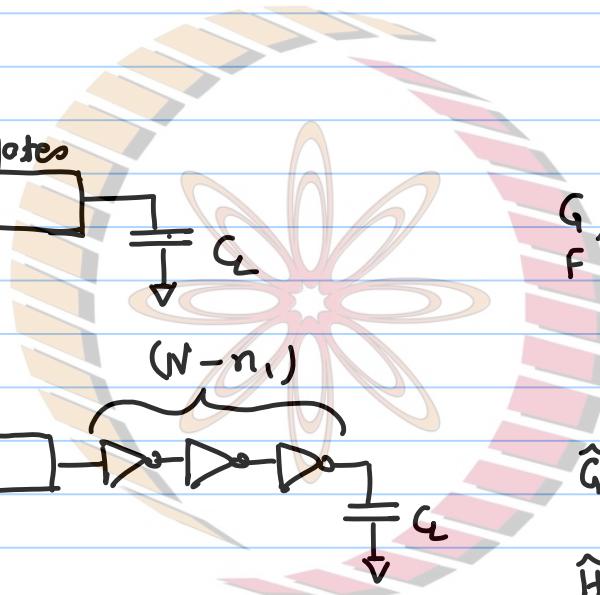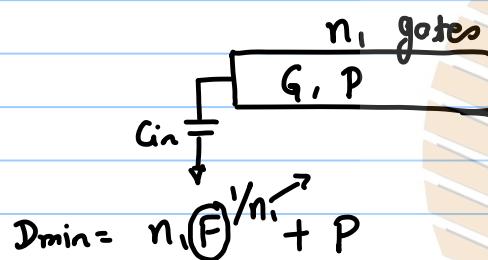
$\hat{G} = $ New Path Logical effort $= G \cdot \Pi \, g_{inv}$

$\qquad = G$

$\hat{H} = $ New path electrical $\sim = H$

$\hat{P} = $ New parasitic effort $= P + (N - n_1)\, p_{inv}$

$p_{inv} = $ Parasitic effort of inv $(= 1)$

$\hat{F} = \hat{G} \hat{H} = GH = F$

$$\frac{\partial \widehat{D}_{min}}{\partial N} = 0$$

$$\widehat{D}_{min} = N F^{1/N} + (N - n_1) p_{inv} + P$$

$$\frac{\partial \widehat{D}_{min}}{\partial N} = F^{1/N} (1) + N F^{1/N} \left(\frac{-1}{N^2}\right) \ln(F) + p_{inv}$$

$$\Rightarrow \left(F^{1/N}\right) \left(1 - \ln\left(F^{1/N}\right)\right) + p_{inv}^0 = 0$$

Let   OPTIMAL STAGE EFFORT $= P = F^{1/N}$

$$\Rightarrow \qquad P \left(1 - \ln(P)\right) + p_{inv}^0 = 0$$

$$P \left(1 - \ln(P)\right) + 1 = 0$$

When $P = 3.59$

$$P_{opt} = 3.59 \sim 4$$

$$P_{opt} = \left(F^{1/N}\right) \Rightarrow 1 = \frac{1}{N} \log_{P_{opt}}(F)$$

$$\Rightarrow \quad N = \frac{\log_4(F)}{}$$
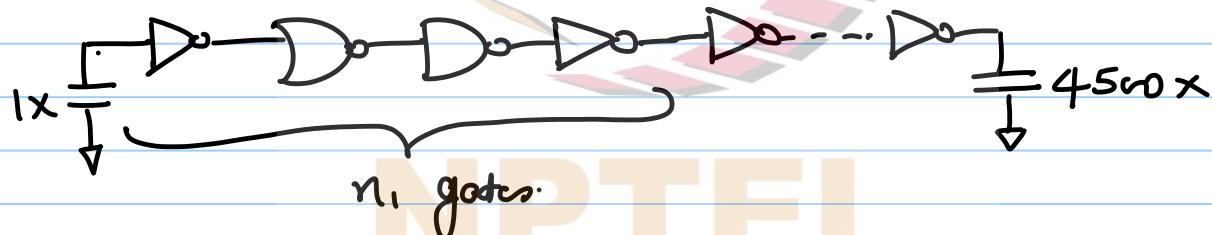
$$F = 10^4 = (20/9) \times 4500$$
$$N = \log_4(10^4) = 6.64$$

Post Buffering: $N_{opt} = 6/7 \longrightarrow 6$

$D_{min} = 6 \times (10^4)^{1/6} + 6 + 2 \times 1$

$= 35.8$