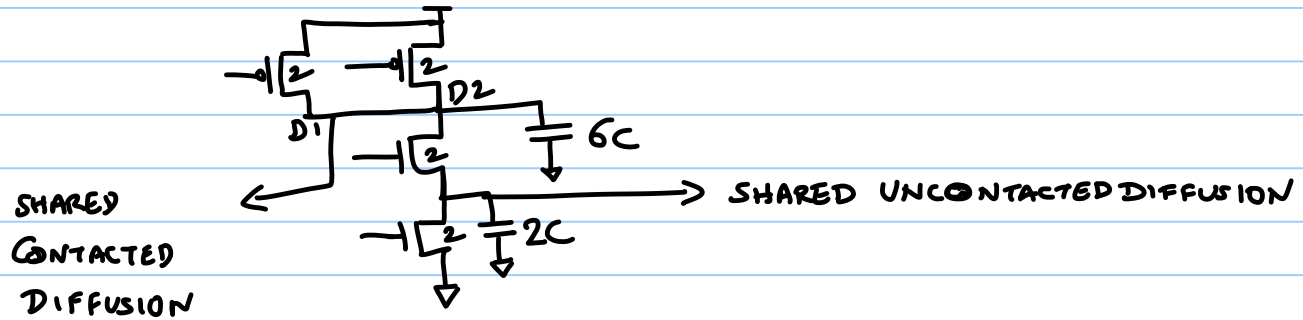
23/09/2019

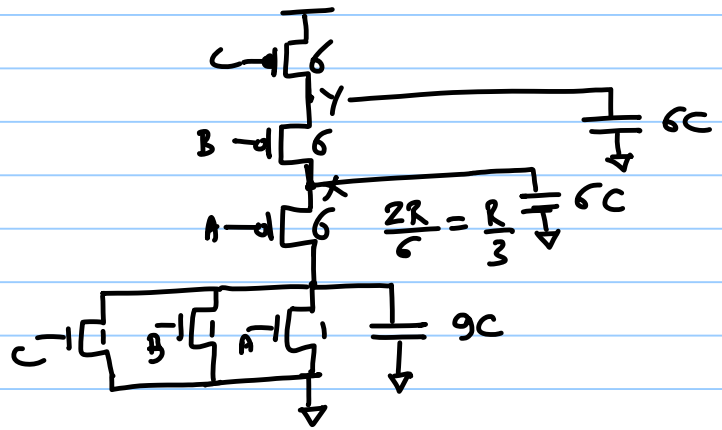
EE5311

MODULE-4 : COMBINTIONAL CIRCUITS

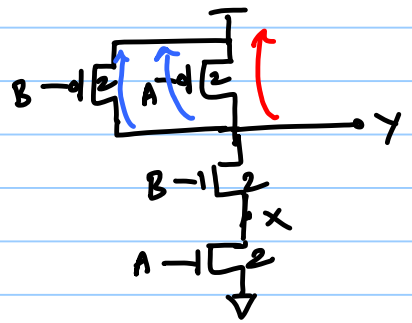


NOR3

$$Y = \overline{A+B+C}$$



DELAY OF LOGIC GATES



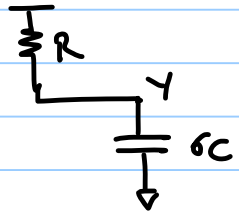
RISE DELAY =

FALL DELAY =

PROPAGATION DELAY = WORST CASE DELAY

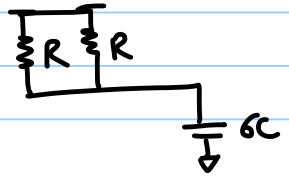
CONTAMINATION DELAY = BEST " "

RISE PROP DELAY :



= 6RC

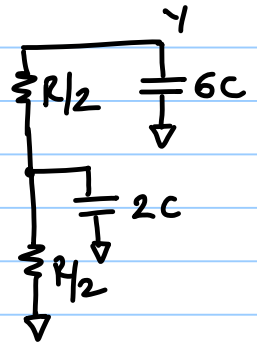
RISE CONT DELAY :



= 3RC

FALL DELAY (PROP) :

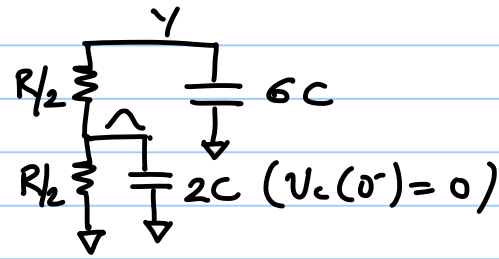
BOTH X & Y NEED TO DISCHARGE TO GND



delay = 7RC

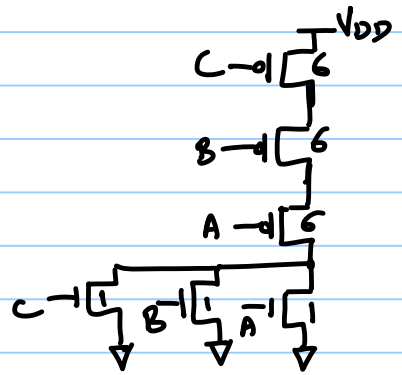
FALL CONT DELAY :

INPUT A IS HIGH FOR LONG. DISCHARGED NODE X TO GND.

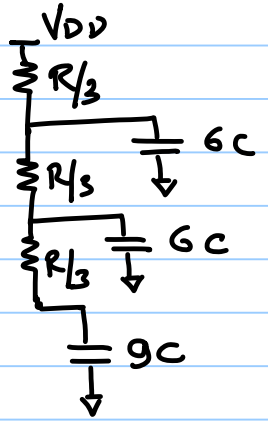


⇒ delay = 6C (R/2 + R/2)
= 6RC

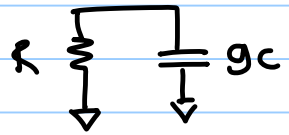
NOR3 GATE: PROP DELAYS:



RISE: 15RC

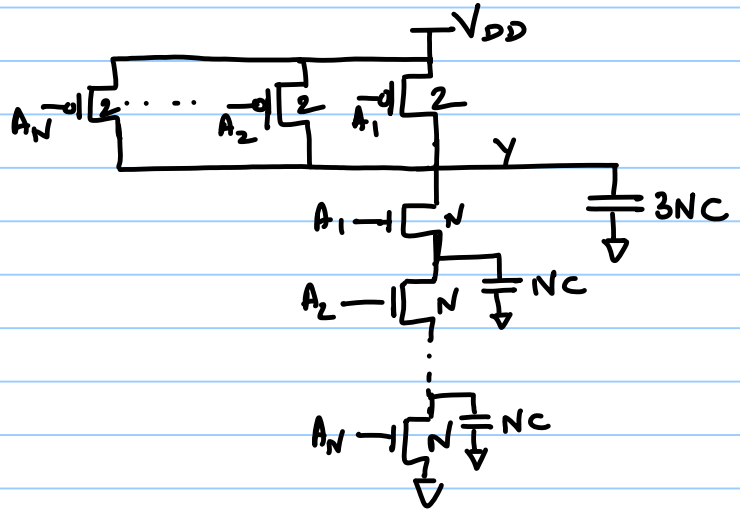


FALL: 9RC

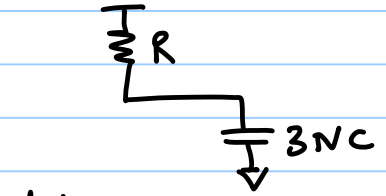


N-INPUT NAND GATE (PROP DELAY)

$$Y = \overline{A_1 A_2 \cdots A_N}$$

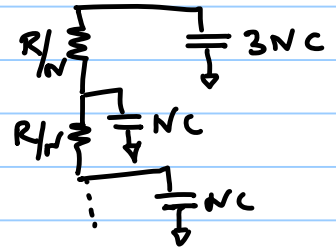


RISE :



delay = 3NRC

FALL :



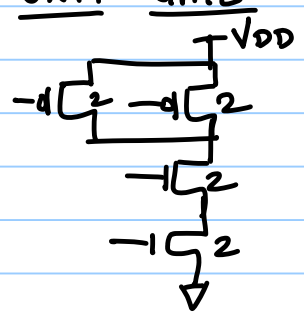
$$\text{FALL DELAY} = 3NC(R) + NC\frac{(N-1)}{N}R + NC\frac{(N-2)}{N}R + \cdots + NC\cdot\frac{R}{N}$$

$$= \frac{N(N+5)}{2}RC$$

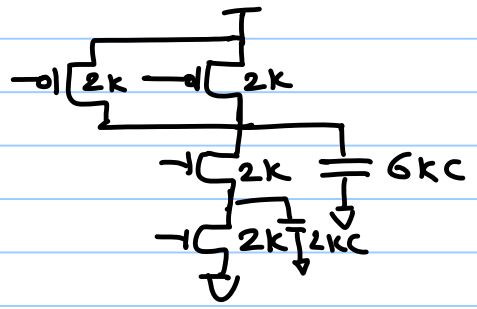
$$\propto N^2$$

$\Rightarrow$ DO NOT STACK MORE THAN 4 TRANSISTORS

UNIT GATE



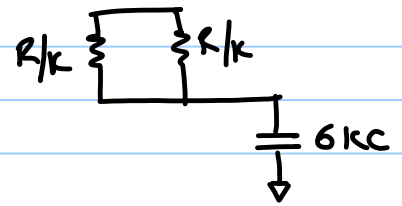
UNIT NAND2 GATE



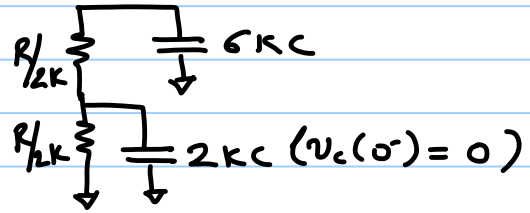
RISE

FALL

CONT



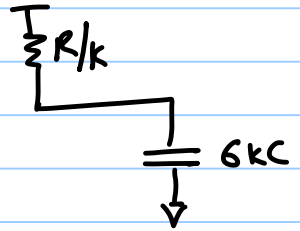
3RC



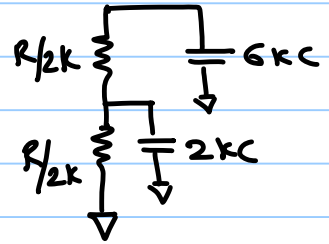
6RC

PARASITIC DELAY IS INDEPENDENT OF DRIVE STRENGTH

PROP



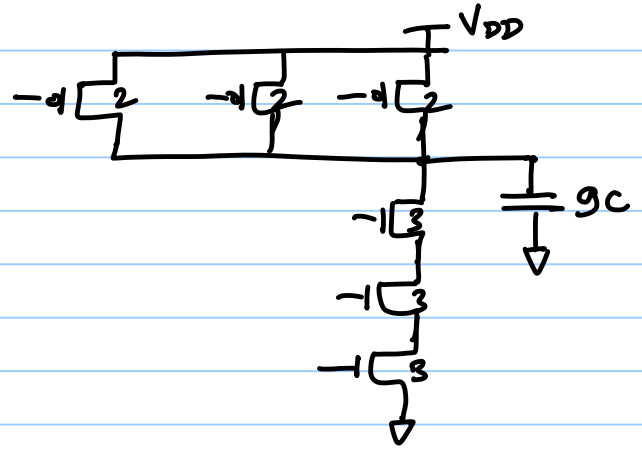
6RC

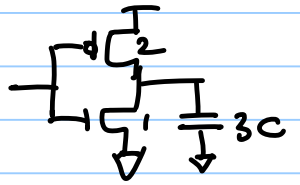


7RC

PARASITIC DELAY APPROXIMATION

COUNT THE O/P DIFF CAP and NORMALIZE TO CAP OF A REF INV :





$$\frac{9C}{3C} = 3.$$

FOR. NAND2 : $\frac{6C}{3C} = 2$