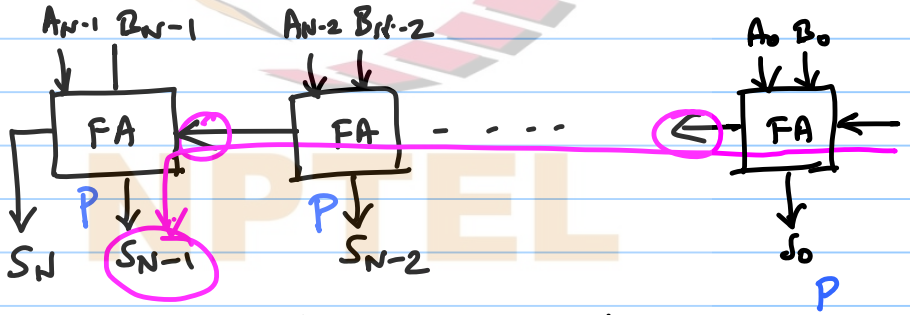
24/10/2019

# EE5311

## MODULE-6 - ADDERS

### MIRROR ADDER

1) MIRROR IDEA TO REDUCE PMOS STACK SIZE
2) $C_{in}$ (TIMING CRITICAL) → TO TRANSISTOR OF LEAST LE
3) $C_{in}$ CONNECTED TO ~ CLOSEST TO O/P
4) OPTIMIZED SUM TO BE GEN FROM $\overline{C_o}$



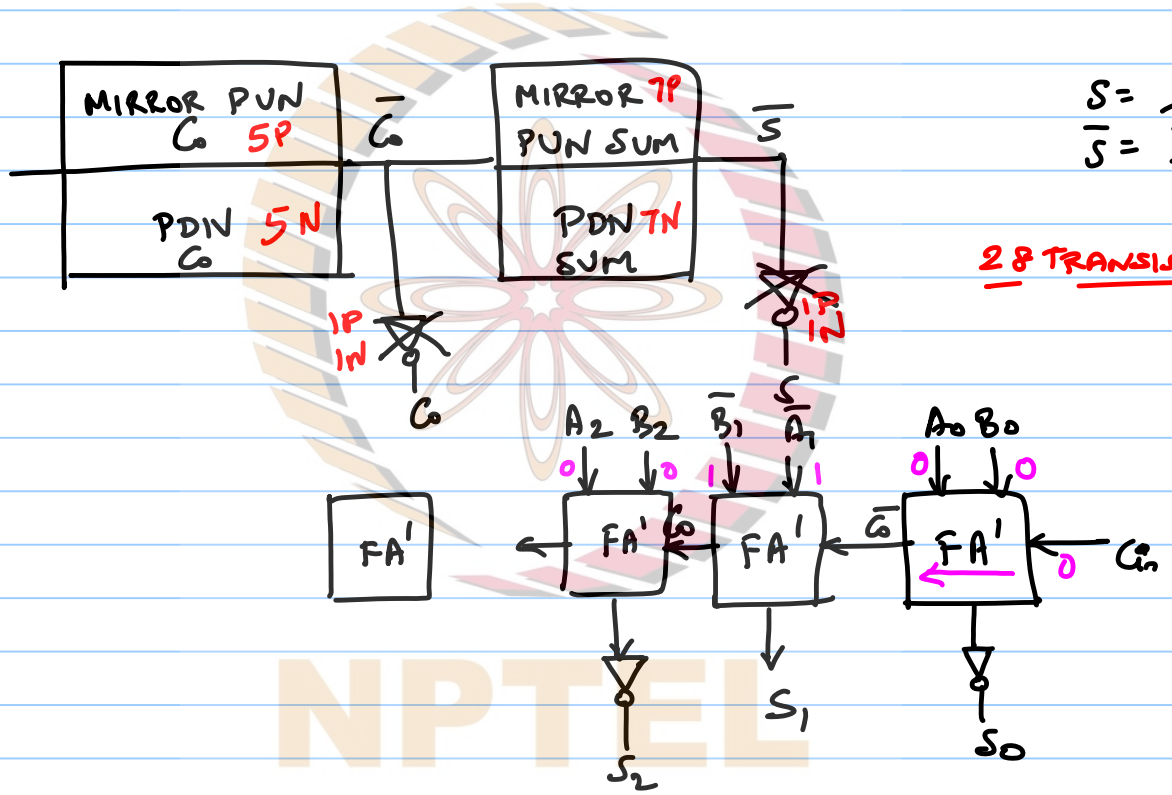

$P = A \oplus B$

$G = AB$

$S = P \oplus C_{in}$

$C_{out} = G + PC_{in}$

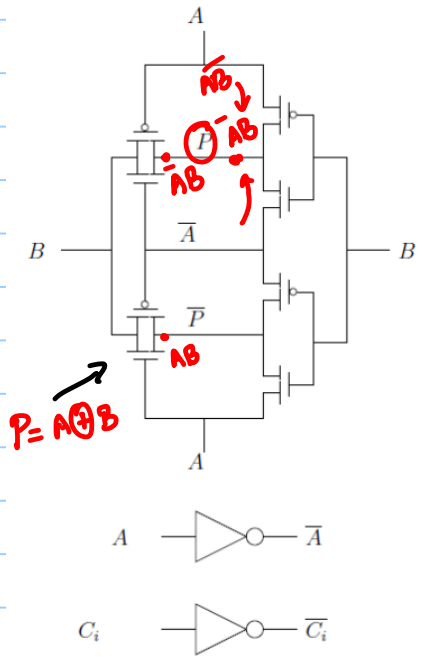
$t_{ripple} = t_{SUM} + (N-1)\, t_{CARRY}$

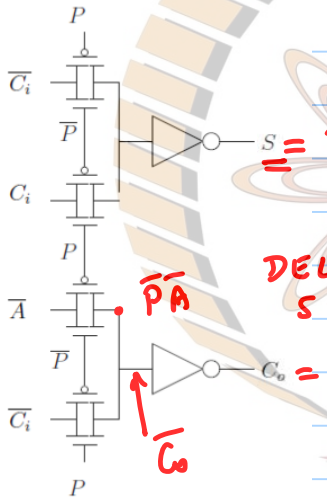



$S = f(A, B, C)$

$\overline{S} = f(\bar{A}, \bar{B}, \bar{C})$

28 TRANSISTORS




$S = P \oplus C_i$

$C_o = G + PC_i$

$= P \oplus C_i$

$P = A\overline{B} + \overline{A}B$

$S = P\overline{C_i} + \overline{P}C_i$

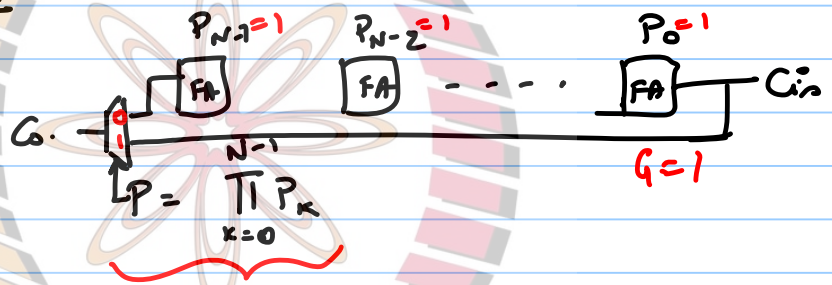
DELAY IS SIMILAR FOR $C_o$ & S

$C_o =$

$C_o = G + PC_i$

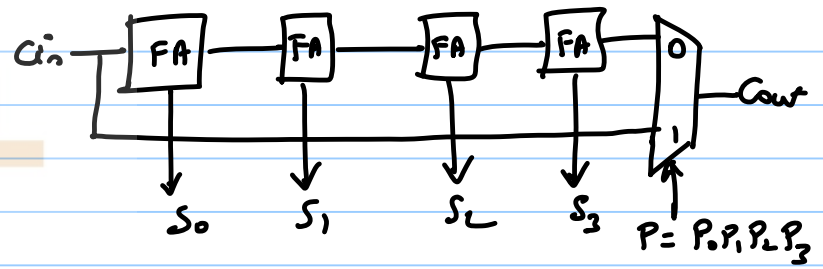
SERVER : 128

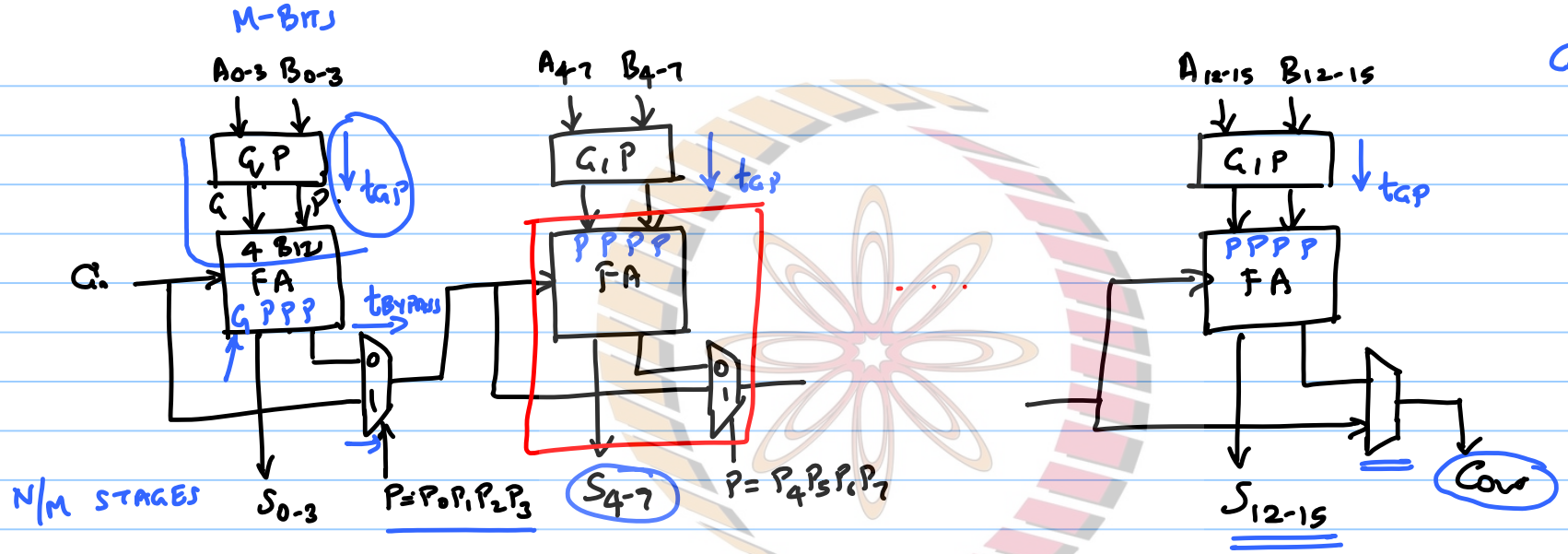
CARRY SKIP ADDER




PARTITION N BITS INTO M BIT SEGMENTS

# STAGES = $\frac{N}{M}$






$C_{out} = G + PC_{in}$

$t_{GP}$ = CREATE GEN/PROP SIGNALS.

$t_{SUM}$ = FA TIME TO CREATE SUM

$t_{CARRY}$ = " " " " Cout

$t_{BYPASS}$ = MUX TIME

$$t_{CARRY\text{-}SKIP} = t_{GP} + M\,t_{CARRY} + \left(\frac{N}{M} - 1\right) t_{BYPASS} + (M-1)\,t_{CARRY} + t_{SUM}$$