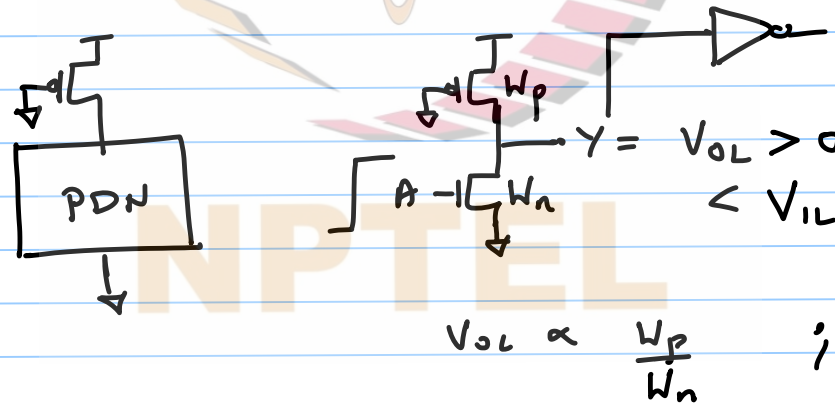


4/10/2019

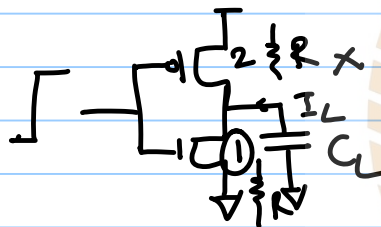
EE5311

## MODULE - 4 - COMBINATIONAL CIRCUITS

### RATIO'ED CIRCUIT / PSEUDO NMOS LOGIC



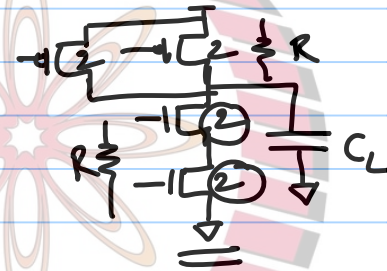
# UNIT INVERTER



$$I_L = |I_n|_{OK}$$

$$I_L = |I_p|$$

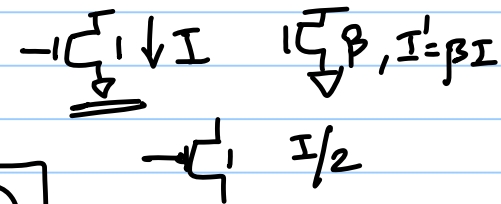
UNIT INV



PULL UP/DOWN RES = R

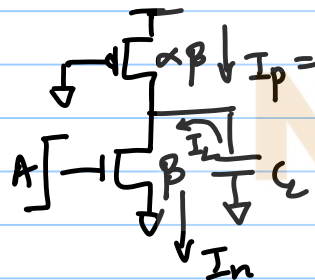
$$\tau = \frac{3}{4} \frac{V_{DD}}{I} \times 0.693 \cdot C$$

$$\tau = \frac{C \Delta V}{I}$$



$$\text{Let } W_n = \beta$$

$$\Rightarrow W_p = \alpha \beta$$



$$\beta = 1 ??$$

$$I_n = I_p + I_L$$

$$I_n = \beta I$$

$$I_p = (\alpha \beta / 2) I$$

$$\beta \frac{L}{2} = \frac{\alpha \beta L}{2} + L$$

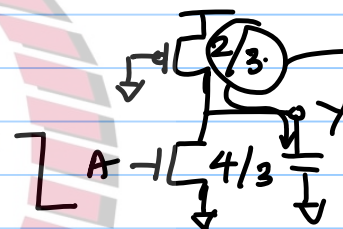
$$\Rightarrow \beta(1 - \alpha/2) = 1$$

$$\therefore \beta = 1/(1 - \alpha/2)$$

$$\alpha = 1/2$$

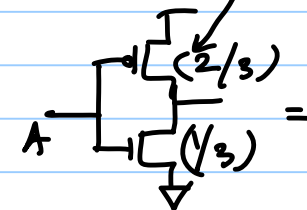
$$\Rightarrow \beta = 4/3$$

UNIT INV: (PSEUDO NMOS)



$$C_A = \frac{4}{3} C$$

PULL UP:

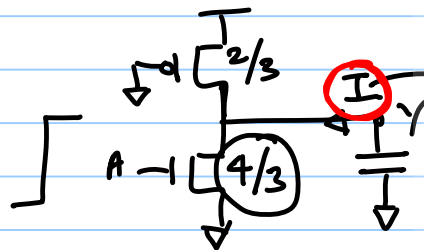


$$C_A = C$$

$$\therefore g_{pu} = 4/3 > 1$$

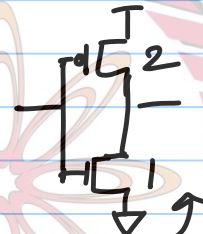
NPTEL

PULL DOWN:



$$C_A = \frac{4}{3} C$$

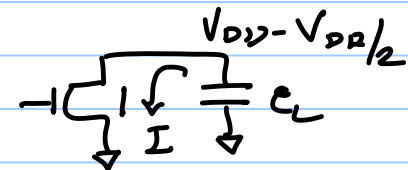
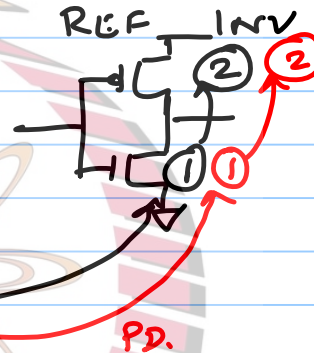
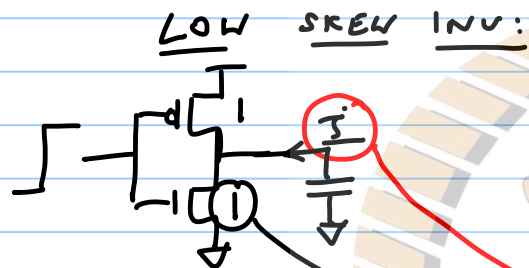
REF INV:



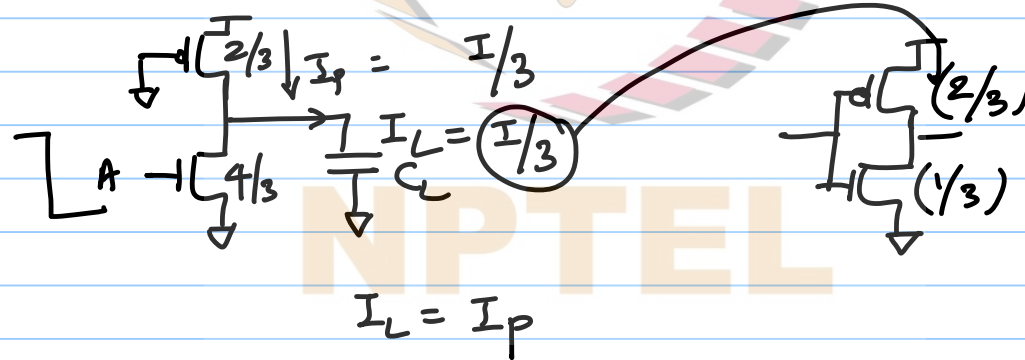
$$C_A = 3 \cdot C$$

$$\therefore g_{pd} = 4/9 < 1$$

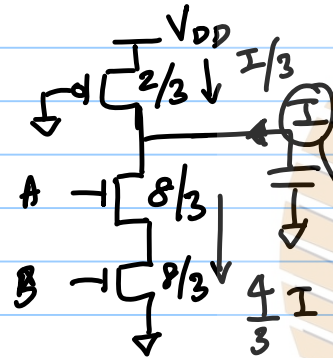
NPTEL



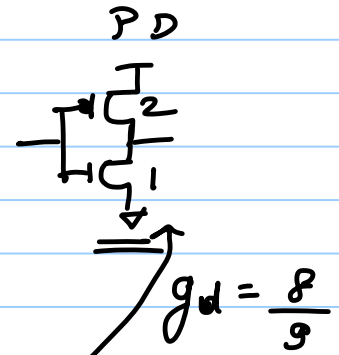
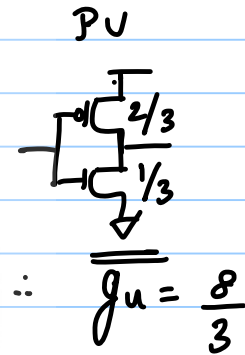
PSEUDO NMOS: PULL UP



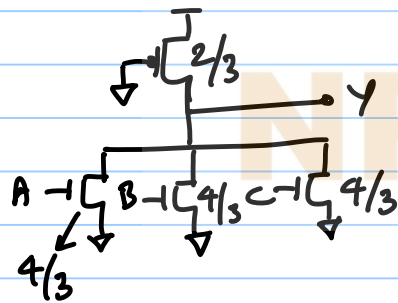
### NAND-2 (PSEUDO NMOS)



$$C_A = C_B = \frac{8}{3} C$$



### NOR-3

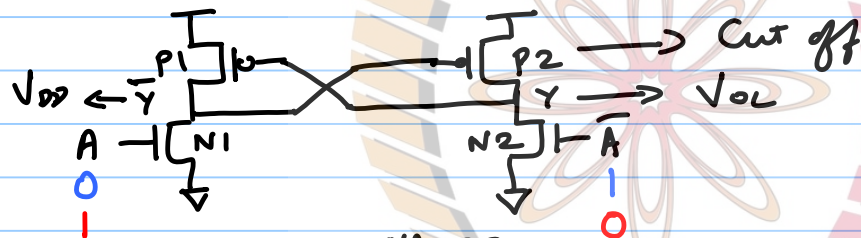


$$g_u = \frac{4}{3}$$

$$g_d = \frac{4}{9}$$

## CASCODE VOLTAGE SWITCH LOGIC

INVERTER



NAND2

