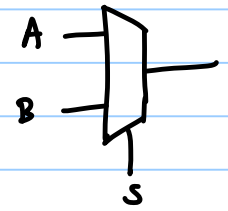
21/10/2019

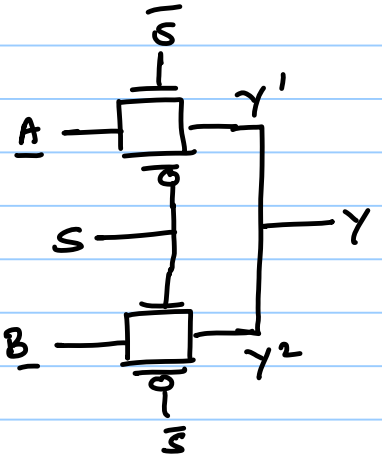
EE5311

MODULE - 4 COMBINATIONAL CIRCUITS

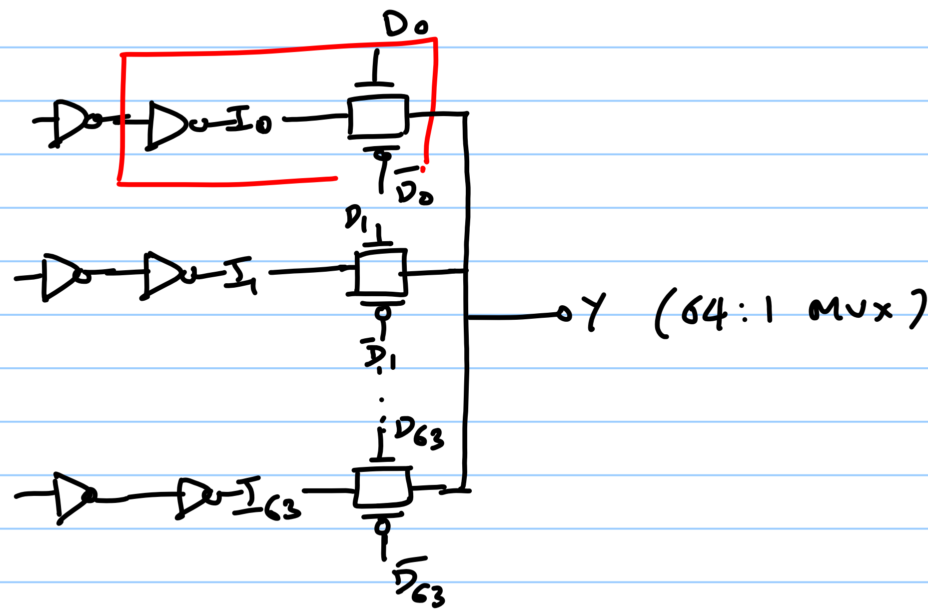
TRANSMISSION GATE CIRCUITS



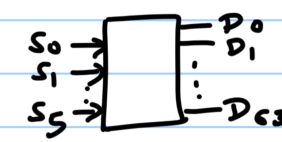
$Y = \bar{S}A + SB$



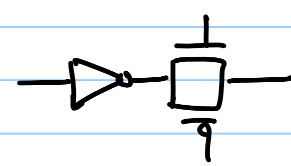
$Y = Y' \text{ (WIRE OR) } Y^2$

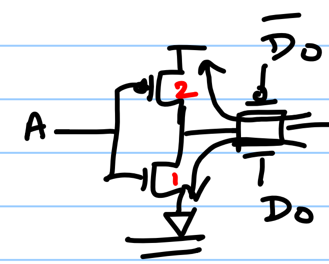


D_0
I_0
$\overline{D_0}$
D_1
I_1
$\overline{D_1}$
D_{63}
I_{63}
$\overline{D_{63}}$
Y (64:1 MUX)

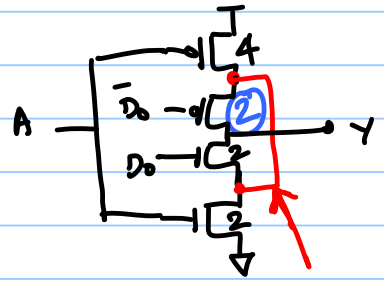


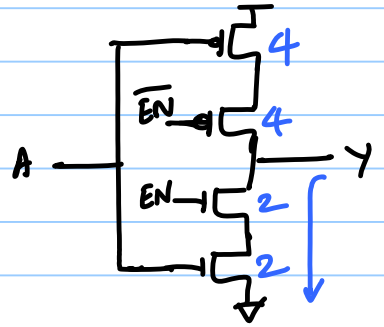
S_0
S_1
S_5
D_0
D_1
D_{63}





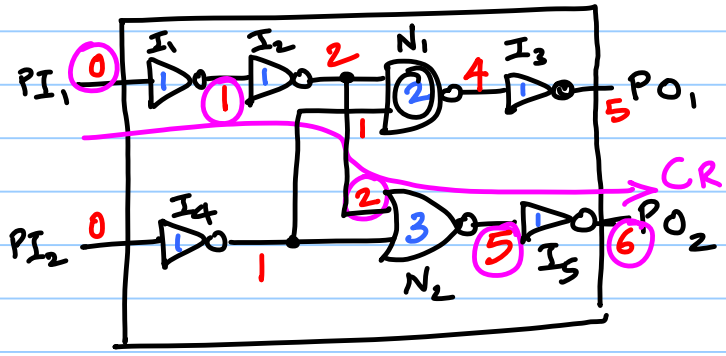
A
$\overline{D_0}$
D_0
2
1





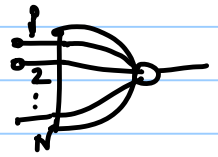
A	EN	Y
0	0	Z
0	1	1
1	0	Z
1	1	0

TRI STATE INVERTER



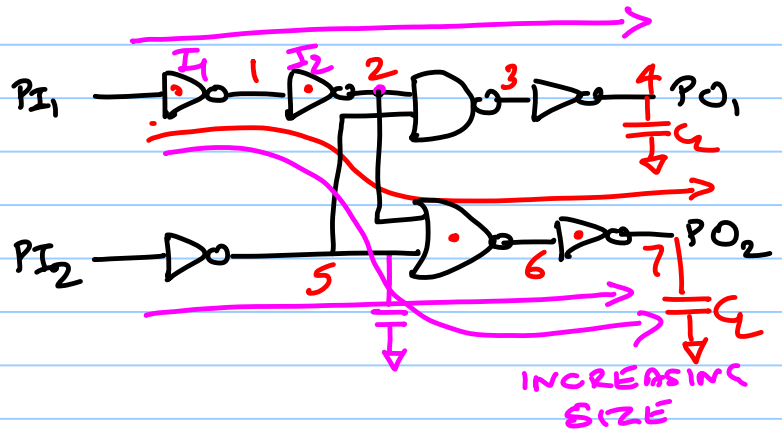
ARRIVAL TIME: MIN TIME AFTER WHICH O/P OF THE GATE IS STABLE

STATIC TIMING ANALYSIS (STA)



$a_o = \max(a_i + d_i)$

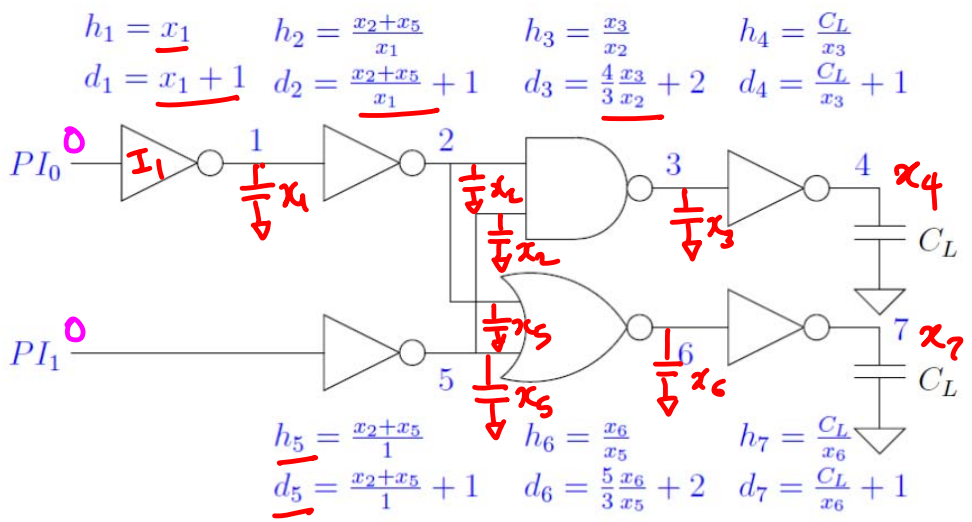
d_i = DELAY FROM i^{th} INPUT TO O/P.



GIVEN: TIMING SPEC

⇒ MAX AT (arrival time) at any PO ≤ T_{SPEC}

PATH SIZING → NOT SCALABLE



Var : $(x_1, x_2 \dots x_7)$

$a_1 \leq (x_1 + 1)$

$a_2 \leq a_1 + d_2$

$a_3 \leq \max(a_2 + d_3, a_5 + d_3)$

$\leq d_3 + \max(a_2, a_5)$

$a_4 \leq a_3 + d_4$

$a_7 \leq a_6 + d_6$.

$\max(a_4, a_7) \leq T_{SPEC}$

$\Rightarrow$ O(N) CONST

MINIMIZE: $\sum x_k$

$\text{MAX}(a_4, a_7) \leq T_{SPEC}$

↳ $a_4 \leq T_{SPEC}$

$a_7 \leq T_{SPEC}$

CONVEX PROBLEM ⇒ SOLUTION IS A GLOBAL MINIMUM