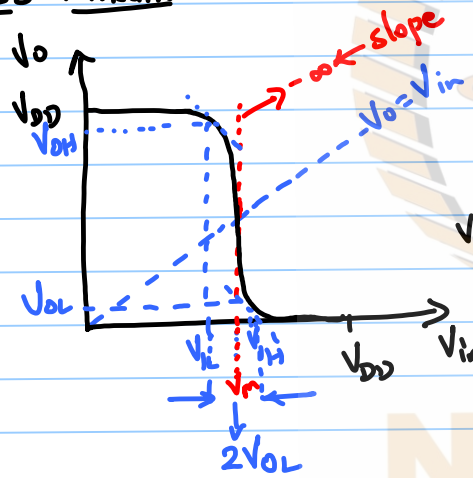
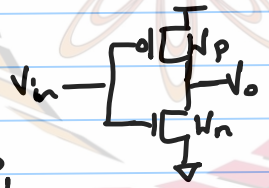
05/09/2019

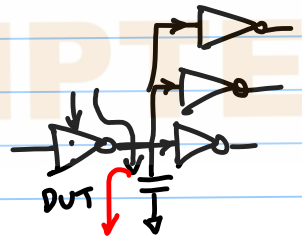
EE5311

MODULE 3 - THE INVERTER

NOISE MARGIN





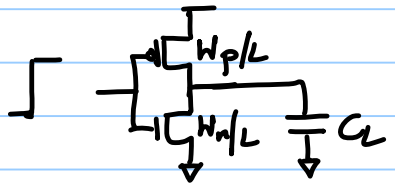


STATIC

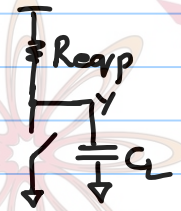
ROBUSTNESS OF CMOS INVERTERS

- ★ RAIL - RAIL VOLTAGE SWING (0 → GND, 1 → VDD)
- ★ RATIOLESS LOGIC (IND OF Wp/Wn)
- ★ O/P IMP IS VERY LOW ⇒ IMMUNE TO NOISE
- ★ ZERO GATE CURRENT ⇒ INFINITE FANOUT
- ★ STEADY STATE CURRENT ~ 0

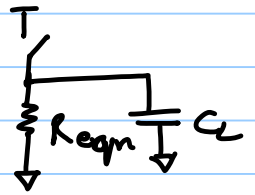
DELAY



O/P RISE



O/P FALL



SWITCH MODEL

τ_{FALL} : FALL DELAY : $0.693 \cdot R_{eqn} C_L$

τ_{RISE} : RISE " : $0.693\, R_{eqp} C_L$

$$R_{eqn} C_L = R_{eqp} \cdot C_L$$

$$\Rightarrow \quad I_{DSATn} = |I_{DSATp}|$$

$$R_{eqn} = \frac{3}{4} \frac{V_{DD}}{I_{DSAT\,n}}$$

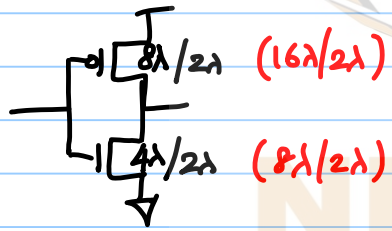
$$R_{eqp} = \frac{3}{4} \frac{V_{DD}}{I_{DSAT\,p}}$$

$$K_n' W_n = |K_p'| W_p$$

$$\Rightarrow \quad \mu_n C_{ox} W_n = \mu_p C_{ox} W_p$$

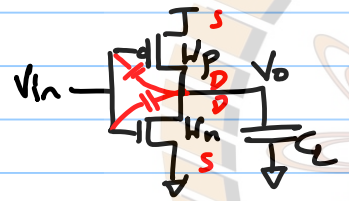
$$\Rightarrow \quad \frac{W_p}{W_n} = \frac{\mu_n}{\mu_p} \quad = \text{FOR EQUAL RISE AND FALL DELAY.}$$

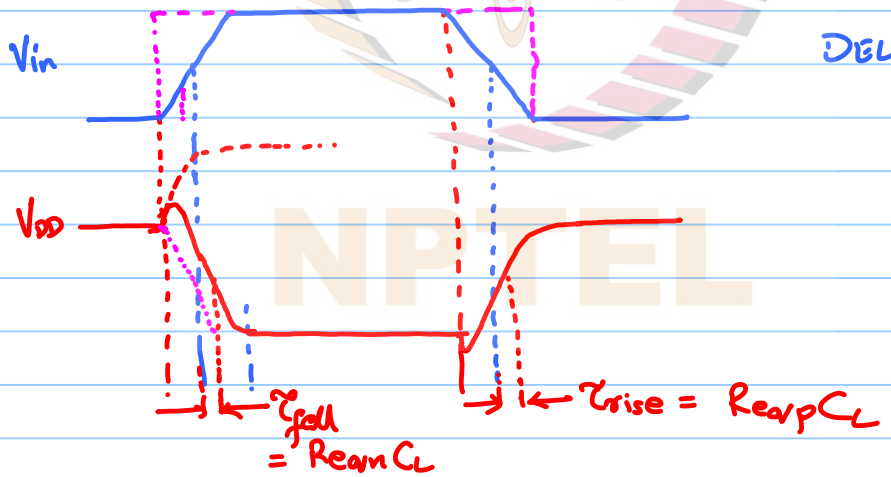
$$\boxed{W_p \simeq 2 W_n}$$



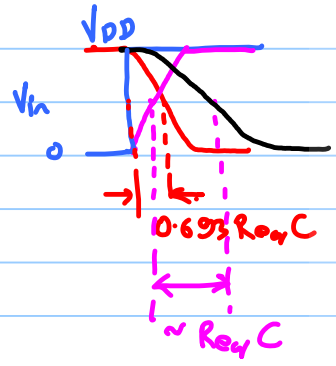
2λ = TECH NODE

TRANSIENT RESPONSE

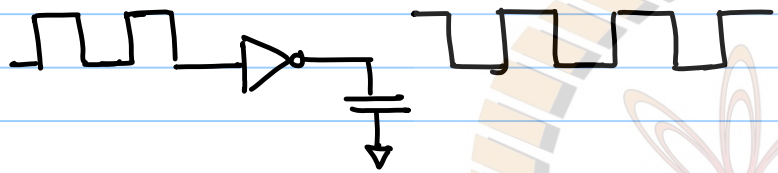


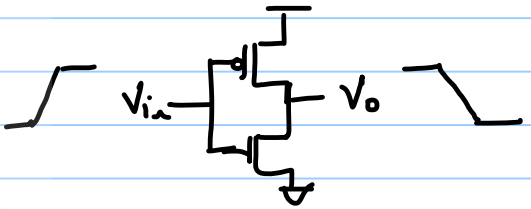


DELAY : INPUT 50% TO OUTPUT 50%


V_{DD}
V_{in}
0
$0.69 R_{eq} C$
$\sim R_{eq} C$

POWER

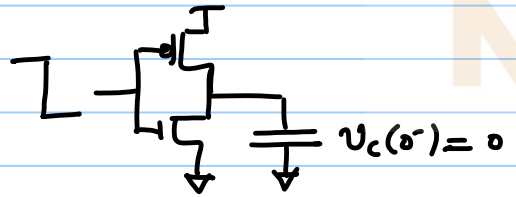




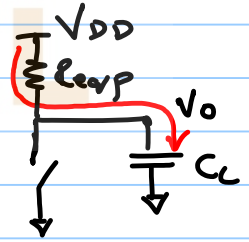
* DYNAMIC POWER
* SWITCHING POWER → SHORT CIRCUIT POWER
* LEAKAGE POWER → STEADY STATE

} SWITCHING

DYNAMIC POWER / ENERGY



$\Rightarrow$



$$i_c(t) = C_L \cdot \frac{dV_o}{dt}$$

$$E_{V_{DD}} = \int_0^\infty V_{supp}(t) \cdot i(t)\, dt$$

$$E_{V_{DD}} = \int_0^{V_{DD}} V_{DD} \cdot C_L \frac{dV_o}{dt} \cdot dt = C_L V_{DD}^2$$

$$E_C = \int_0^{\infty} V_o \cdot i(t)\, dt = \int_0^{V_{DD}} V_o \cdot C_L\, dV_o = \frac{1}{2} C_L V_{DD}^2$$

FOR EVERY CHARGE: $\frac{1}{2} C_L V_{DD}^2$ is dis in the PMOS Transistor

FOR " DISCHARGE: " " " " NMOS