08/08/2019

EE5311

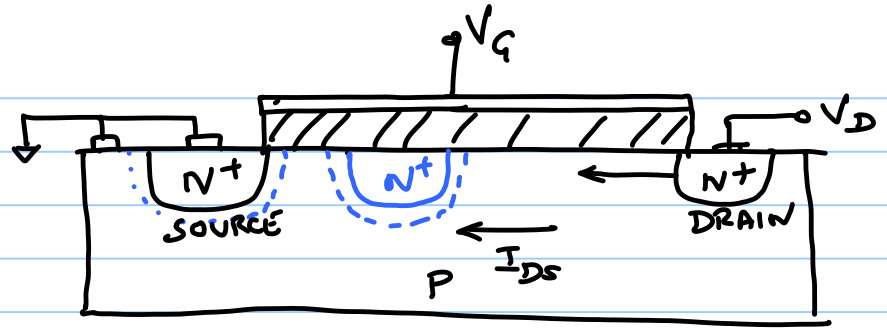
MODULE-1: THE TRANSISTOR

SHORT CHANNEL EFFECTS (SCE)

1) CHANNEL LENGTH MODULATION (CLM) $\rightarrow$ $\frac{\Delta L}{L} = \lambda V_{DS}$

$$I_D = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)^2 (1 + \lambda V_{DS})$$

2) VELOCITY SATURATION:



$V_{DD} \downarrow$ WITH TECH

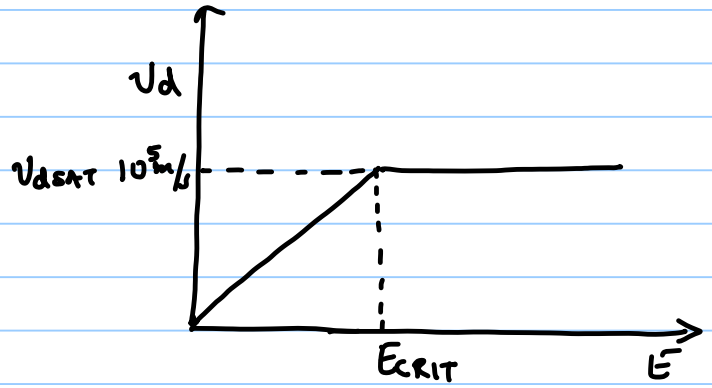
$$E = \frac{V_{DS}}{L}$$

v_d = drift vel $\leq 10^5$ m/s

$$v_d = \mu_n E$$

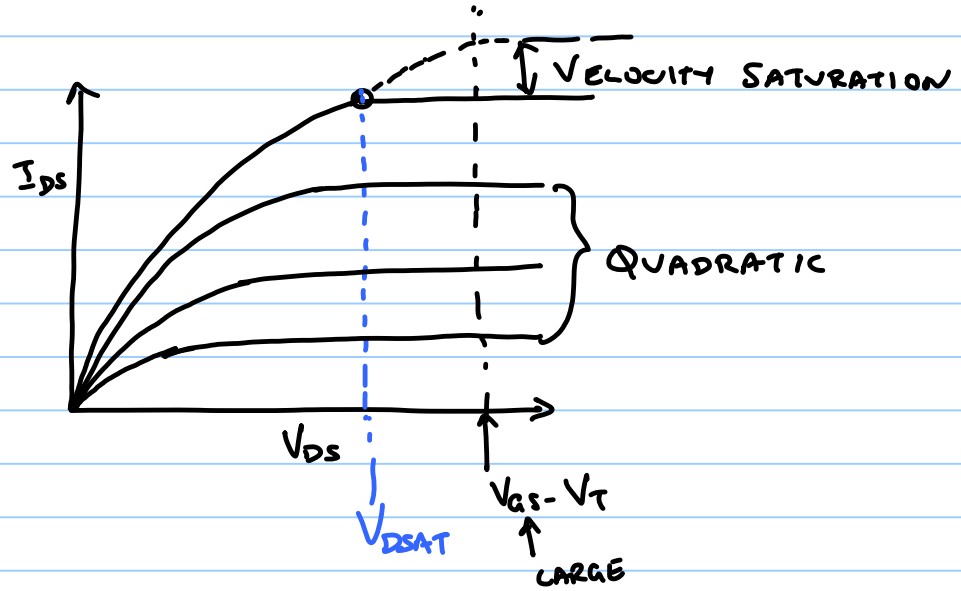
$$v_{dSAT} = \mu_n \cdot \frac{V_{DSAT}}{L}$$

$$\therefore \quad V_{DSAT} = \frac{v_{DSAT} \cdot L}{\mu_n}$$



$V_{GS} \rightarrow$ SMALL ($>V_T$)

$V_{GS} \rightarrow$ LARGE



$$I_D = \begin{cases} 0 & V_{GS} < V_T \\ \mu_n C_{ox} \frac{W}{L} V_{DS}\left[(V_{GS}-V_T) - \frac{V_{DS}}{2}\right] & V_{DS} \le V_{GS}-V_T \rightarrow \text{LINEAR (TRIODE)} \\ \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(V_{GS}-V_T)^2 \rightarrow V_{DS} = V_{GS}-V_T & V_{DS} > V_{GS}-V_T \rightarrow \text{(SATURATION)} \\ \mu_n C_{ox} \frac{W}{L} V_{DSAT}\left[(V_{GS}-V_T) - \frac{V_{DSAT}}{2}\right] & V_{DSAT} < V_{GS}-V_T \text{ (VEL SAT)} \end{cases}$$

UNIFIED CURRENT MODEL

$$I_D = \underbrace{\mu_n C_{ox}}_{k_n'} \frac{W}{L} V_{min}\left[(V_{GS}-V_T) - \frac{V_{min}}{2}\right](1+\lambda V_{DS})$$

$\lambda \hookrightarrow \frac{\Delta L}{L}$

$$V_{min} = \min(V_{GS}-V_T,\ V_{DS},\ V_{DSAT})$$

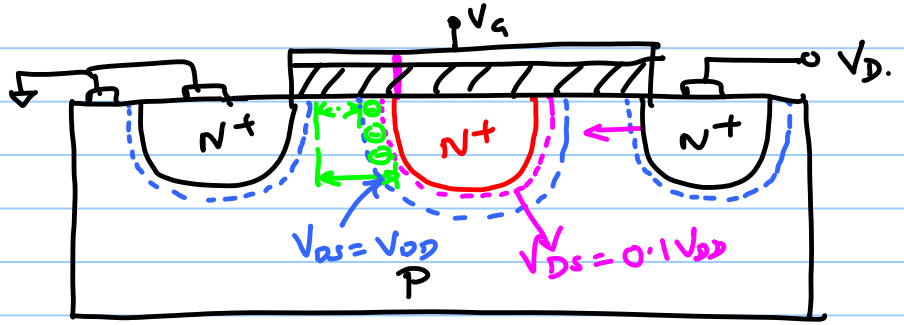
$V_{GS}-V_T$ → SAT; V_{DS} → LIN; V_{DSAT} → VEL SAT.

$$V_{TH} = V_{THO} + \gamma\left(\sqrt{|V_{SB}+2\psi_s|} - \sqrt{|2\psi_s|}\right)$$

5 PARAMETERS: $(k_n', V_{DSAT}, \lambda, V_{THO}, \gamma)$ ← LEVEL 1 SPICE MODEL (TECHNOLOGY PARAMETERS)

$$k_n' = \mu_n C_{ox} = \mu_n \frac{\varepsilon_{ox}}{t_{ox}}$$

DRAIN INDUCED BARRIER LOWERING (DIBL)

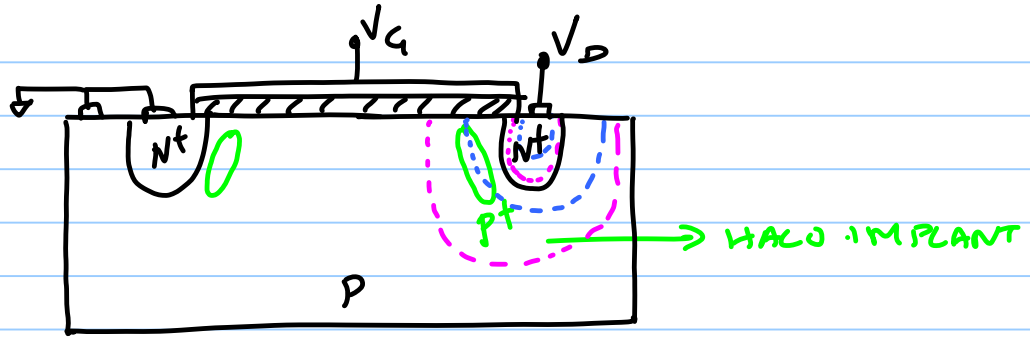


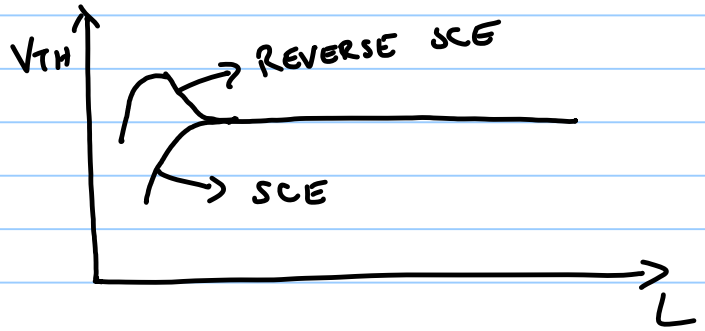
$V_{DS1} = 0.1 V_{DD} \rightarrow V_{TH} = V_{TLIN}$

$V_{DS2} = V_{DD} \rightarrow V_{TH} = V_{TSAT}$

$$\eta = DIBL = \frac{V_{TLIN} - V_{TSAT}}{(V_{DD} - 0.1 V_{DD})}$$

$$V_{TH} = V_{TH0} + \gamma \left(\sqrt{|V_{SB} + 2\Psi_s|} - \sqrt{|2\Psi_s|} \right) - \eta V_{DS}$$


V_G
V_D
N^+
N^+
P^+
HALO IMPLANT
P


V_{TH}
REVERSE SCE
SCE
L