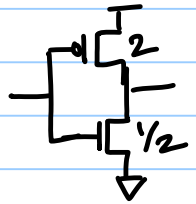
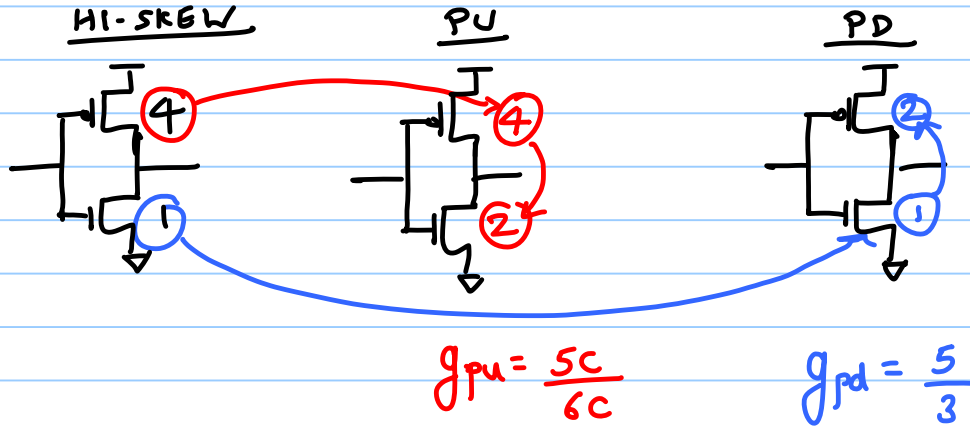
11/10/2019

EE5311

MODULE-4 : COMBINATIONAL CIRCUITS

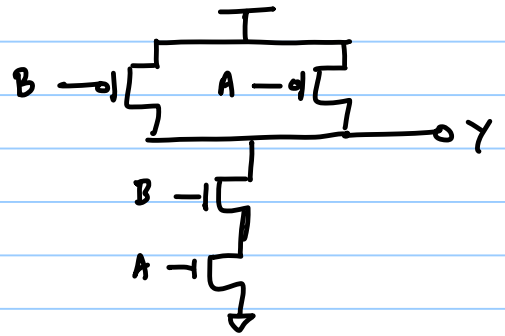
HI-SKEW INV





$g_{pu} = \frac{5C}{6C}$ $\quad g_{pd} = \frac{5}{3}$

SPECIAL FUNCTIONS



$Y_{PD} = \overline{AB}$

$Y_{PU} = \bar{A} + \bar{B}$

$Y_{PD} = Y_{PU}$

$$Y_{PD} = \bar{f}(A_1, A_2 \ldots A_N)$$

$$Y_{PU} = g(\bar{A}_1, \bar{A}_2 \ldots \bar{A}_N)$$

$$Y_{PD} = Y_{PU}$$

IF PMOS STACK (PUN) WAS A MIRROR IMAGE OF PDN

$$Y_{PU} = f(\bar{A}_1, \bar{A}_2 \ldots \bar{A}_N)$$

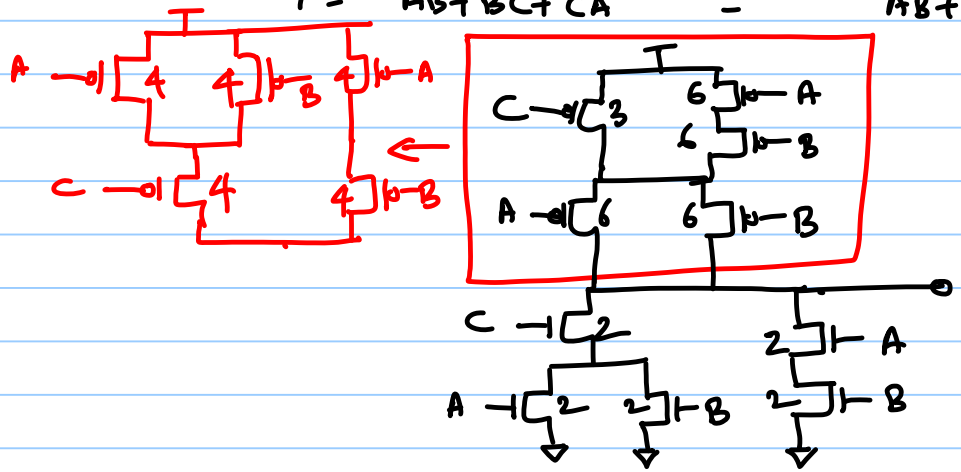
GIVEN

$$Y_{PD} = \bar{f}(A_1, A_2, \ldots A_N)$$

$$f(\bar{A}_1\, \bar{A}_2 \ldots \bar{A}_N) = \bar{f}(A_1\, A_2 \ldots A_N)$$

$$Y = \overline{AB + BC + CA}$$

$$Y = \overline{AB + BC + CA} = \overline{AB + C(A+B)}$$



A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

$$Y = \sum m(0,1,2,4)$$

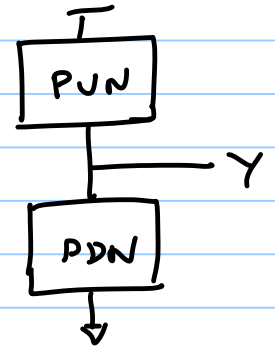
$$\overline{Y} = \sum m(3,5,6,7)$$

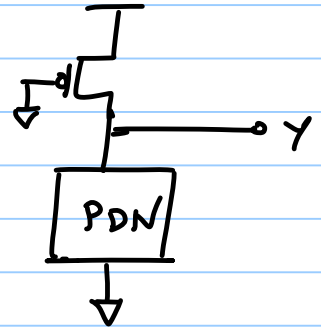
$$Y = A \oplus B \oplus C$$

PMOS CAN KILL YOUR LOGICAL EFFORT

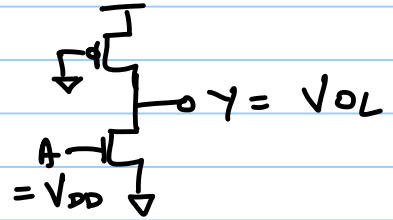
RATIO'D CIRCUITS (PSEUDO NMOS LOGIC)

STATIC CMOS





$V_{OL} > 0$



	V_{GS}	V_{DS}	REGION
NMOS	V_{DD}	V_{OL}	LIN
PMOS	$-V_{DD}$	$V_{OL}-V_{DD}$	VEL SAT

$$I_{DSn} = K_n' \frac{W_n}{L} \cdot V_{OL}\left[\overbrace{(V_{DD}-V_{Tn})}^{\sim (V_{DD}-V_{Tn})} - \frac{V_{OL}}{2}\right]$$

$$I_{DSp} = K_p' \frac{W_p}{L} \cdot V_{DSATp}\left[(-V_{DD}-V_{Tp}) - \frac{V_{DSATp}}{2}\right]$$

$\therefore$ $I_{DSp} = -I_{DSn}$

$$\Rightarrow + K_p' \frac{W_p}{L} V_{DSATp}\left[(V_{DD}+V_{Tp}) + \frac{V_{DSATp}}{2}\right] = - K_n' \frac{W_n}{L} \cdot V_{OL}(V_{DD}-V_{Tn})$$

$$\Rightarrow V_{OL} = \frac{K_p' \cdot W_p \cdot V_{DSATp}\left[(V_{DD}+V_{Tp}) + V_{DSATp}/2\right]}{K_n' \cdot W_n (V_{DD}-V_{Tn})}$$

$$\Rightarrow V_{OL} = \frac{K_p' W_p}{K_n' W_n} \cdot V_{DSATp} \cdot \Rightarrow (W_p/W_n) = V_{OL} \cdot \frac{K_n'}{K_p' \cdot V_{DSATp}}$$

$$\frac{W_p}{W_n} = \alpha$$