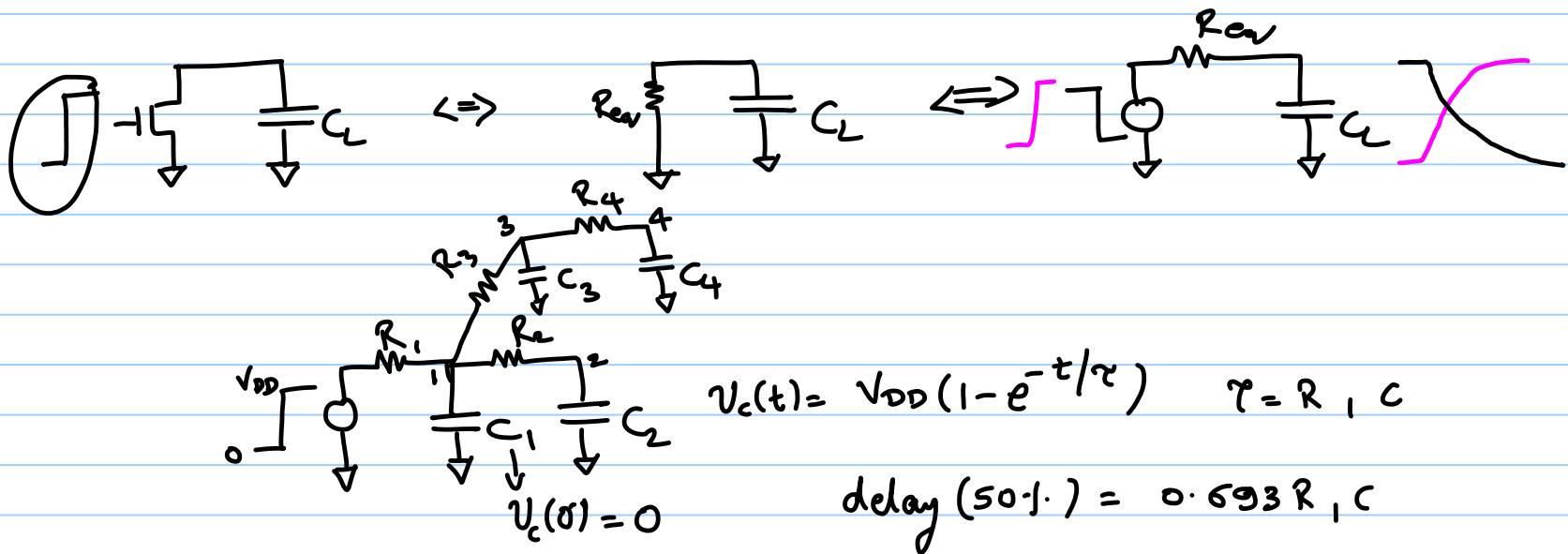


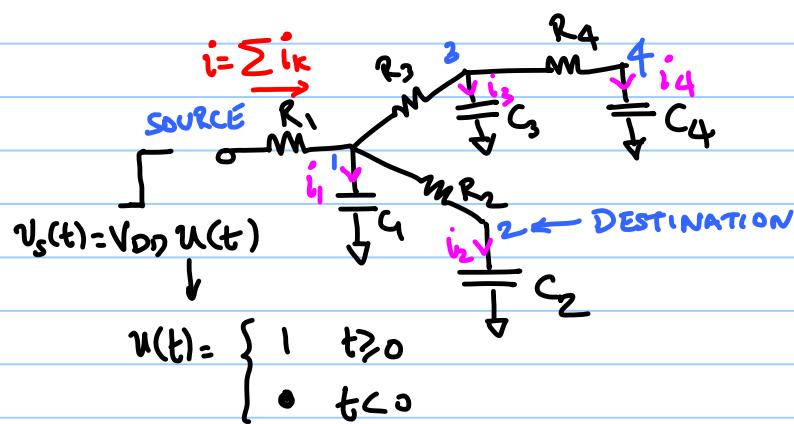
22/08/2019

EES311

MODULE - 2 - INTERCONNECTS



ELMORE DELAY MODEL



$$i_k(t) = C_k \frac{dV_k}{dt}$$

$$V_s(t) - V_2(t) = (\sum i_k) R_1 + i_2 R_2$$

$V_k(t) = V_{ck}(t) =$ Voltage across caps C_{ik}

$$\tau_{s2} = \tau_\Sigma$$

OBSERVATION:

1) If $V_{ck}(t) = V_{DD}$.
 $t \rightarrow \infty$.

2) Majority: τ_Σ not dep on C_2 or C_4
 $\tau_\Sigma \sim \frac{1}{R_3 + R_4}$

ASSUMPTION:

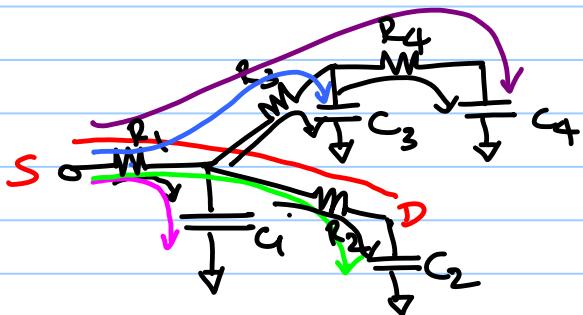
- 1) SOURCE is $V_{DD} u(t)$ ←
- 2) RC TREE
- 3) ALL CAPACITORS ARE BETWEEN nodes & GND
- 4) $u_k(t) = V_{DD} (1 - e^{-t/\tau_k})$

$\tau_2 \rightarrow$ TIME CONSTANT OF node 2

$$(V_{DD} u(t) - V_{DD} (1 - e^{-t/\tau_2}) u(t)) = R_1 \sum C_k \frac{d u_k}{dt} + R_2 C_2 \frac{d u_2}{dt}$$
$$\Rightarrow \int_0^\infty V_{DD} e^{-t/\tau_2} u(t) dt = \int_0^{V_{DD}} R_1 \sum C_k d u_k + \int_0^{V_{DD}} R_2 C_2 d u_2$$
$$= V_{DD} \cdot \tau_2 = R_1 (\sum C_k) V_{DD} + R_2 C_2 V_{DD}$$

$$\Rightarrow \tau_2 = R_1 \sum_{k=1}^4 C_k + R_2 C_2$$

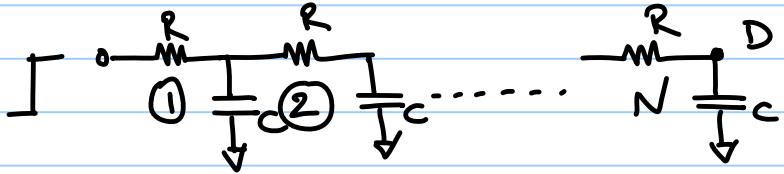
- 1) DOES NOT DEPEND ON R_3 & R_4
- 2) DEPENDS ON EVERY CAP IN THE CIRCUIT



$$\begin{aligned}\tau_2 = & R_1 C_1 + \\ & (R_1 + R_2) C_2 + \\ & R_1 C_3 + \\ & R_1 C_4\end{aligned}$$

$$\tau_3 = R_1 C_1 + R_1 C_2 + (R_1 + R_3) C_3 + (R_1 + R_3) C_4$$

$$\tau_4 = R_1 C_1 + R_1 C_2 + (R_1 + R_3) C_3 + \frac{C_4}{(R_1 + R_3 + R_4)}$$



$$T = RC + 2RC + 3RC + \dots + NRC$$

$$= \frac{N(N+1)}{2} RC.$$

$$V_k(0^-) = a_k$$

$$C_2 = R_1 \sum C_k + R_2 C_2$$

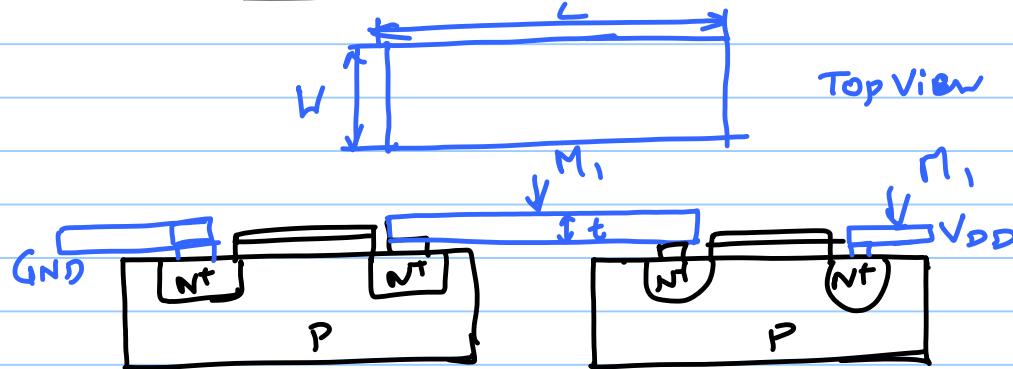
$$\Rightarrow V_{DD} C_2 = R_1 \sum C_k (V_{DD} - a_k) + R_2 C_2 (V_{DD} - a_k)$$

$$D_K = \text{DELAY (50%)} = 0.693 \tau_K$$

↓
(DROP)

$$\boxed{\text{Delay} = \tau_K}$$

INTER CONNECT

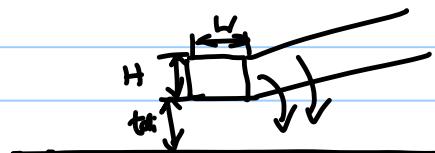
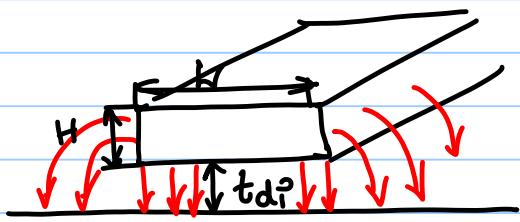


L → DESIGN PARAM

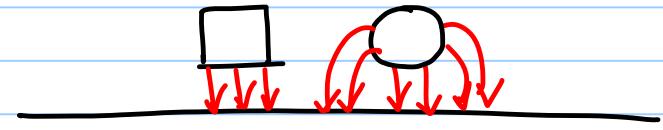
t → Tech PARAM

W → SEMI (DESIGN/Tech)





$$\text{CAPACITANCE} = \frac{\epsilon_{ox} WL}{t_{d\ell}}$$



$$C_{||} = \frac{\epsilon_{ox} WL}{t_{d\ell}} =$$

$$C_{cyl} = \frac{2\pi \epsilon_{ox}}{\log(t_{d\ell}/H)}$$