EE5311

MODULE-5- SEQUENTIAL CIRCUITS

t_{pcq} t_{ccq}

$t_{DC} = t_{SETUP}$

t_{DC}

t_{cq}

t_{DQ}

D

CLK

Q

$t_{DQ} = t_{DC} + t_{cq}$

CLK
t_{DC}
D
t_{cq}
Q

$\overline{D}$

$\overline{CLK}$ I_1 X_m CLK Q_m $\overline{I_2}$ CLK X $\overline{CLK}$ Q.

$\overline{CLK}$

Q

D.

$\overline{CLK}$

CLK

$\rightarrow T_{cq}$
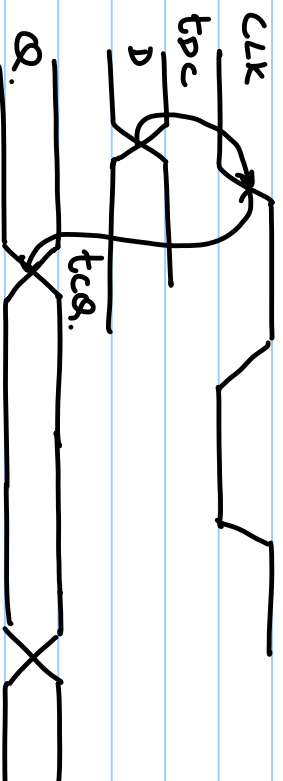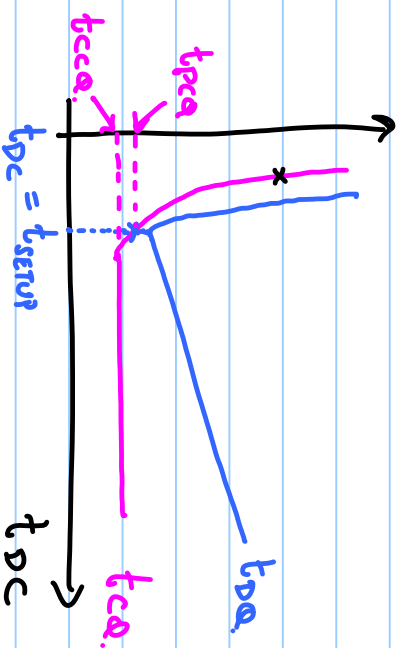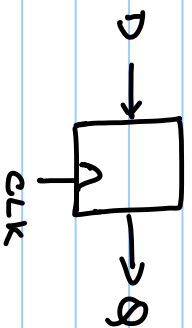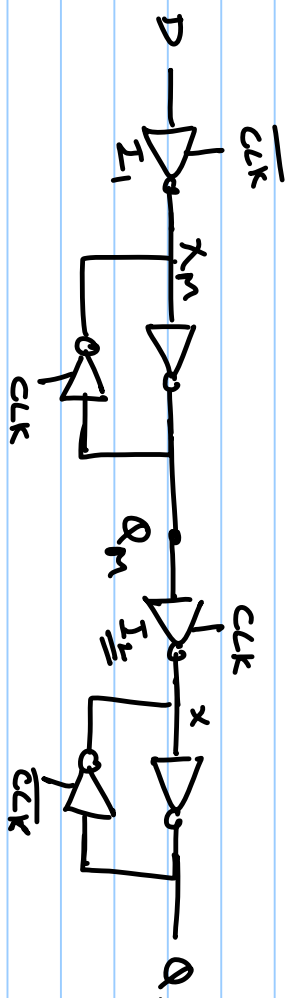
Q_m & Q.
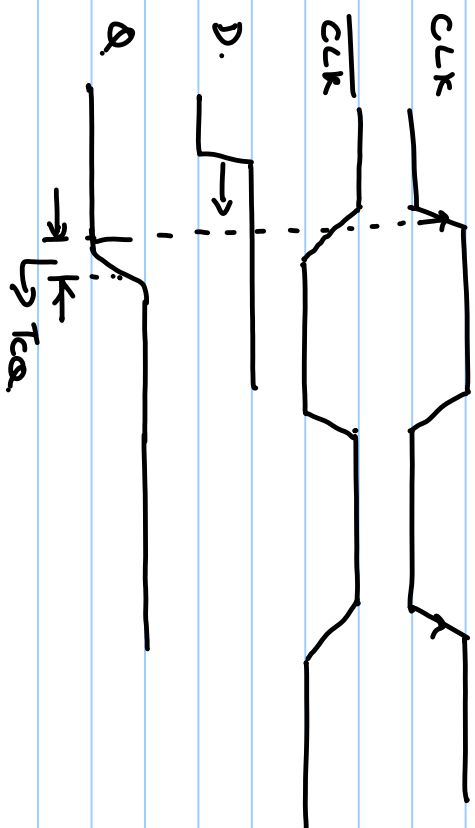
COMB BLOCKS → t_{CD}, t_{PD}.

SEQ ELEMENTS → t_{CCQ}, t_{PCQ}, t_{SETUP}, t_{HOLD}.
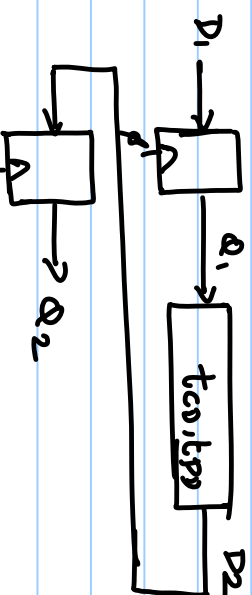
SYSTEM DELAY CONSTRAINTS
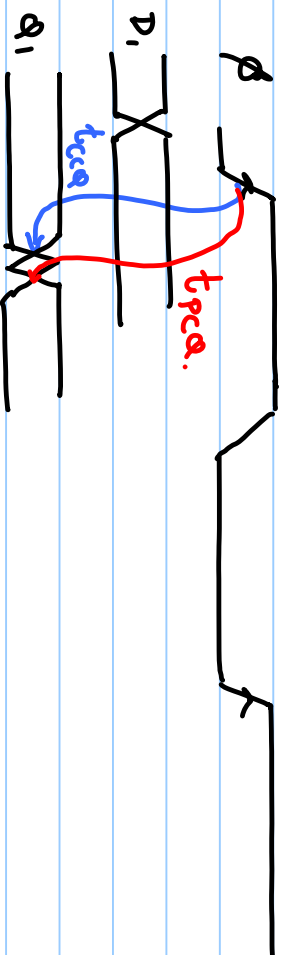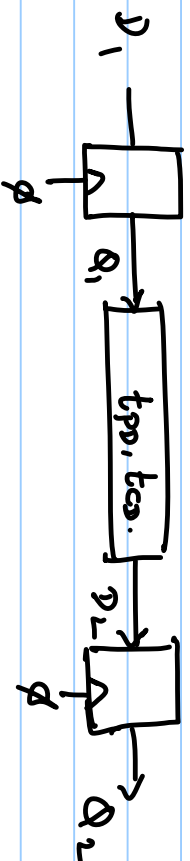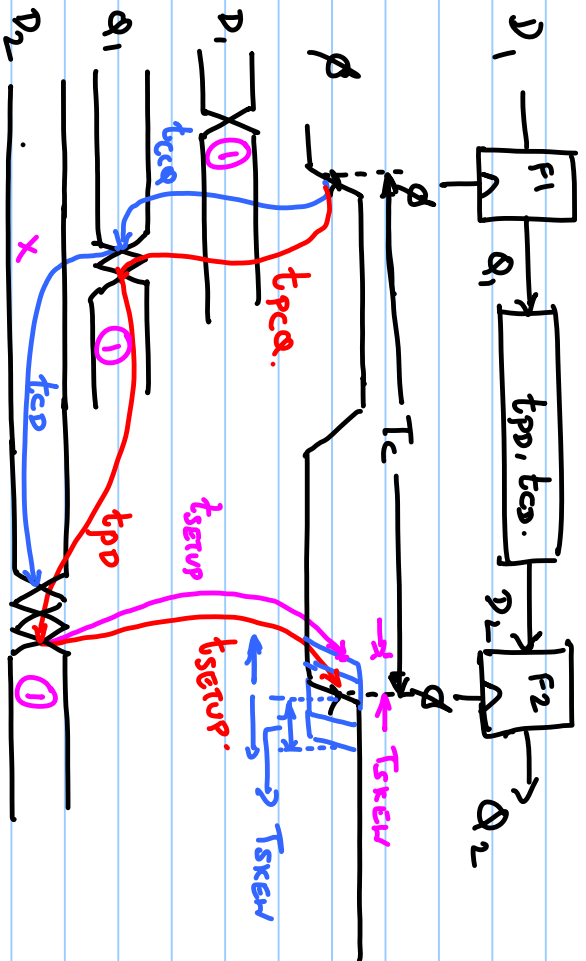
MAX DELAY CONSTRAINT

$$T_c \geq t_{pcq} + t_{pd} + t_{setup} + t_{skew}$$

$$\Rightarrow t_{pd} \leq T_c - \underbrace{(t_{pcq} + t_{setup} + t_{skew})}_{\substack{\text{SEQUENCING} \\ \text{OVERHEAD}}}$$

MIN DELAY CONSTRAINT

$$t_{skew} + t_{hold} \le t_{ccq} + t_{cd} \quad —① $$

$$\Rightarrow t_{cd} \ge t_{hold} - t_{ccq} + t_{skew} \quad —②$$