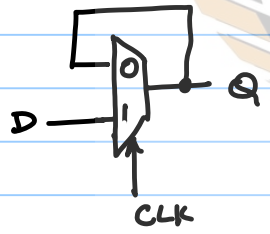
01/11/2019

EE5311

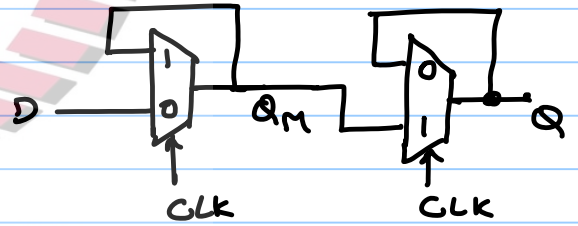
MODULE-5 - SEQUENTIAL CIRCUITS

LATCH → LEVEL SENSITIVE (+ve) → IF CLK == 1 Q = D;

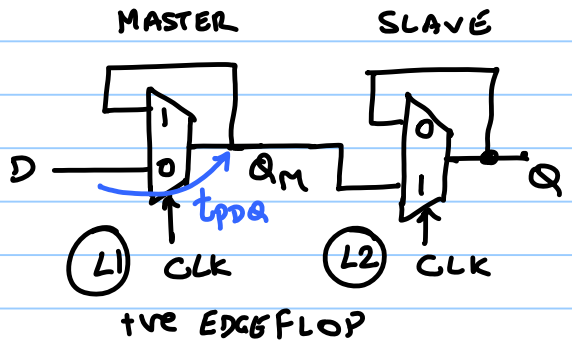
FLOP → EDGE TRIG. else $Q_{n+1} = Q_n$;

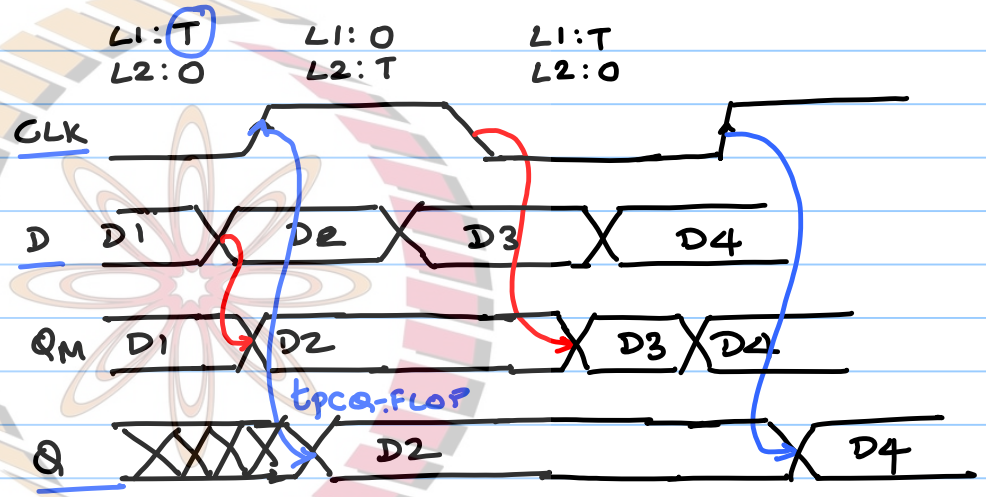


+ve LATCH



+ve EDGE FLOP





$t_{pCQ-FLOP} = t_{pCQ-L2}$

$t_{SETUP-FLOP} = t_{SETUP-L1}$

CIRCUIT IMPLEMENTATION