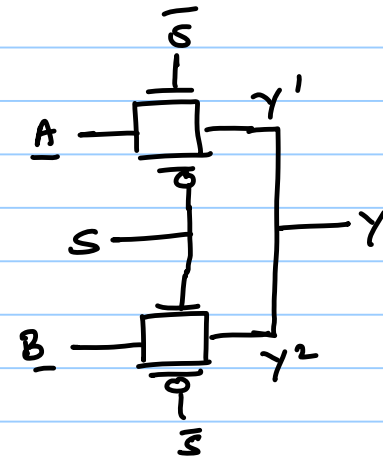
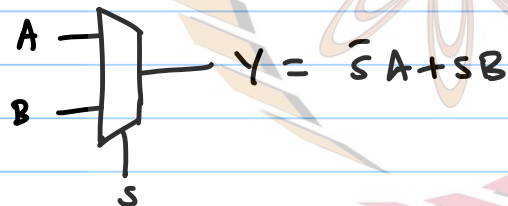


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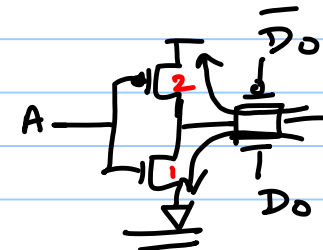
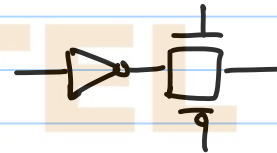
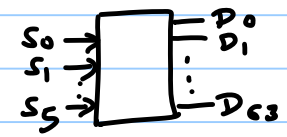
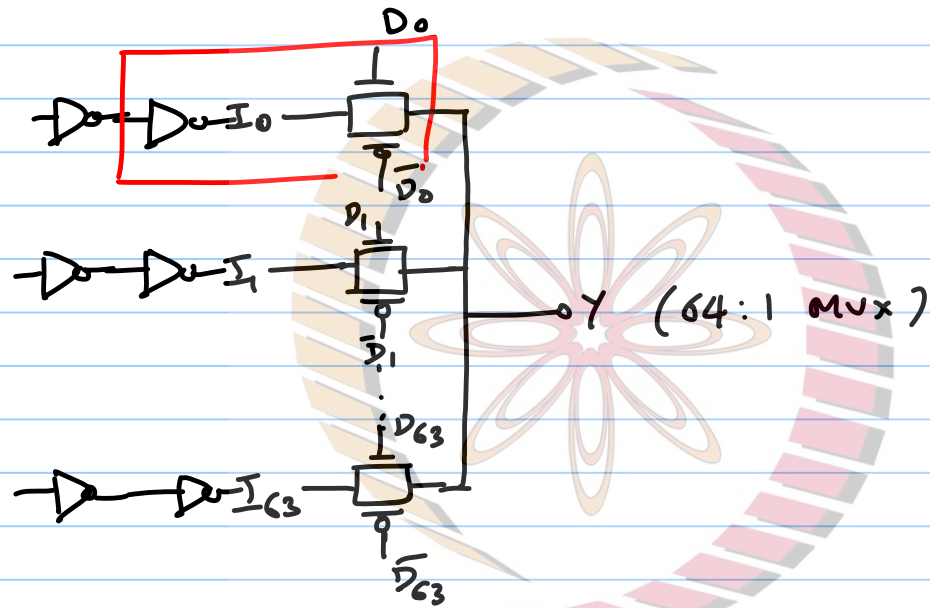
MODULE - 4 COMBINATIONAL CIRCUITS

TRANSMISSION GATE CIRCUITS

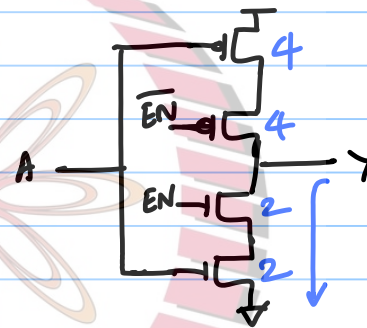
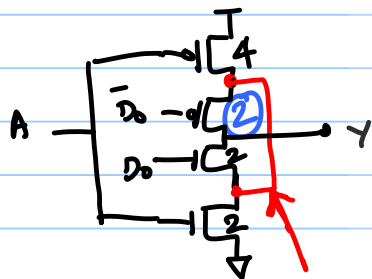


$$Y = Y' (\text{WIRE OR}) Y^2$$

NPTEL



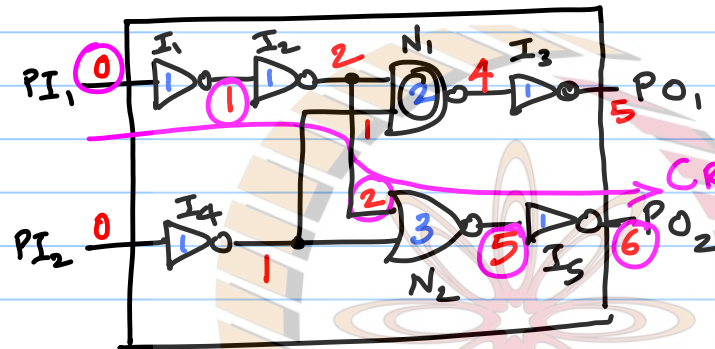
NPTTEL



A	EN	Y
0	0	2
0	1	1
1	0	2
1	1	0

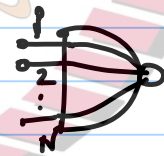
TRI STATE INVERTER

NPTTEL



STATIC TIMING ANALYSIS (STA)

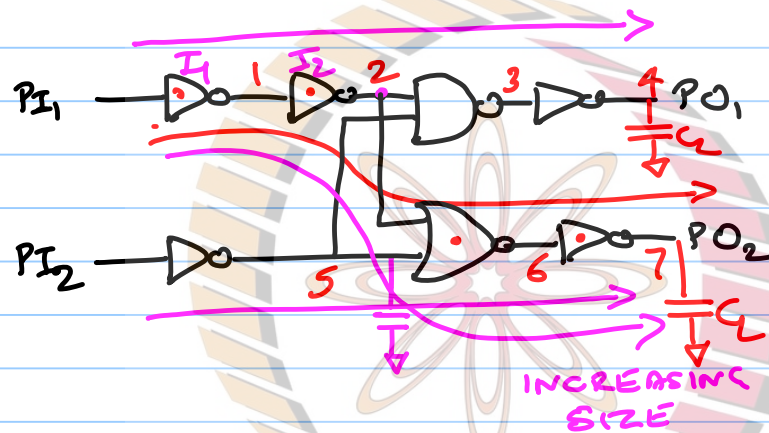
ARRIVAL TIME: MIN TIME
AFTER WHICH
OP OF THE
GATE IS
STABLE



$$a_0 = \max(a_i + d_i)$$

d_i = DELAY FROM i^{th} INPUT
TO O/P.

NPTEL

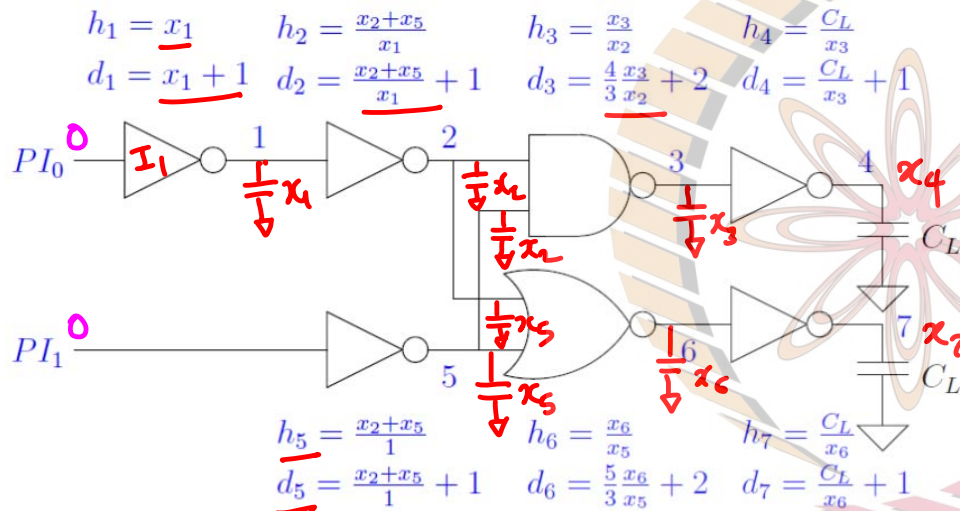


GIVEN: TIMING SPEC

\Rightarrow MAX AT (arrival time)
at any $PO \leq T_{SPEC}$

PATH SIZING \rightarrow NOT SCALABLE

NPTEL



Var : (x_1, x_2, \dots, x_7)

$$a_1 \leq (x_1 + 1)$$

$$a_2 \leq a_1 + d_2$$

$$a_3 \leq \max(a_2 + d_3, a_5 + d_3)$$

$$\leq d_3 + \max(a_2, a_5)$$

$$a_4 \leq a_3 + d_4$$

$$a_7 \leq a_6 + d_6$$

$$\max(a_4, a_7) \leq T_{spec}$$

$$\Rightarrow O(N) \text{ CONST}$$

NPTEL

MINIMIZE: $\sum x_k$

$$\max(a_4, a_7) \leq T_{\text{SPEC}}$$



$$a_4 \leq T_{\text{SPEC}}$$

$$a_7 \leq T_{\text{SPEC}}$$

CONVEX PROBLEM \Rightarrow SOLUTION IS A GLOBAL MINIMUM

NPTEL