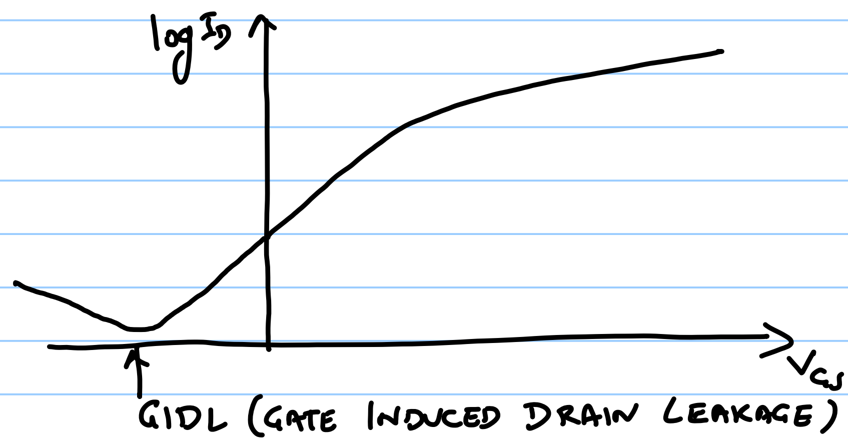
4/08/2019

EE5311

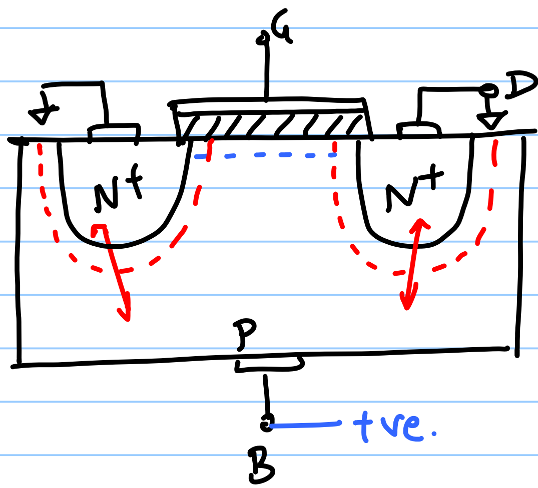
Module 1 - The Transistor

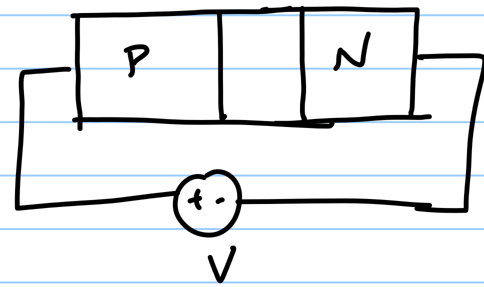
SubThreshold Leakage:

$$I_{SUB} = I_{OFF} = I_0\, e^{\frac{V_{GS}-V_T}{n\phi_T}} \left(1 - e^{-V_{DS}/\phi_t}\right)\left(1+\lambda V_{DS}\right)$$

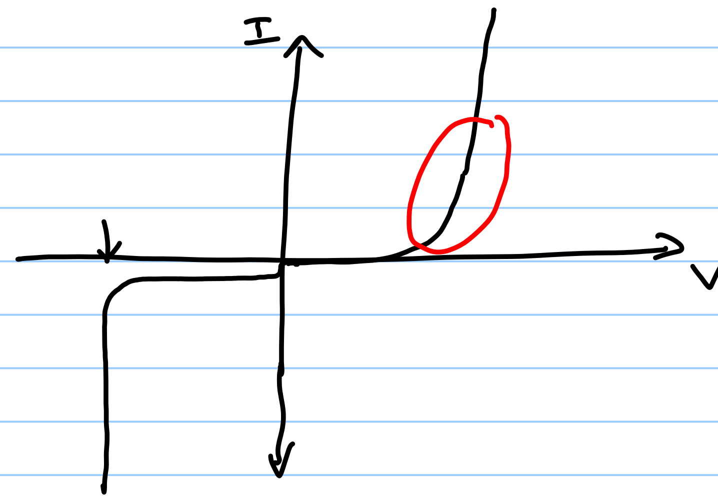


SUBSTRATE LEAKAGE:





$I \propto e^{\frac{qV}{nKT}}$

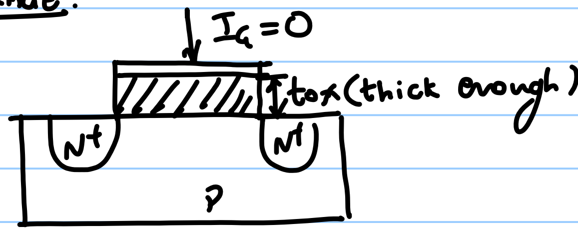


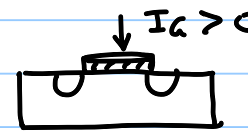
$V_{SB} \downarrow$

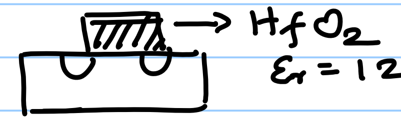
$\Rightarrow V_{TH} \downarrow$

BEWARE OF FORWARD BIASED PN JUNCTIONS:

GATE LEAKAGE:





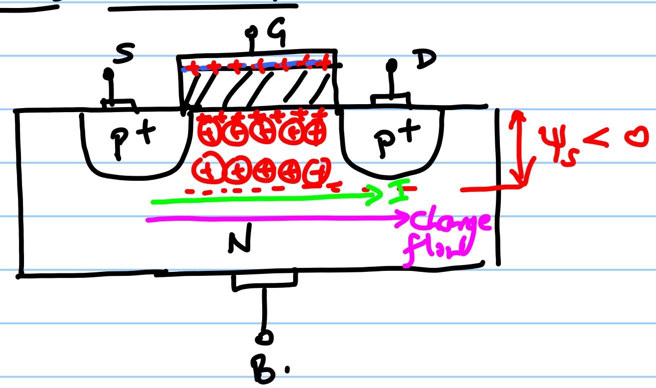


$\uparrow \underline{\varepsilon_0 A}$ $\rightarrow$ Hi K DIELECTRICS FROM 45nm node

$t_{ox} \rightarrow \uparrow$

In 14 nm node $t_{ox} \sim 1nm$

PMOS TRANSISTOR



1) $V_{GS} > 0 \rightarrow$ ACCUMUL

2) $V_{GS} < 0 \rightarrow$ DEPLETION

3) $V_{GS} < V_{TH} \rightarrow$ INVERSION

For current flow: $V_{SD} > 0$ OR $V_{DS} < 0$ $\quad (V_{GS} < 0)$

$$I_{DS} = k_p' \frac{W}{L} V_{DS}\left[(V_{GS} - V_{Tp}) - \frac{V_{DS}}{2}\right] \quad \text{Linear}$$

$$k_p' \frac{W}{L} (V_{GS} - V_{Tp})^2 \quad (1 + \lambda_p V_{DS}) \quad V_{DSATp}.$$

$$V_{TH} = V_{T0p} + \gamma_p \left(\sqrt{|2\psi_s + V_{SB}|} - \sqrt{|2\psi_s|}\right)$$

$$\underline{I_{DS}} = \begin{cases} K_p' \dfrac{W}{L} V_{max}\left[(V_{GS}-V_{Tp}) - \dfrac{V_{max}}{2}\right](1+\lambda_p V_{DS}) & V_{GS} < V_{Tp} \\ 0 & V_{GS} > V_{Tp}. \end{cases}$$

$\lambda_p \rightarrow -ve$, $V_{DS} \rightarrow -ve$

$$V_{max} = max(V_{GS}-V_{Tp}, V_{DS}, V_{DSATp})$$

$max(-1, -1.2, -1.5)$

$$V_{TH} = V_{TOp} + \gamma_p\left(\sqrt{|V_{SB}+\Psi_s|} - \sqrt{|\Psi_s|}\right)$$

$$-0.3 + \gamma_p\left(\underbrace{\sqrt{|V_{SB}+\Psi_s|} - \sqrt{|\Psi_s|}}\right) \rightarrow +ve$$

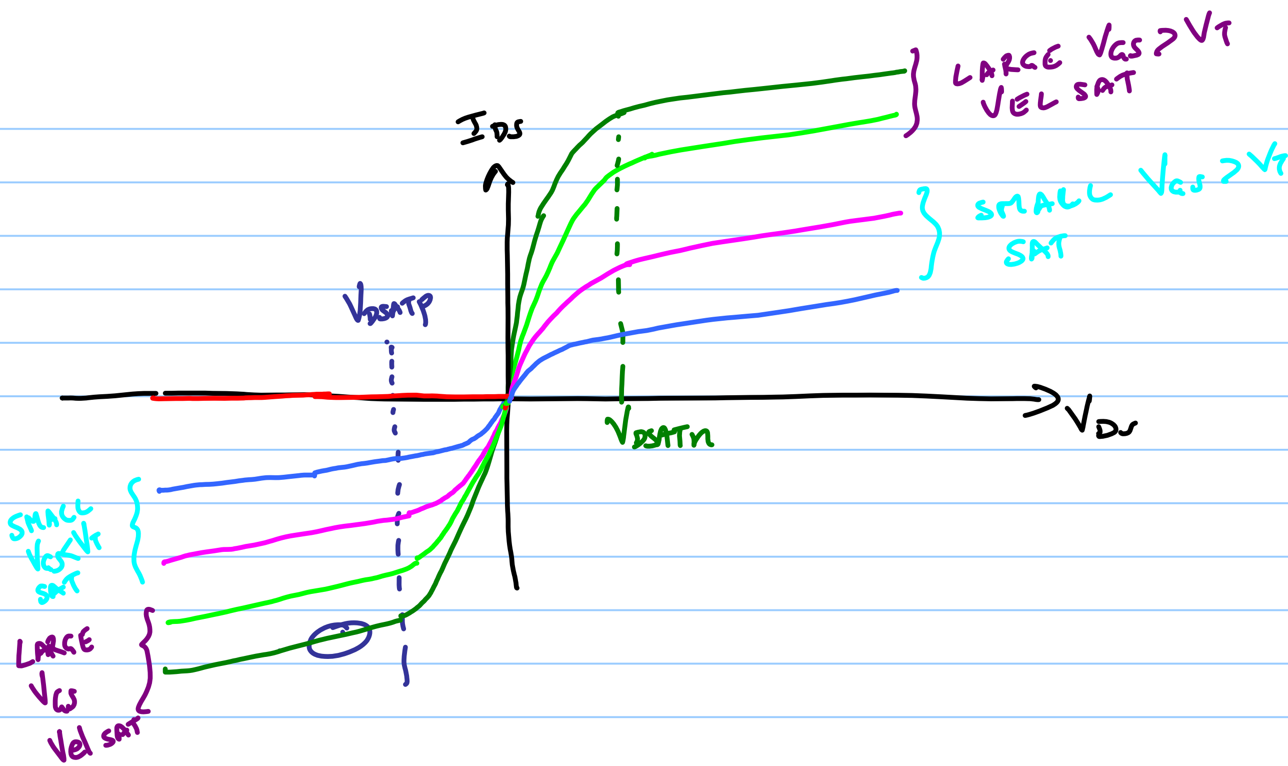
if $V_{SB} \uparrow$

$\Rightarrow |V_{TH}|$? $\downarrow$

	k'	V_{DSAT}	λ	V_{TO}	γ
NMOS	+ve	+ve	+ve	+ve	+ve
PMOS	-ve	-ve	-ve	-ve	-ve

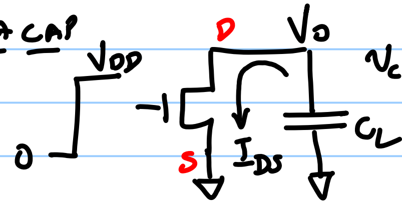
$$V_{TH} = V_{TO} + \gamma_p\left(\sqrt{|-0.25+V_{SB}|} - \sqrt{|-0.25|}\right)$$

$$= V_{TO} + \gamma_p\left(\underbrace{\sqrt{0.25-V_{SB}} - 0.5}\right) \rightarrow -ve \Rightarrow \gamma_p < 0$$

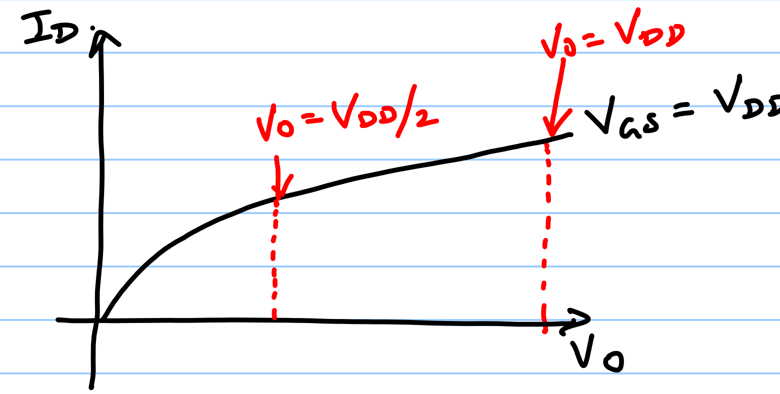


I_{DS}
V_{DS}
LARGE $V_{GS} > V_T$
VEL SAT
SMALL $V_{GS} > V_T$
SAT
V_{DSATP}
V_{DSATN}
SMALL
$V_{GS} < V_T$
SAT
LARGE
V_{GS}
Vel SAT

DISCHARGE OF A CAP



$V_c(0^-) = V_{DD}.$

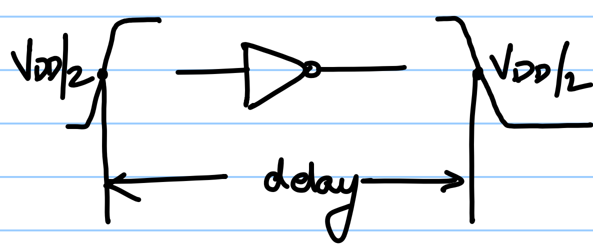


$\tau = RC_L$

$\downarrow$

R of NMOS TRANSISTOR

ASSUME: $\frac{V_{DD}}{2} > V_{DSATn}$



$$I_D = k_n' \frac{W}{L} V_{DSAT}\left((V_{DD} - V_T) - \frac{V_{DSAT}}{2}\right) \times (1 + \lambda V_O)$$

$$R_{eq}(V_O) = V_O / I_{DS}.$$

$$R_{eq} = \frac{1}{(-V_{DD}+V_{DD}/2)} \int_{V_{DD}}^{V_{DD}/2} R(V_o)\, dV_o \; = \frac{1}{(-V_{DD}/2)} \int_{V_{DD}}^{V_{DD}/2} \frac{V_o}{I_o(1+\lambda V_o)}\, dV_o$$

$$\sim (1-\lambda V_o)$$

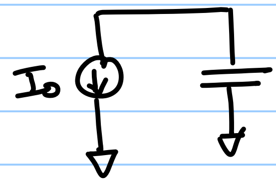
$$= \frac{1}{(-V_{DD}/2)} \int_{V_{DD}}^{V_{DD}/2} \frac{V_o}{I_o}(1-\lambda V_o)\, dV_o$$

$$= \frac{1}{(V_{DD}/2)} \left[\frac{1}{I_o} \frac{V_o^2}{2} \Big|_{V_{DD}/2}^{V_{DD}} - \frac{\lambda}{I_o} \left(\frac{V_o^3}{3} \Big|_{V_{DD}/2}^{V_{DD}} \right) \right]$$

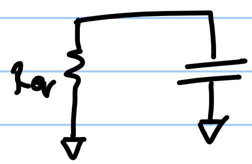
$$= \frac{3}{4} \frac{V_{DD}}{I_o} - \frac{\lambda}{I_o} \frac{7}{12} V_{DD}^2$$

$$R_{eq} = \frac{3}{4} \frac{V_{DD}}{I_o}$$

I MODEL



$$\tau\,(V_{DD} \rightarrow V_{DD}/2) = \frac{C\,\Delta V}{I_o} = \frac{C\cdot(V_{DD}/2)}{I_o}$$



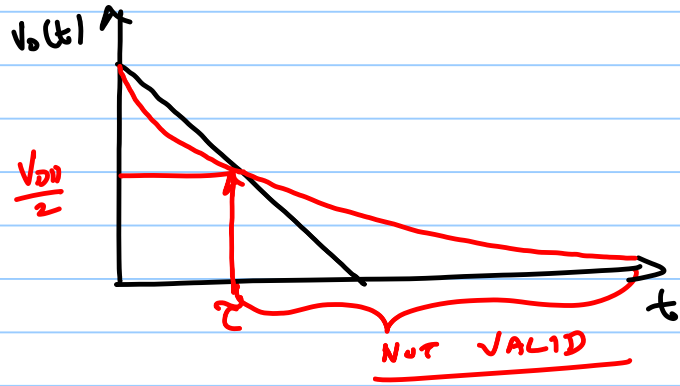
$$R_{eq} = \frac{3}{4}\,\frac{V_{DD}}{I_o}$$

$$V_o(t) = V_{DD}\,e^{-t/R_{eq}C} \Rightarrow \tau = 0.693\,R_{eq}C = \frac{3}{4}\,\frac{V_{DD}\cdot C}{I_o}$$

$$= \underbrace{0.693\times\frac{3}{4}}_{\sim 0.5}\,\frac{V_{DD}C}{I_o}$$

$$V_o(t) = V_{DD} - \frac{I_o t}{C}$$

$$\frac{C(V_{DD}/2)}{I_o}.$$


$V_o(t)$
$\frac{V_{DD}}{2}$
τ
t
NOT VALID