EES311

MODULE-5 - SEQUENTIAL CIRCUITS
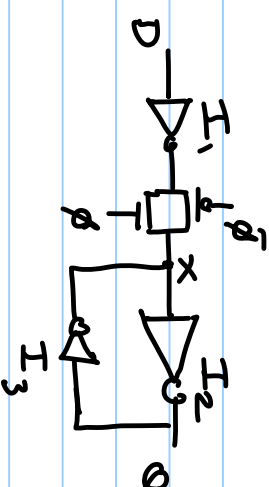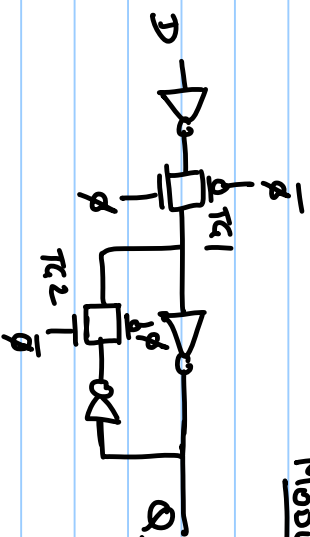
BREAKING THE FEEDBACK PATH

OVER POWERING FEEDBACK

* Transistor size don't matter for functionality.

* Tran sizes matter
  $I_1 >> I_3$.

ASSUMPTIONS: CLOCK → * IDEAL EDGES (RISE/FALL TIME = 0)

* CLK (ϕ) & $\overline{CLK}$ $(\overline{\phi})$ HAVE NO SKEW
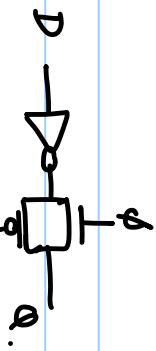
IF CLK & $\overline{CLK}$ HAVE OVERLAP / DELAY

CLK

$\overline{CLK}$

CLK

$\overline{CLK}$

D | D1 | D2 | D3 | D4 | D5

Q

L1:T L2:0   L1:0 L2:T

$\hookrightarrow$ 1-1 OVERLAP? (NON-SAMPLING EDGE)

$\rightarrow$ INVALID U&G CASE
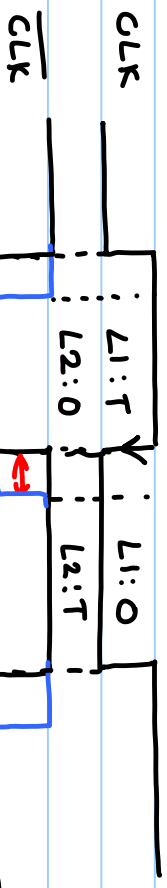
$\rightarrow$ t_{OV-1-1} < $t_{I_1} + t_{W_1} + t_{I_2}$ + t_{I_4}

t_{OV-0-0} $\rightarrow$ NO PROBLEM

$\hookrightarrow$ t_{HOLD} > t_{OV-0-0}

D —▷I₁o— [N1] ⊗ [N2] ◁I₃ — Qm — I₄ —▷o [N3]X [N4] ◁I₆ — Q

CLK $\overline{CLK}$ CLK $\overline{CLK}$

clk / clk̄   clk / clk̄

$\rightarrow$ RACE CONDITION
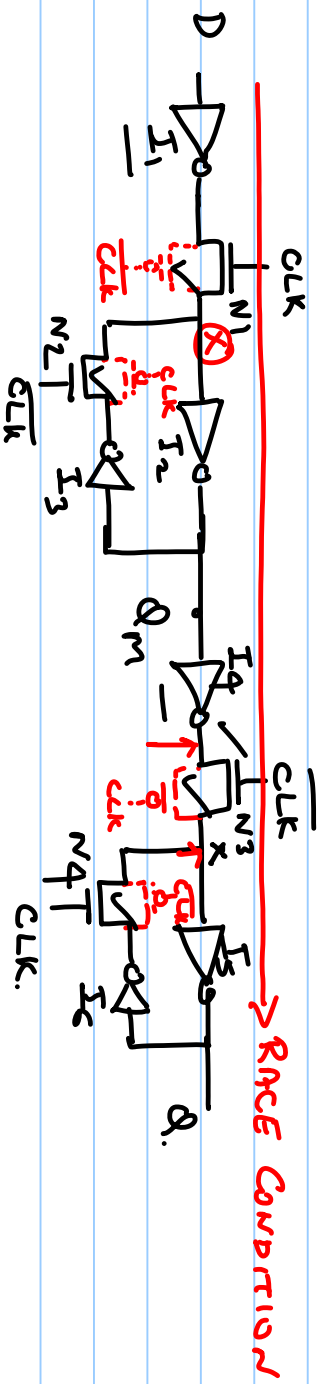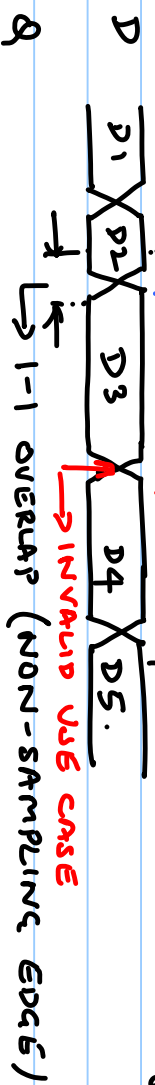
(L1: +ve   L2: -ve) $\rightarrow$ -ve edge F-LOP

REPLACE WITH TRISTATE INV
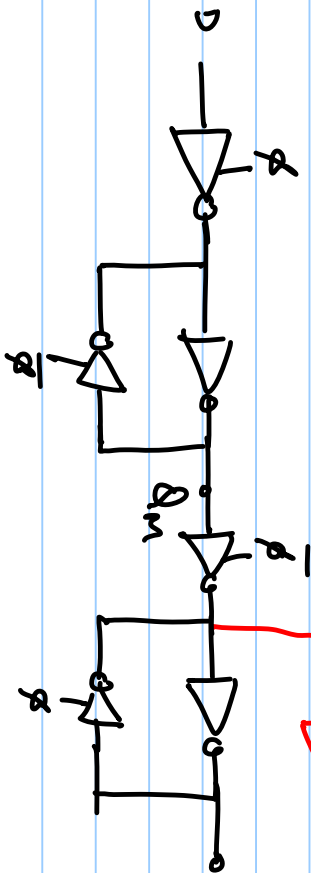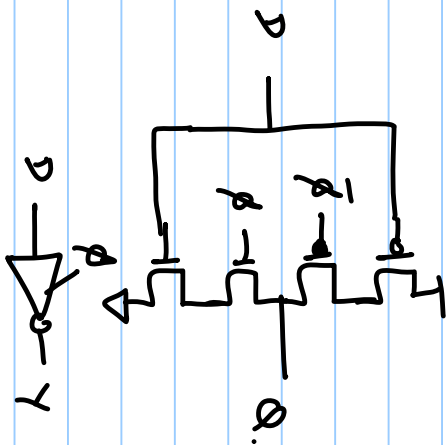
D

Q

Y

ϕ

$\phi1$

Qm

$\bar{\phi}$

D

CLK

$\overline{CLK}$

CLK

Q_M

CLK

weak

0

0

P: 0→1

D: 1→0

OVER POWER F/B.

→ BREAKING F/B.

STATIC LATCH

D

$\bar{Q}$

Q

$\bar{Q}$

DYNAMIC LATCH

D

$\bar{Q}$

Q

$$V_c(0') = 0$$

$$C_X = V(0)$$

$$V_X(0')$$

$2C$

$1:T$

$0:T$

$0.2V$

D

N1   P1   P2

ϕ

Q_M

$\bar{\phi}$

N3   P3   P4

$\bar{X}$

Q

L1 −ve

L2 +ve

+ve EDGE FLOP (DYNAMIC)

$\bar{\phi}$ ϕ

ϕ $\bar{\phi}$

Q_M

D

$\bar{\phi}$

ϕ

$t=1$ $t=0$

CMOS FLOP/LATCH

D

$\bar{\phi}$ $\bar{\phi}$ P2   N1   N2 Q_M ϕ P4   N3   N4   Q

L1
-ve

L2
+ve
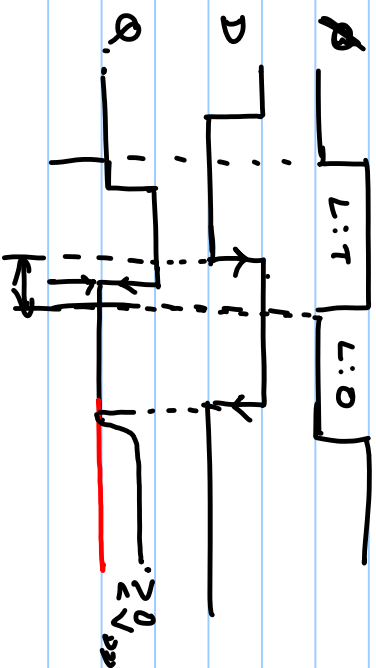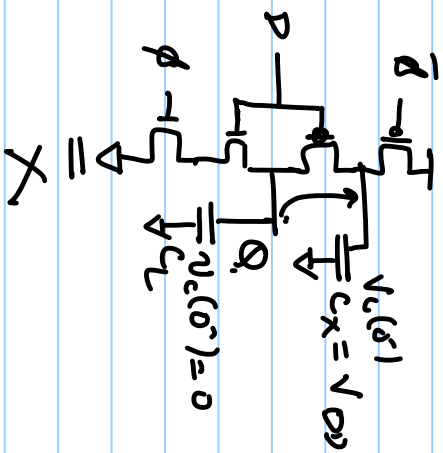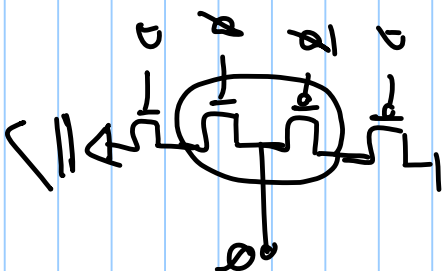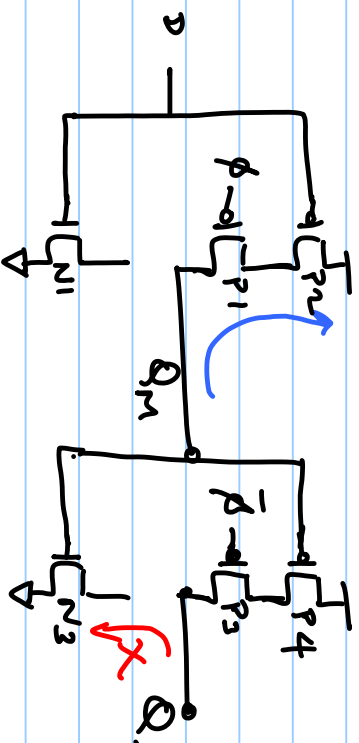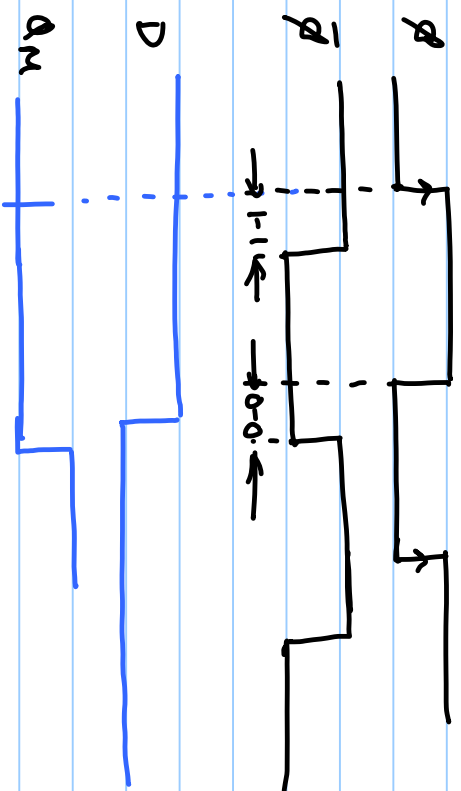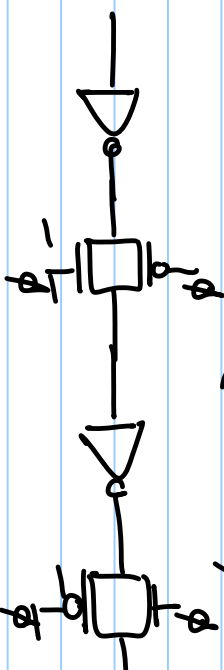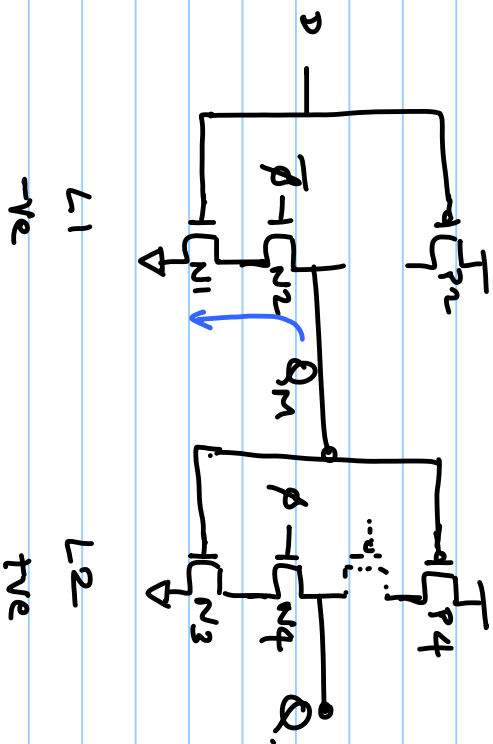
$t_{HOLD} > t_{ov-1-1}$

$t_{SETUP} = t_{TRI-STATE-L1}$

$t_{CQ} = t_{TRI-STATE-L2}$

ϕ

$\bar{\phi}$

D

Q_M

Q

L1:1
L2:0

L1:0
L2:1
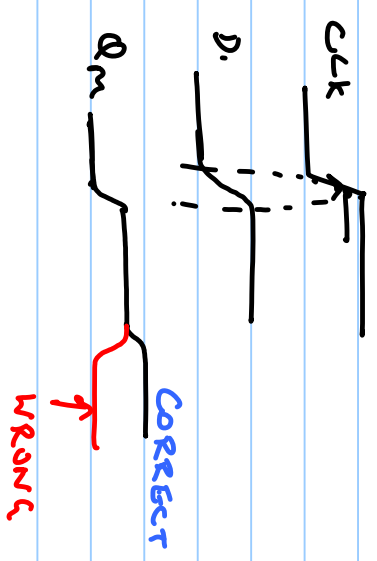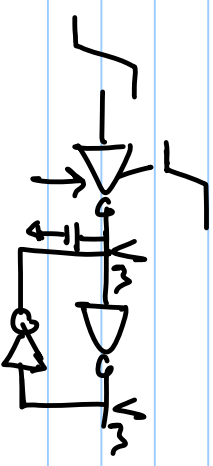
L1:1
L2:0
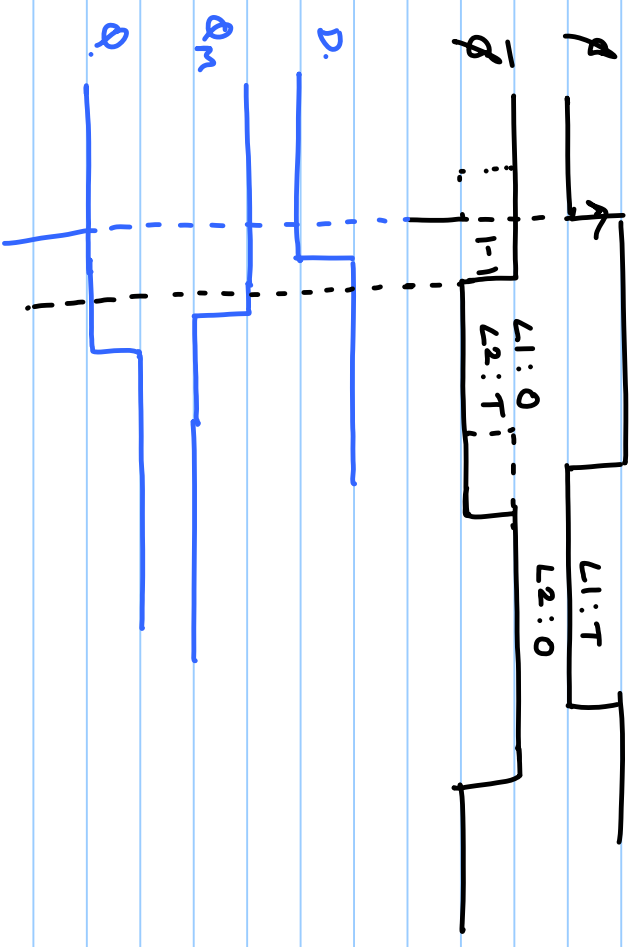
* CLOCK EDGES ARE NOT INSTANTANEOUS.

$t_{DQ} = t_{DC} + t_{CQ}$

t_{DQ}
t_{CQ}.

$t_{DQ} = t_{DC} + t_{CQ}$