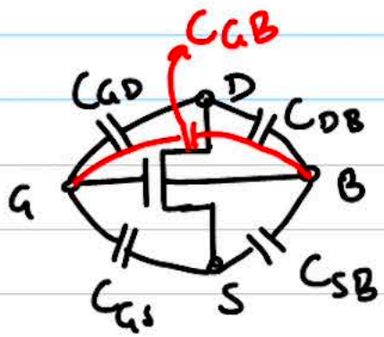
19/08/2019

EE531

MODULE - 1: THE TRANSISTOR

CAPACITANCE:



C_G (Total Gate Cap) $= C_0 + 2C_{ox} \cdot L_{ov} W$

$C_0 = \frac{\varepsilon_{ox} WL}{t_{ox}}$

$= C_0 + 2C_{ov} \cdot W$

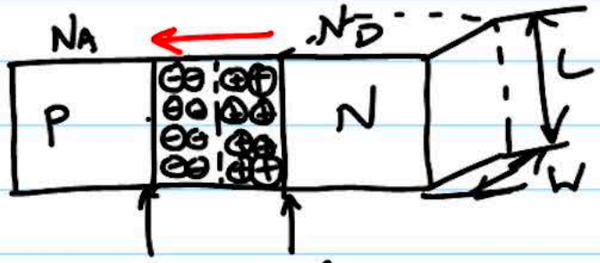
$= C_{ox} \cdot WL + 2C_{ov} W$

($fF/\mu m^2$ $\quad$ $fF/\mu m$)

$= (C_{ox} \cdot L + 2C_{ov}) W$

if $W \uparrow \Rightarrow C_G$ also $\uparrow$

DIFFUSION CAP

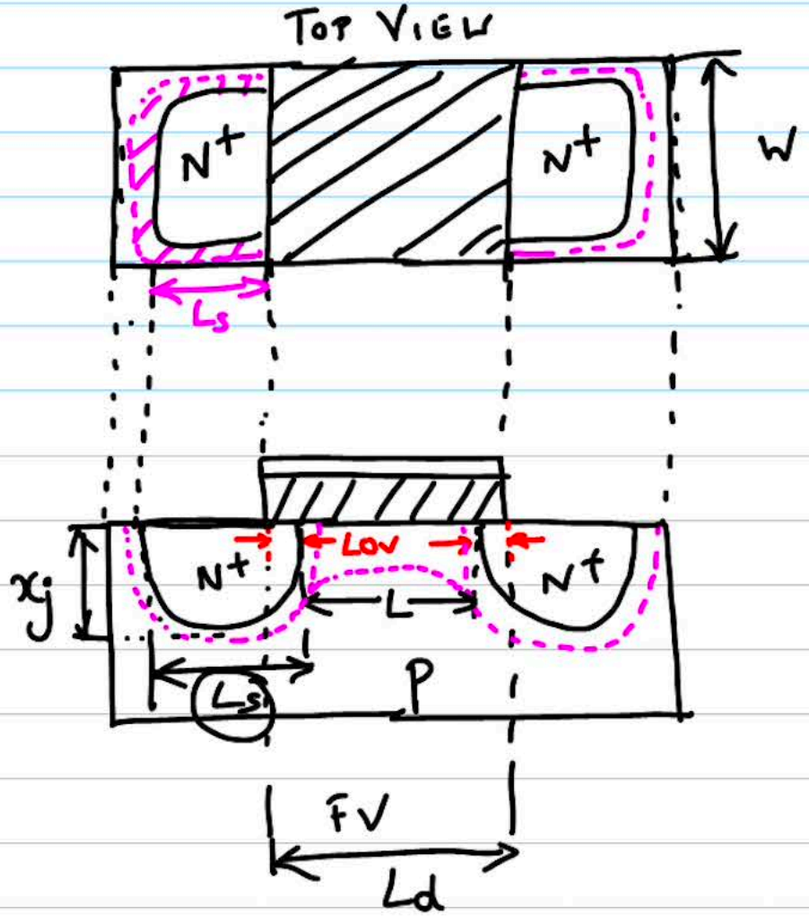


$$\phi_0 = \frac{KT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \leftarrow$$

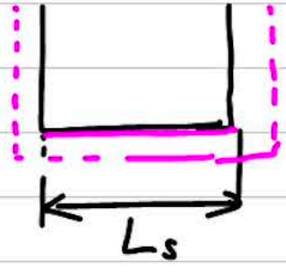
$$p = N_A \quad \frac{n_i^2}{N_D}$$

$$\text{Cap per unit area} = C_{j0} = \sqrt{\left(\frac{\varepsilon_{Si} q}{2}\right)\left(\frac{N_A N_D}{N_A + N_D}\right)\frac{1}{\phi_0}}$$

$$C_{pN} = C_{j0} \cdot WL$$



$C_j \rightarrow$ CAP per unit area.



BOTTOM PLATE CAP.

$C_{BOT} = C_j W L_s.$

SIDE WALL CAP

$C_{SW} = C_j x_j (W + 2L_s)$

$= C_{jSW} (W + 2L_s)$

$C_{SB} = C_{DB} = C_{BOT} + C_{SW} = C_j W L_s + C_{jSW} (W + 2L_s)$

$$C_{SB} = C_{DB} = C_j W L_s + C_{jsw}(W + 2L_s) = W\left(C_j L_s + C_{jsw}\left(1 + \frac{2L_s}{W}\right)\right).$$

C_j : $fF/\mu m^2$

C_{jsw} : $fF/\mu m$