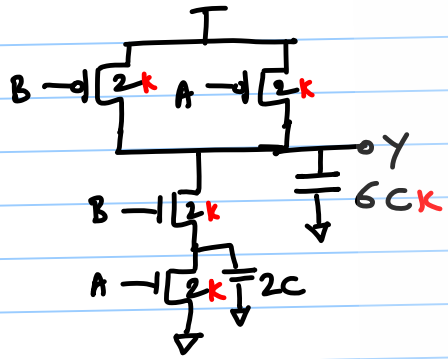
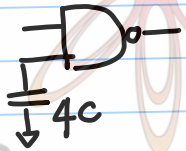
26/09/2019

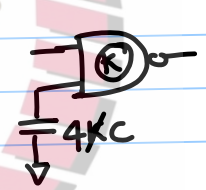
EG5311

MODULE - 4 : COMBINATIONAL CIRCUITS

PARASITIC DELAY



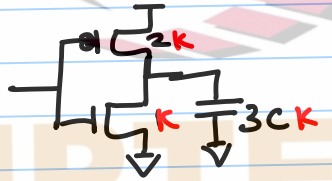




R/K

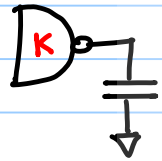
R/K.

Delay 7RC/6RC



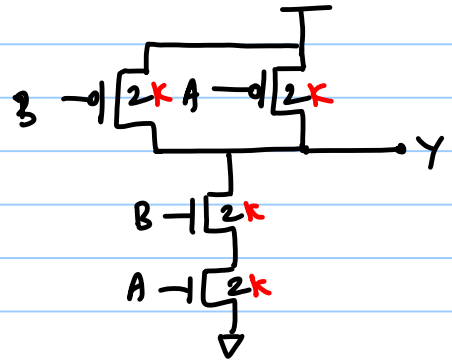
$$p = \frac{6CK}{3CK} = 2$$

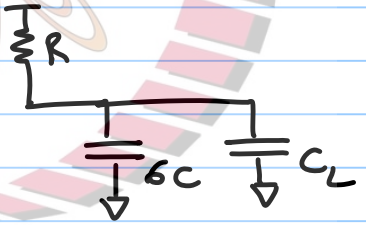
DRWING A LOAD CAPACITANCE



→ NOT A FN OF "NAND2'S" DRIVE STRENGTH

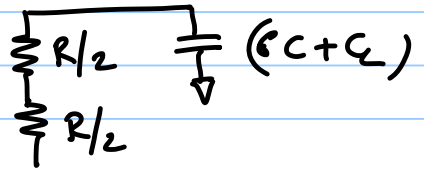
RISE PROP DELAY :

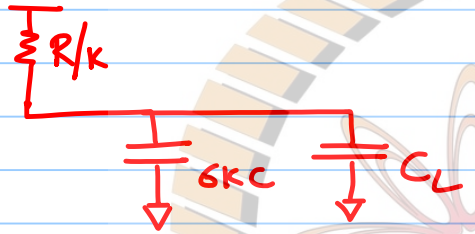




Rise delay = $R \cdot (6C + C_L)$

Fall delay = $R(6C + C_L)$





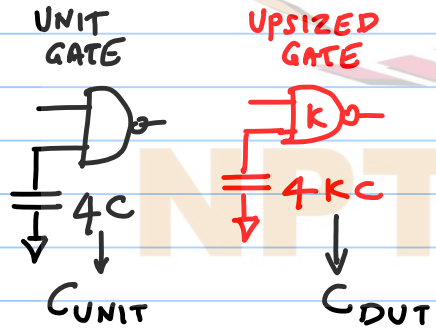
Rise delay $= \frac{R}{K}(6KC + C_L)$

$= \underbrace{6RC}_{\text{Parasitic delay.}} + \underbrace{\frac{R \cdot C_L}{K}}_{\text{Load delay term}}$

Fall delay $= \frac{R}{K}(6KC + C_L)$

$= \underbrace{6RC}_{\text{Parasitic delay.}} + \underbrace{\frac{R}{K} C_L}_{\text{Load delay term}}$

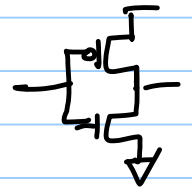
$\frac{R}{K} \cdot C_L$



$K = \frac{C_{DUT}}{C_{UNIT}}$

$$\frac{R}{K} \cdot C_L = \frac{R \times C_L \cdot (C_{UNIT})}{(C_{DUT})} = R \cdot \left(\frac{C_L}{C_{DUT}}\right) \cdot C_{UNIT}.$$

$$\text{delay} = R\left(\frac{C_L}{C_{DUT}}\right) \cdot C_{UNIT} + nRC$$



Normalised delay : delay ÷ delay of a Ref unit $inv = 3RC$

$$\hat{d} = \left(R \cdot \left(\frac{C_L}{C_{DUT}}\right) \cdot C_{UNIT} + nRC\right) / 3RC.$$

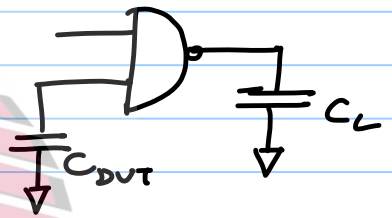
$$= \underbrace{\left(\frac{C_L}{C_{DUT}}\right) \cdot \left(\frac{C_{UNIT}}{3C}\right)} + \left(\frac{n}{3}\right)$$

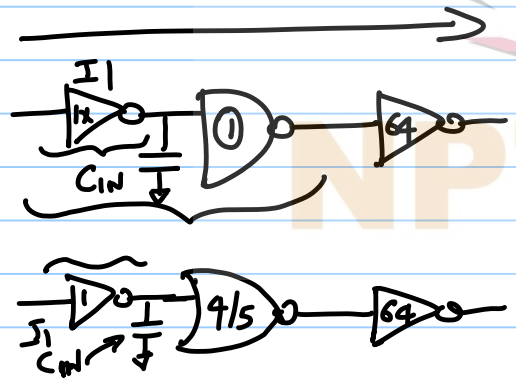
$$\left(\frac{C_L}{C_{DUT}}\right)\cdot\left(\frac{C_{UNIT}}{3C}\right)$$

ELECTRICAL EFFORT

LOGICAL EFFORT

} PURELY A FN OF THE LOGIC TOPOLOGY



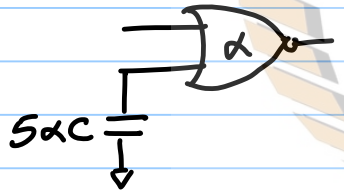


PATH delay = $d_{I_1} + d_{DUT}$ (d_{NAND} OR d_{NOR})

delay of I_1 should be same

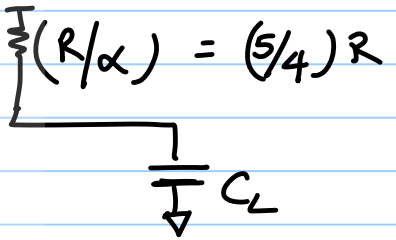
$(C_L >> C_{PAR})$

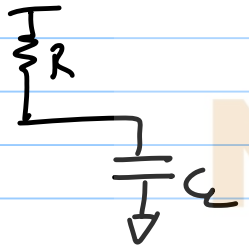
$d_{dut} = RC_L$



$\Rightarrow 5\alpha C = 4C$

$\therefore \boxed{\alpha = \frac{4}{5}}$



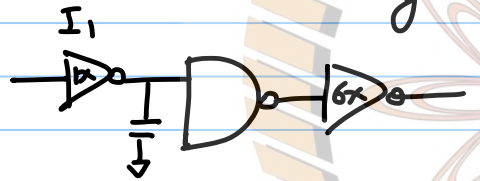


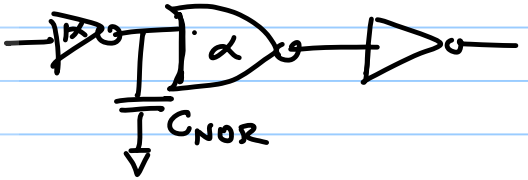
$d_{DUT} = \frac{5}{4} R \cdot C_L$

$$\text{delay} = \left(\frac{C_L}{C_{DUT}}\right)\cdot\left(\frac{C_{UNIT}}{C_{INV}}\right) + p \cdot \leftarrow$$

$$\downarrow$$

$$g$$



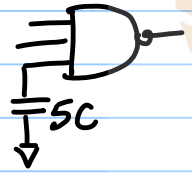


$$\underline{d_{I_1}} = \left(\frac{C_{NAND}}{C_{1X}}\right)\cdot + \qquad \underline{d_{I_1}} = \left(\frac{C_{NOR}}{C_{1X}}\right)\cdot$$

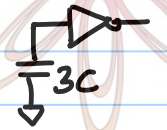
$$\underline{d_{NAND}} = \left(\frac{C_{INV\,6q}}{C_{NAND}}\right)\cdot\left(\frac{C_{UNIT}}{C_{INV}}\right) + \qquad \underline{d_{NOR}} = \left(\frac{C_{INV\,6q}}{C_{NOR}}\right)\cdot\left(\frac{C_{UNIT-NOR}}{C_{INV}}\right) + \ldots$$

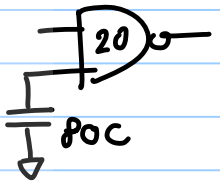
LOGICAL EFFORT = g = RATIO OF GATE CAP OF THE GATE (DUT) TO GATE CAP OF A STATIC CMOS INVERTER WITH SAME DRIVE STRENGTH.

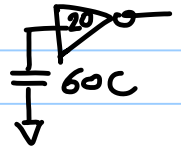
NAND3:



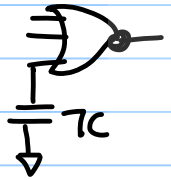
$g = \frac{5}{3}$



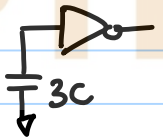


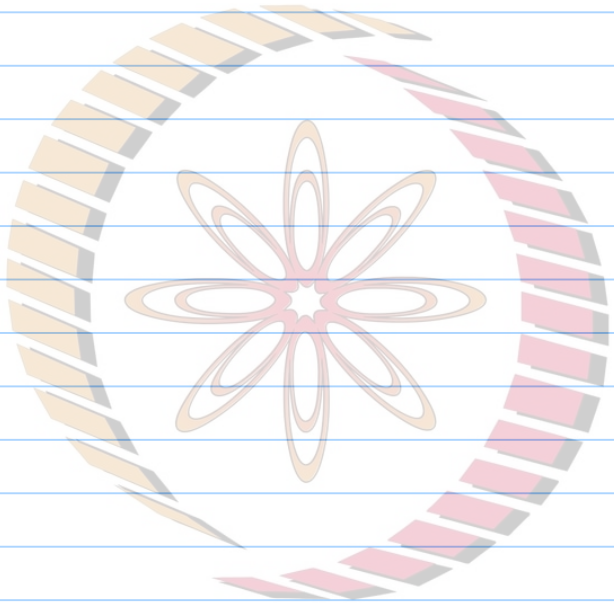


$\therefore g = \frac{4}{3}$



$g = \frac{7}{3}$




NPTEL