EES311

MODULE-5 - SEQUENTIAL CIRCUITS

LATCH → LEVEL SENSITIVE (+ve) →   IF CLK==1   Q = D;

FLOP → EDGE TRIG.   else $Q_{n+1} = Q_n$;

+ve LATCH

+ve EDGE FLOP

MASTER

D
(L1)
+ve EDGE FLOP
CLK
tpdq
Qm
(L2)
CLK
SLAVE
Q

CLK
D   D1   D2   D3   D4
Qm   D1   D2   D3   D4
Q   D2   D3   D4

L1:T L2:0   L1:0 L2:T   L1:T L2:0

tpcq-flop = tpcq-L2

tpcq-flop
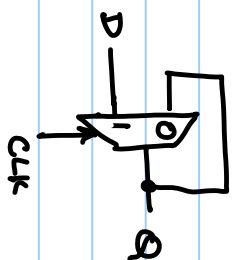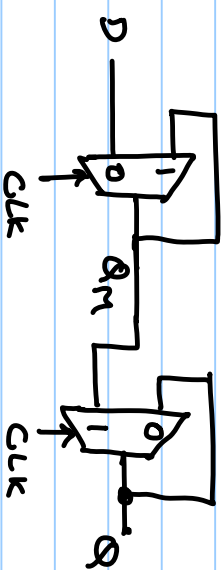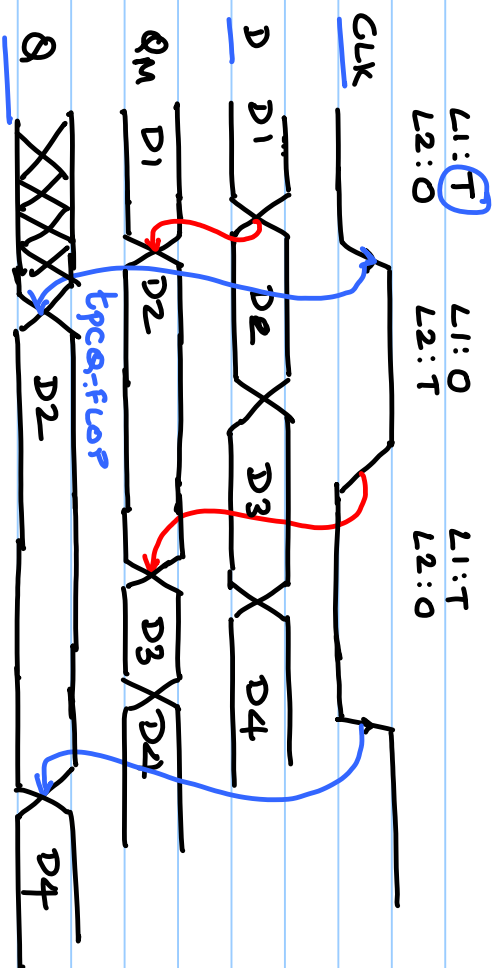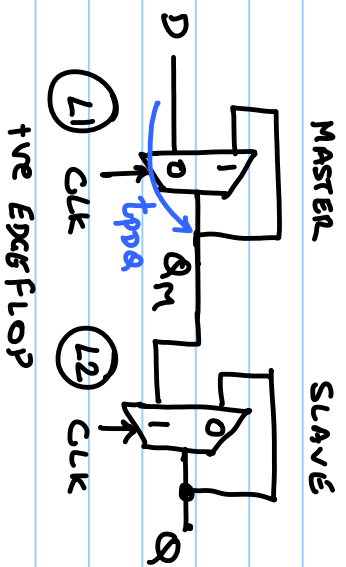
tsetup-flop = tsetup-L1

CIRCUIT IMPLEMENTATION