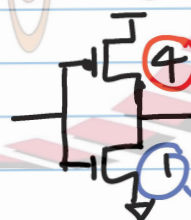EE5811

MODULE -4 : COMBINATIONAL CIRCUITS
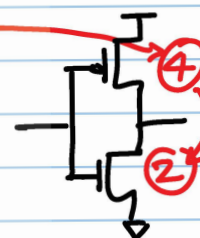
HI- SKEW INV
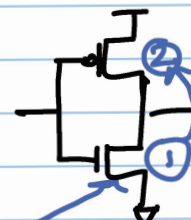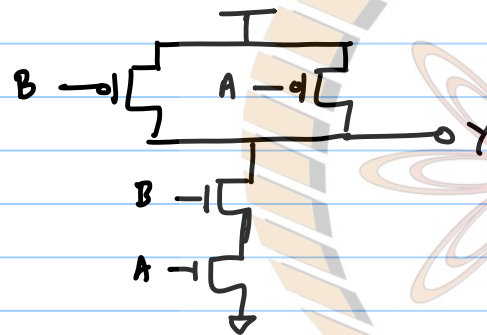

$$g_{pu} = \frac{5c}{6c}$$

$$g_{pd} = \frac{5}{3}$$

SPECIAL FUNCTIONS

$$Y_{PD} = \overline{AB}$$

$$Y_{PU} = \overline{A} + \overline{B}$$

$$Y_{PD} = Y_{PU}$$

$$Y_{PD} = \overline{f}(A_1, A_2 \dots A_N)$$

$$Y_{PU} = g(\overline{A_1}, \overline{A_2} \dots \overline{A_N})$$

$$Y_{PD} = Y_{PU}$$

IF   PMOS   STACK (PUN) WAS A   MIRROR IMAGE OF PDN
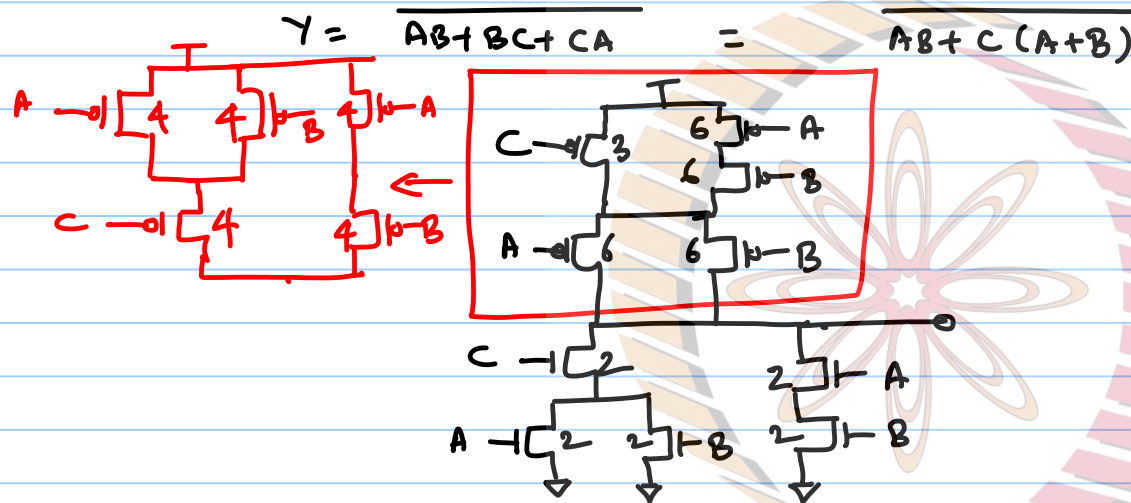
$$Y_{PU} = f(\bar{A_1}, \bar{A_2} \ldots \bar{A_N})$$

GIVEN

$$Y_{PD} = \bar{f}(A_1, A_2, \ldots A_N)$$

$$f(\bar{A_1} \bar{A_2} \ldots \bar{A_N}) = \bar{f}(A_1 A_2 \ldots A_N)$$

$$Y = \overline{AB + BC + CA}$$

$$Y = \overline{AB + BC + CA} = \overline{AB + C(A+B)}$$

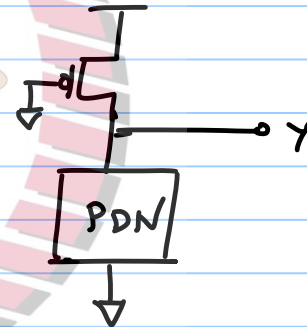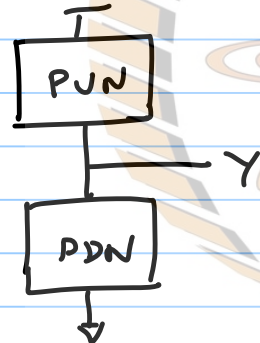| A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1.
1	1	0	1
1	1	1	1

$$Y = \sum m(0,1,2,4)$$

$$\overline{Y} = \sum m(3,5,6,7)$$

$$Y = A \oplus B \oplus C$$

PMOS CAN KILL YOUR LOGICAL EFFORT

RATIO'D CIRCUITS (PSEUDO NMOS LOGIC)

STATIC CMOS

$V_{OL} > 0$

$Y = V_{OL}$

$A = V_{DD}$

	V_{GS}	V_{DS}	REGION
NMOS	V_{DD}	V_{OL}	LIN
PMOS	$-V_{DD}$	$V_{OL}-V_{DD}$	VEL SAT

$$I_{DSn} = K_n' \frac{W_n}{L} \cdot V_{OL} \left[\overbrace{(V_{DD} - V_{Tn}) - \frac{V_{OL}}{2}} \right] \sim (V_{DD} - V_{Tn})$$

$$I_{DSp} = K_p' \frac{W_p}{L} \cdot V_{DSATP} \left[(-V_{DD} - V_{TP}) - \frac{V_{DSATP}}{2} \right]$$
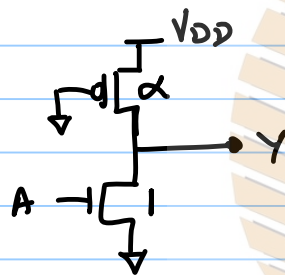
$$\therefore \quad I_{DSp} = - I_{DSn}$$

$$\Rightarrow \quad + K_p' \frac{W_p}{L} V_{DSATP} \left[(V_{DD} + V_{TP}) + \frac{V_{DSATP}}{2} \right] = + K_n' \frac{W_n}{L} \cdot V_{OL} (V_{DD} - V_{Tn})$$

$$\Rightarrow \quad V_{OL} = \frac{K_p' \cdot W_p \cdot V_{DSATP} \left[(V_{DD} + V_{TP}) + V_{DSATP}/2 \right]}{K_n' \cdot W_n (V_{DD} - V_{Tn})}$$

$$\Rightarrow \quad V_{OL} = \frac{K_p' W_p \cdot V_{DSATP}}{K_n' W_n} \quad \Rightarrow \quad (W_P / W_n) = V_{OL} \cdot \frac{K_n'}{K_p' \cdot V_{DSATP}}$$

$$\frac{W_p}{W_n} = \alpha$$