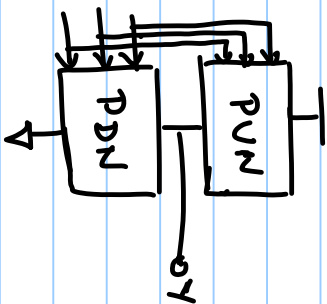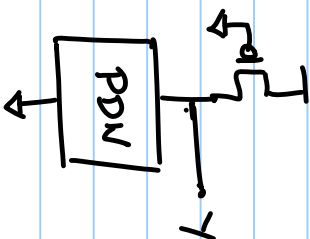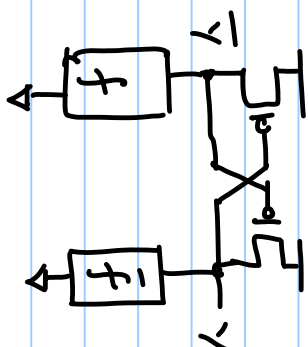# EE5311

MODULE-4 - COMBINATIONAL CIRCUITS

STATIC
CMOS

PSEUDO
NMOS

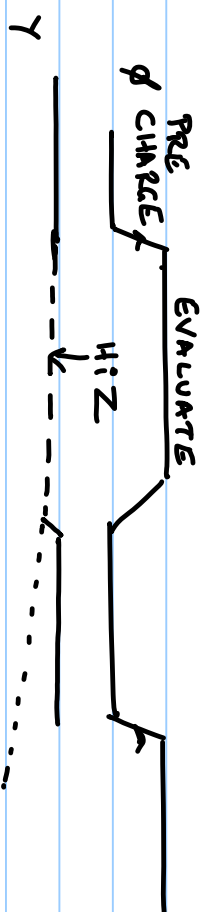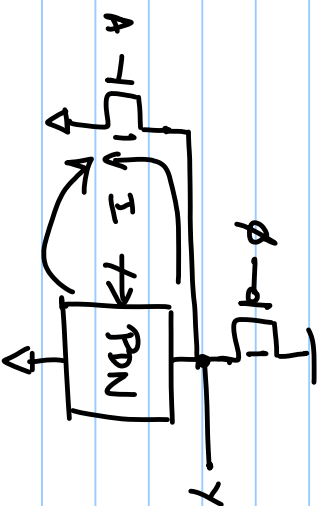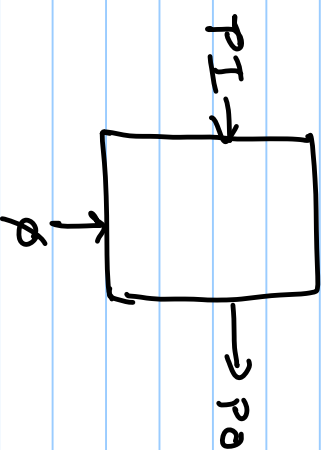$V_{OL} > 0$
$U_p | W_n \propto V_{OL}$
RATIO'ED CKT
STATIC CURRENT

CVSL
REQUIRE A & Ā
MORE AREA

DYNAMIC CIRCUITS.

A

Y

I

PDN

φ

Y

φ

PI

PO

Y

PRE
φ CHARGE

EVALUATE

HiZ

$C_R = 2C$

V_{DD}

φ —| 1 H

A —| 2

φ —| 2F → Y
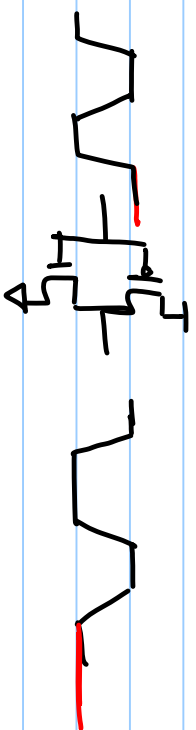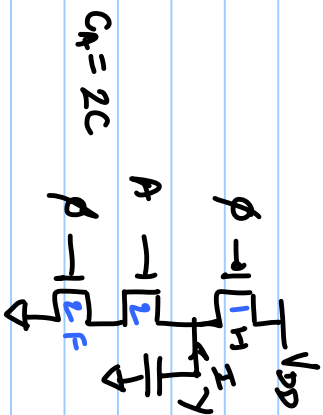
INPUT CANNOT FALL IN
EVAL PHASE

g_u —→ NOT RELEVANT HERE

$g_u = 2/3.$

P   E   Y   A

IF THERE
IS A FOOTER
DEVICE

① ②

REP INV:

$C_R' = 3C$

Y —| 2

A —| 1 → Z
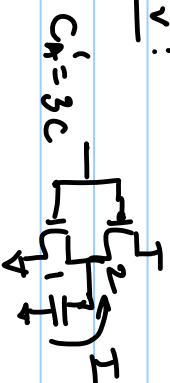
W/O FOOTER DEVICE: $g_u = 1/3.$
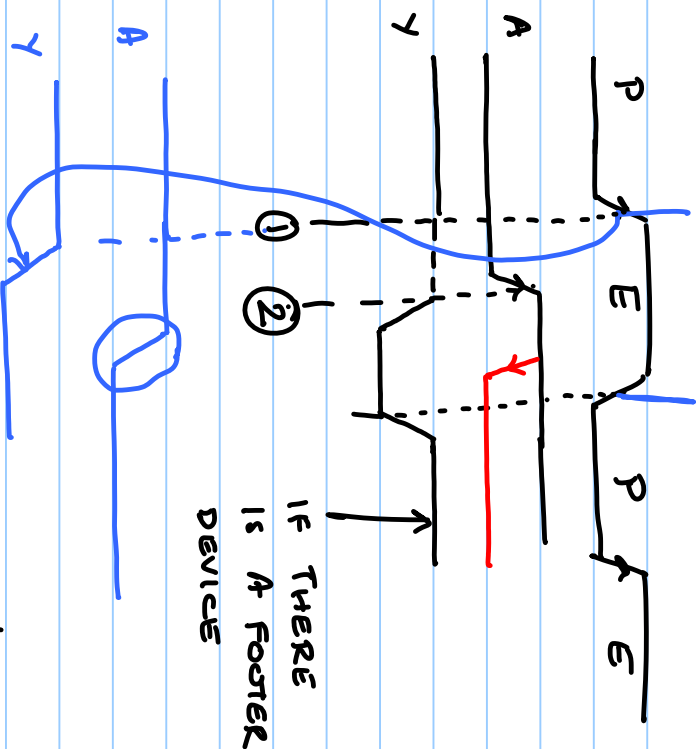
NAND2:
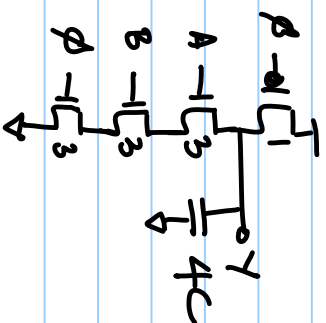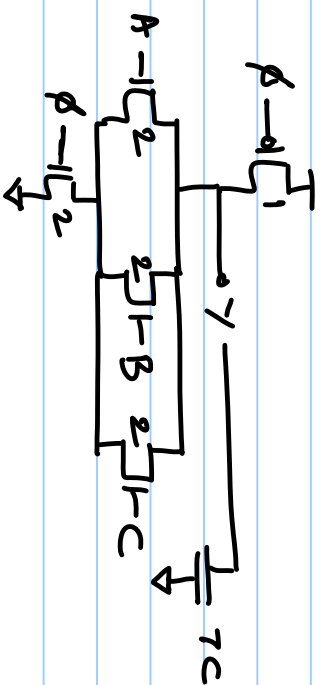
$g_A = g_B = 1$

$p = 4/3$

NOR2/3
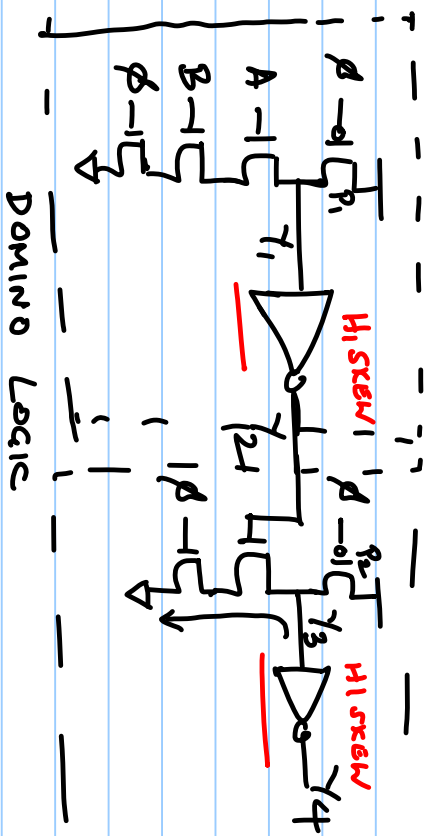
$g_A = g_B = g_C = 2/3$

$p = 7/3.$

φ

B

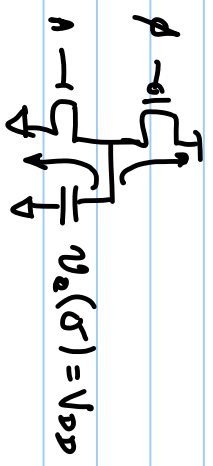A

φ

φ

B

A

φ

Y_1

φ

φ

$Y = A \cdot B$
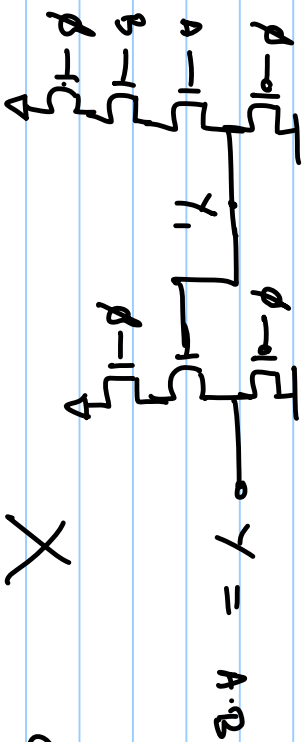
CANNOT CASCADE DYNAMIC
GATES

φ

P   E   P   E

B

A

Y_1

VIOLATING MONOTONE NON DECREASING CONDITION

DYNAMIC AND:

DOMINO LOGIC

B = 1

HI SKEW

HI SKEW

$V_o(\sigma) = V_{DD}$

EVAL $\phi = 1$

PRECHARGE: $\phi = 0$

PDN

ϕ

ϕ

X

Y_2

Y_3

PDN IS (ACTIVE
WEAK)
KEEPER DEVICE

$\phi = 1$

A
B
C

Y_3
Y_2
Y_1

Y_1

Y_2