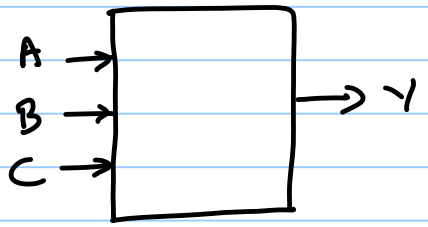
19/09/2019

EE5311

MODULE-4 : COMBINATIONAL CIRCUITS

IMPLEMENTING ANY BOOLEAN FUNCTION



A	B	C	Y
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
⋮			
1	1	1	0

Y = SUM OF PRODUCTS

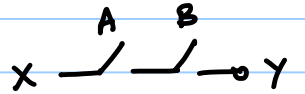
$= \sum m(0,3,7) = \bar{A}\bar{B}\bar{C} + \bar{A}BC + ABC$

$Y = m_0 + m_3 + m_7$ (SOP)

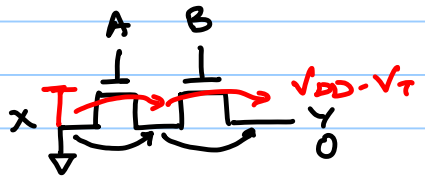
$\bar{A}\bar{B}\bar{C} + \bar{A}BC + ABC$

OR (SUM)

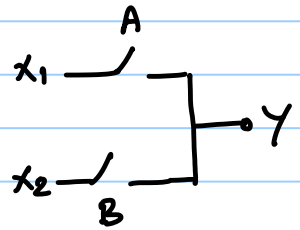
PRODUCT (AND)



$= Y = (A \cdot B)X$



$Y = (AB)X$



$= Y = AX_1 + BX_2$

NMOS TRANSISTORS → PULL DOWN LOGIC

$Y = ABC + \bar{A}\bar{B}\bar{C}$

WHEN $A=1, B=1, C=1 \Rightarrow ABC = 1 \Rightarrow Y = 1$

$\bar{A} = \bar{B} = \bar{C} = 1 \Rightarrow \bar{A}\bar{B}\bar{C} = 1 \Rightarrow Y = 1$

$\Rightarrow$ (USE NMOS)

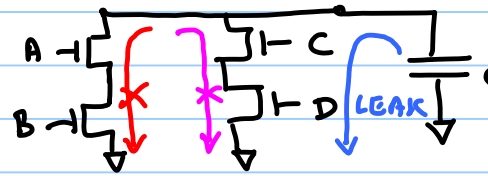
$Y = f(A,B,C)$

STEP 1: INVERT Y

$\Rightarrow \bar{Y} = \bar{f}(A,B,C)$

$Y = \overline{AB + CD}$

$\Rightarrow \bar{Y} = AB + CD$



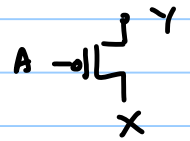
PDN
PULL DOWN NETWORK

$A=1, B=1, Y=0$
$C=1, D=1, Y=0$
$A=B=C=D=1, Y=0$
} SIMILAR CONDITIONS $Y=0$

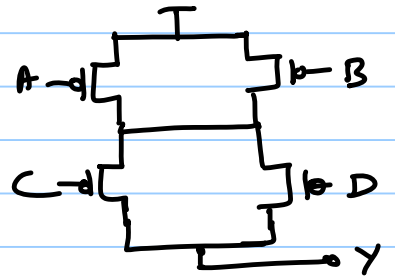
OTHE CONDITIONS ⟶ O/P IS "FLOATING" OR HiZ state (Z)

$\overline{Y} = AB+CD$

$Y = \overline{\overline{Y}} = \overline{AB+CD} = (\bar{A}+\bar{B})(\bar{C}+\bar{D})$ PUN – PULL UP N/W



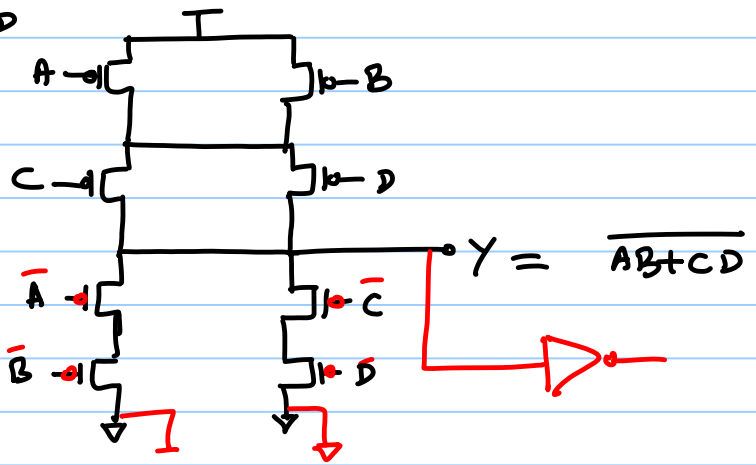
$\Rightarrow Y = \bar{A}X$



PUN

$Y = \overline{AB+CD}$

$Y = AB+CD$

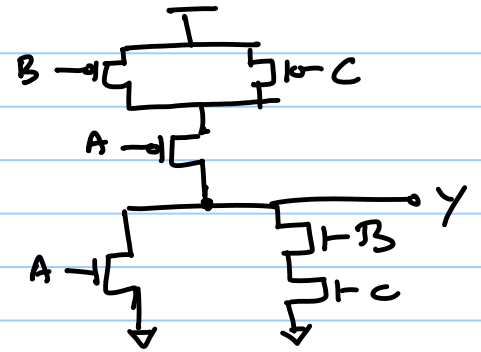


$Y = \bar{A}\cdot\bar{B} + \bar{C}\bar{D}$

$Y = \overline{A + BC}$

① INVERT $Y \Rightarrow \overline{Y} = A + BC$

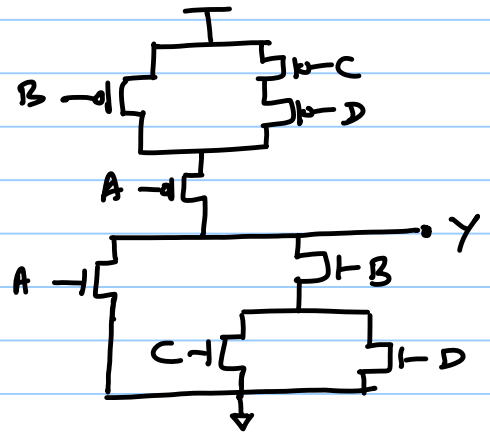
② IMPLEMENT PDN



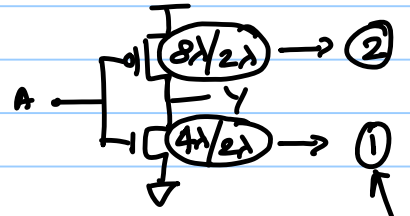
$Y_{PDN} = \overline{A + BC}$

$Y_{PUN} = \bar{A}(\bar{B} + \bar{C})$

$Y = \overline{A + B(C + D)}$

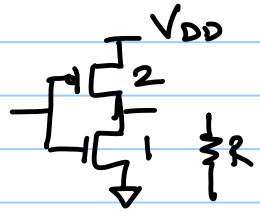


SIZING:



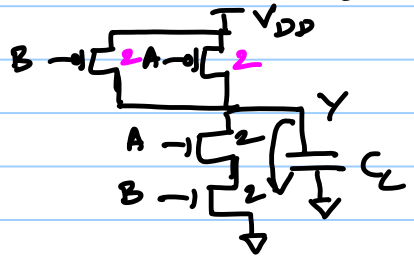
DELAY IS SYM

$W_p = 2W_n$

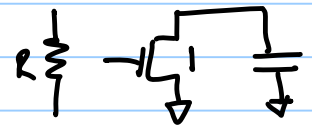


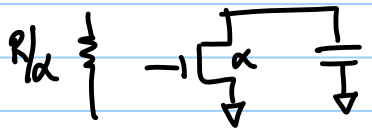
REFERENCE CMOS INVERTER

NAND 2: $Y = \overline{AB}$



WORST CASE PU/PD RESISTANCE

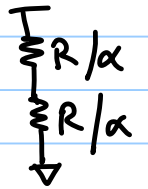




$$R = \frac{3V_{DD}}{4I_{DSAT}}$$

$$R_\alpha = \frac{3V_{DD}}{4 \cdot \alpha \cdot I_{DSAT}} = \frac{R}{\alpha}$$

PDN RESISTANCE



$$\Rightarrow \frac{2R}{\alpha} = R$$