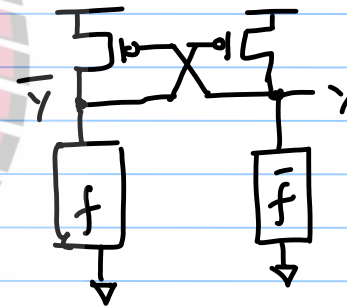# EE5311

Module-4 – Combinational Circuits
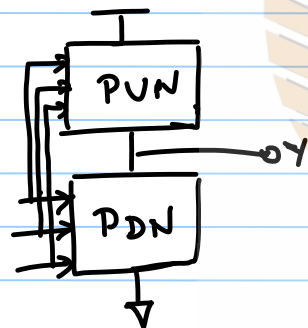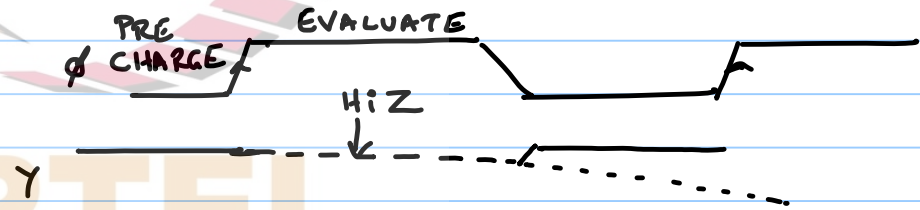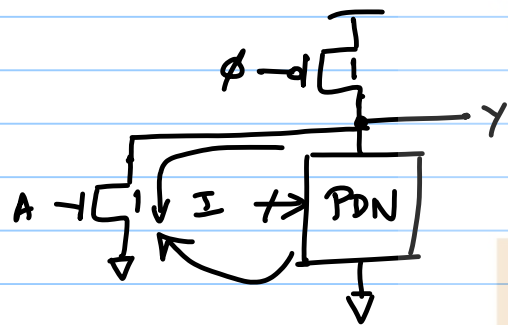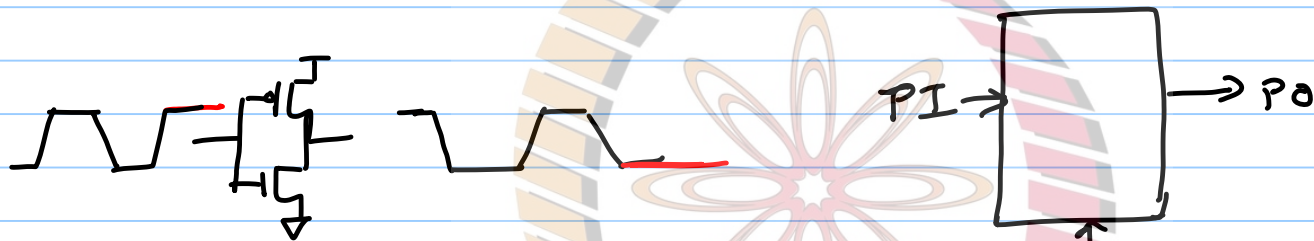

STATIC CMOS
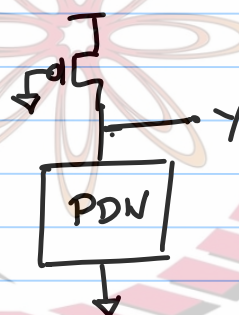
PSEUDO NMOS
$V_{OL} > 0$
$W_p|W_n \propto V_{OL}$
RATIO'ED CKT
STATIC CURRENT

CVSL
REQUIRE A & $\bar{A}$
MORE AREA

DYNAMIC CIRCUITS.

$PI \rightarrow$ | | $\rightarrow PO$

ϕ

$\phi \multimap$

Y

$A \dashv$ $I \Rightarrow$ PDN

PRE CHARGE   EVALUATE

ϕ

HiZ

Y

V_{DD}

$\phi \rightarrow \vdash 1_H$ I Y

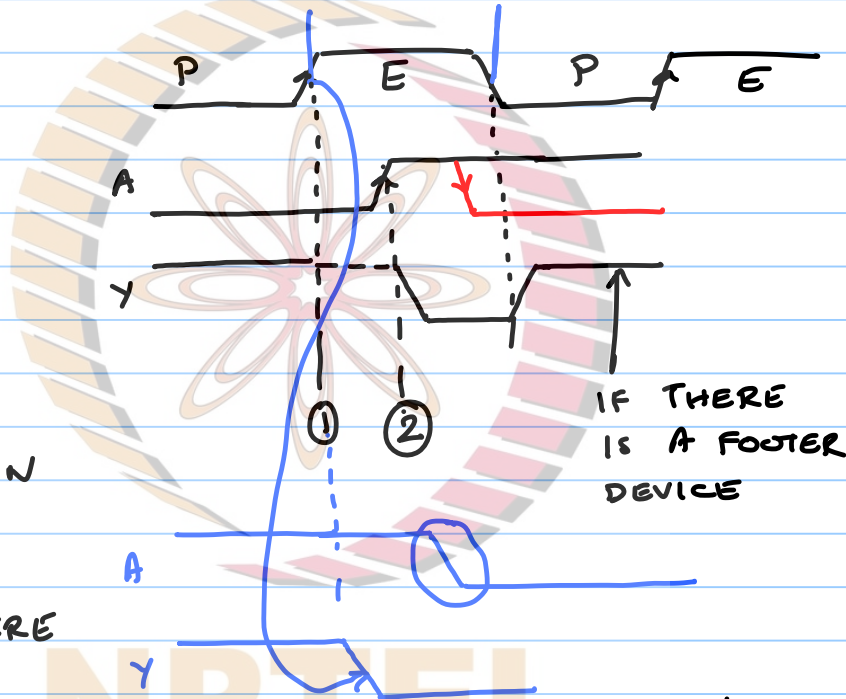$A \rightarrow \vdash 2$

$C_A = 2C$ $\phi \rightarrow \vdash 2_F$
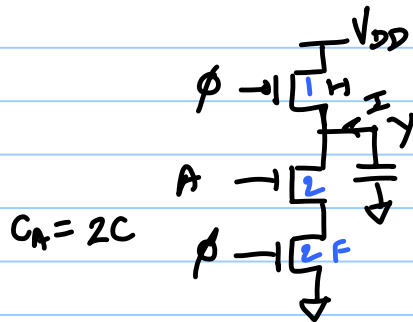
INPUT CANNOT FALL IN
EVAL PHASE

$g_u \rightarrow$ NOT RELEVANT HERE

$g_d = 2/3.$ REF INV:

P   E   P   E

A

Y

①   ②

IF THERE
IS A FOOTER
DEVICE

$C_A' = 3C$ I 2 I 1
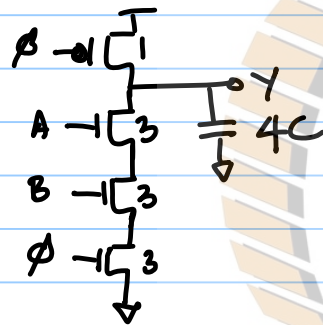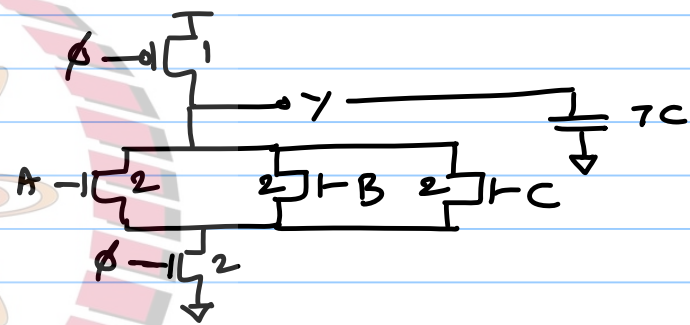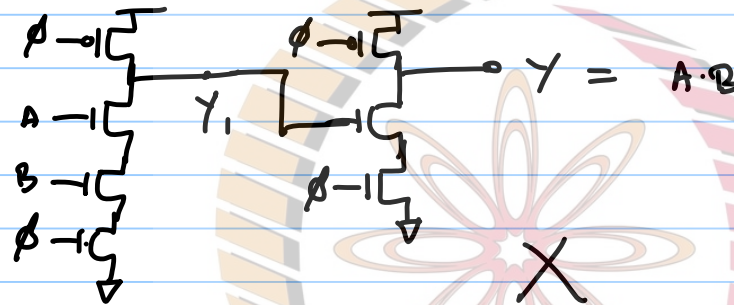
A

Y
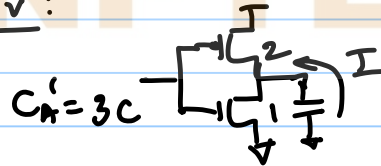
W/O FOOTER DEVICE: $g_d = 1/3.$

NAND2:

$$g_A = g_B = 1$$

$$p = 4/3$$

NOR2/3

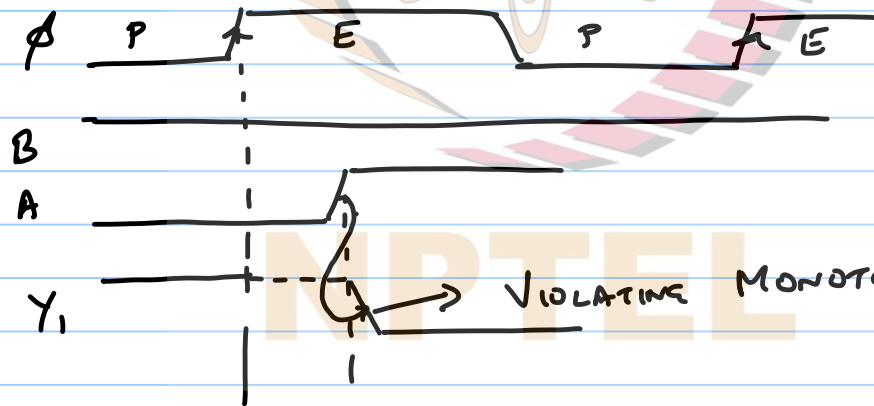

$$g_A = g_B = g_C = 2/3$$

$$p = 7/3.$$
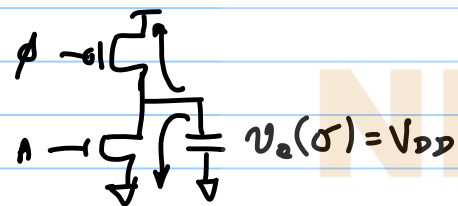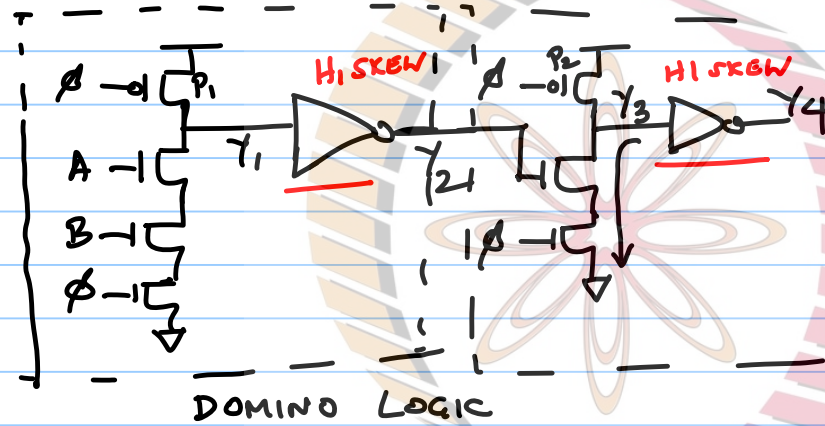
$Y = A \cdot B$

CANNOT CASCADE DYNAMIC GATES

VIOLATING MONOTONE NON DECREASING CONDITION

DYNAMIC AND:

HI SKEW   HI SKEW

ϕ —o| P_1
A —|
B —|
ϕ —|

Y_1 Y_2 ϕ —o| P_2 Y_3 Y_4

DOMINO LOGIC

ϕ —o|
A —| $v_0(0) = V_{DD}$

$B = 1$

ϕ P   E   P   E

A

Y_1

Y_2

Y_3

Y_4

EVAL $\phi = 1$

PRECHARGE: $\phi = 0$

WEAK

PDN IS   ACTIVE
KEEPER DEVICE

Y_1

Y_2

V_{IL}