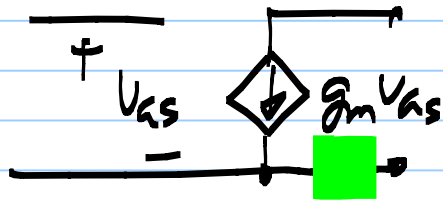
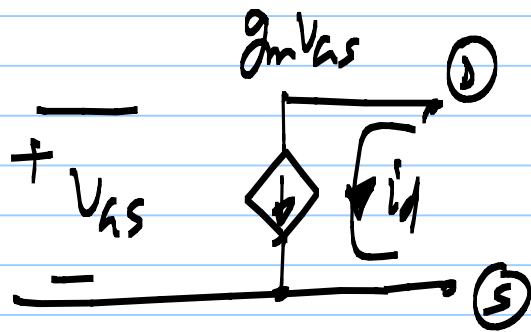


## VCCS using a MOS transistor



$g_m$ : changes with temperature

VCCS:  $i_o' = V_{in} \cdot \overbrace{G_1}^{G_m} = \frac{V_{in}}{R_1} \quad R_1 = 1/G_1$

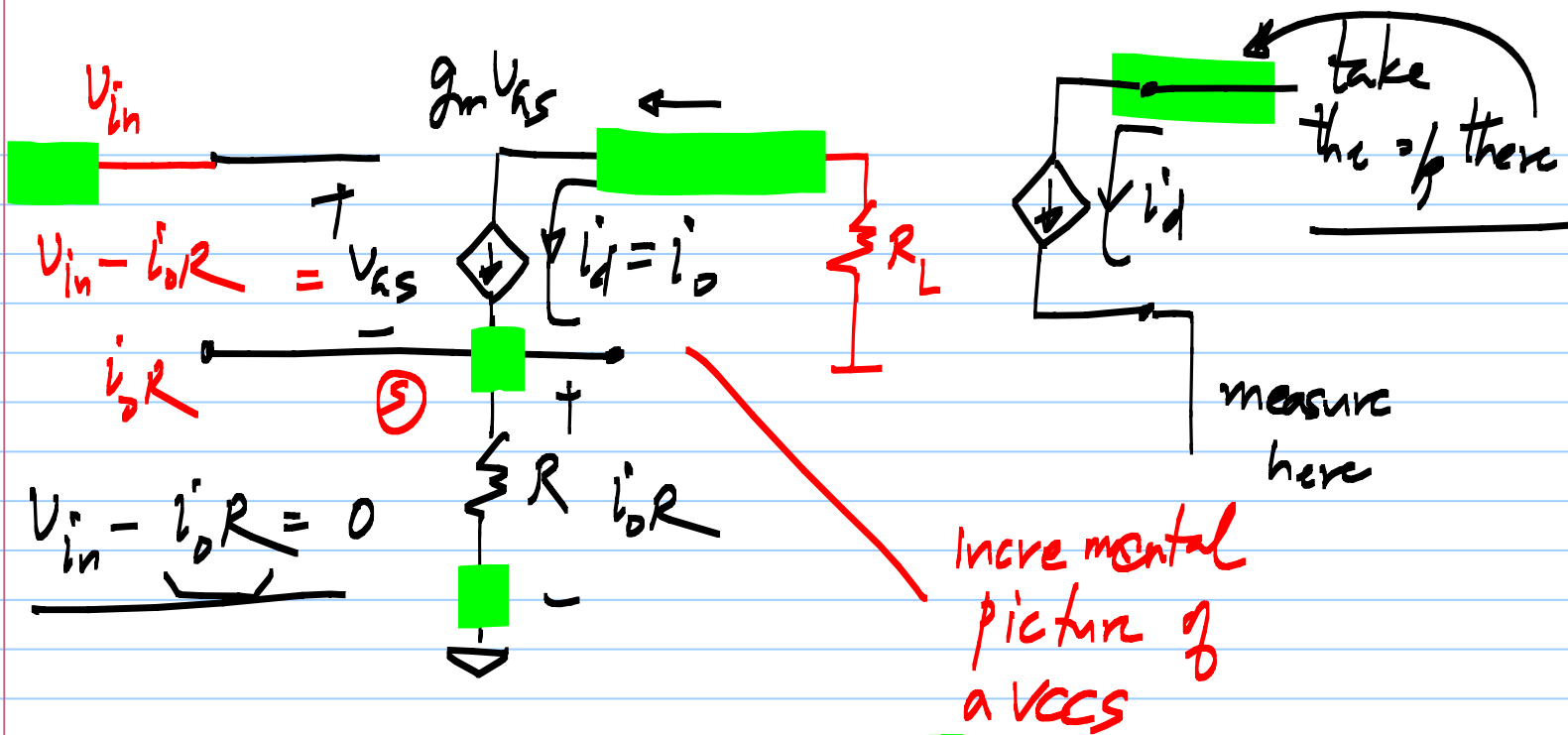


$i_o'$ : large  $\Rightarrow V_{as}$  must  $\downarrow$   
 $i_o'$ : small  $\Rightarrow V_{as}$  must  $\uparrow$

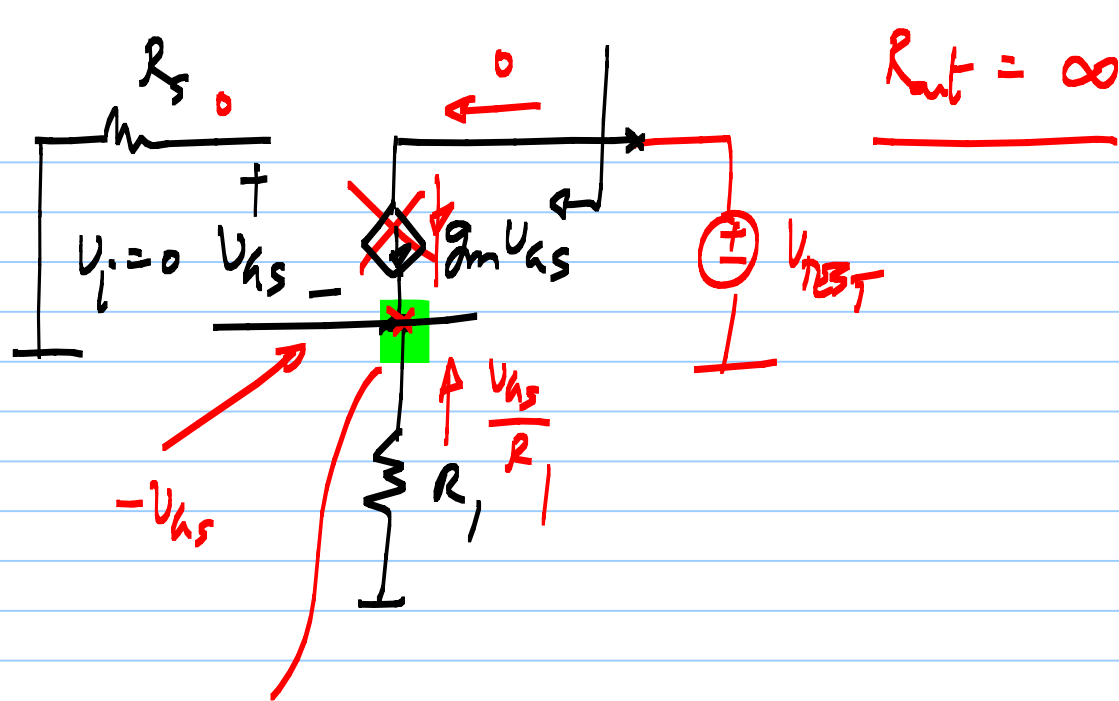
$V_{as} = V_{in} - i_o' R_1$  :

$(V_{in} - i_o' R_1) = 0$

$V_{as} = i_o' R_1 - V_{in}$



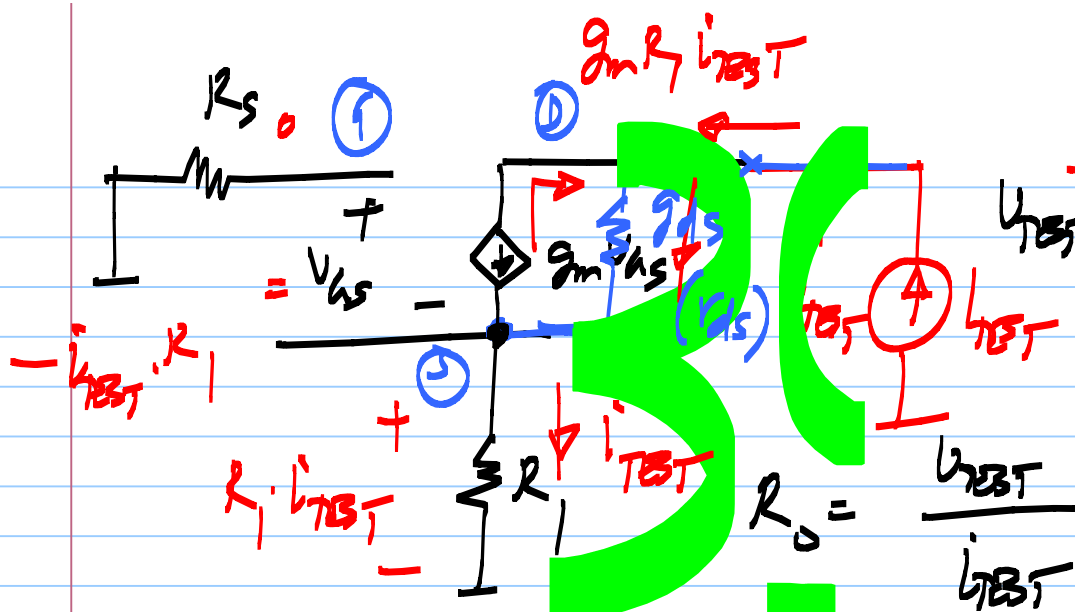




$$R_{out} = \infty$$

$$\underbrace{V_{CCS}}_{R_{in} = \infty}; \quad \underbrace{R_{out} = \infty}$$

$$\left[ \frac{V_{gs}}{R_s} + g_m V_{gs} = 0 \right] \quad \underline{V_{gs} = 0}$$



$$\underline{g_m R_1 i_{TEST} + i_{TEST}}$$

$$V_{TEST} = g_m R_1 r_{ds} \cdot i_{TEST} + r_{ds} \cdot i_{TEST} + R_1 i_{TEST}$$

$$R_o = \frac{V_{TEST}}{i_{TEST}}$$

$$= \underline{g_m r_{ds} R_1 + r_{ds} + R_1}$$

high output resistance

$$- g_m R_1 \cdot i_{TEST}$$

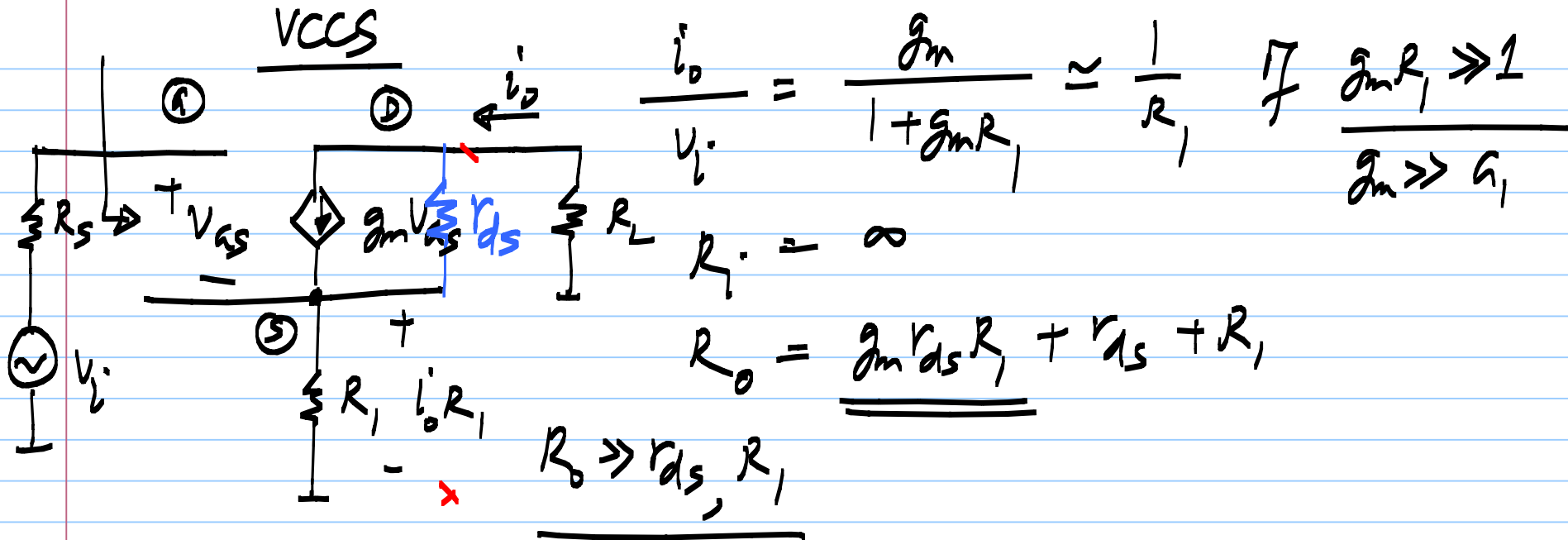
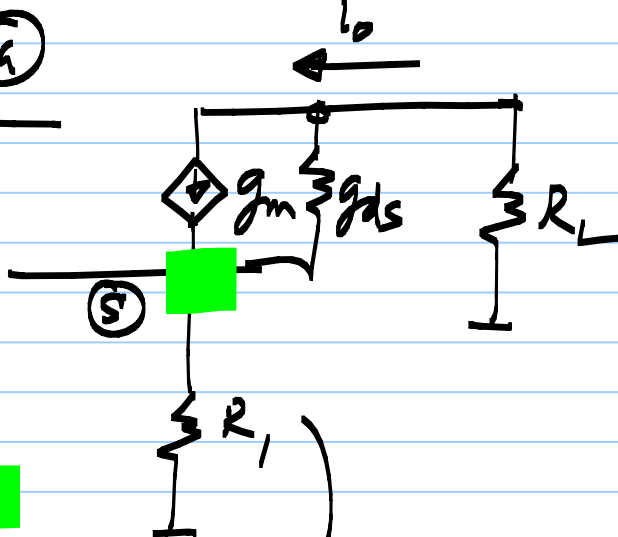
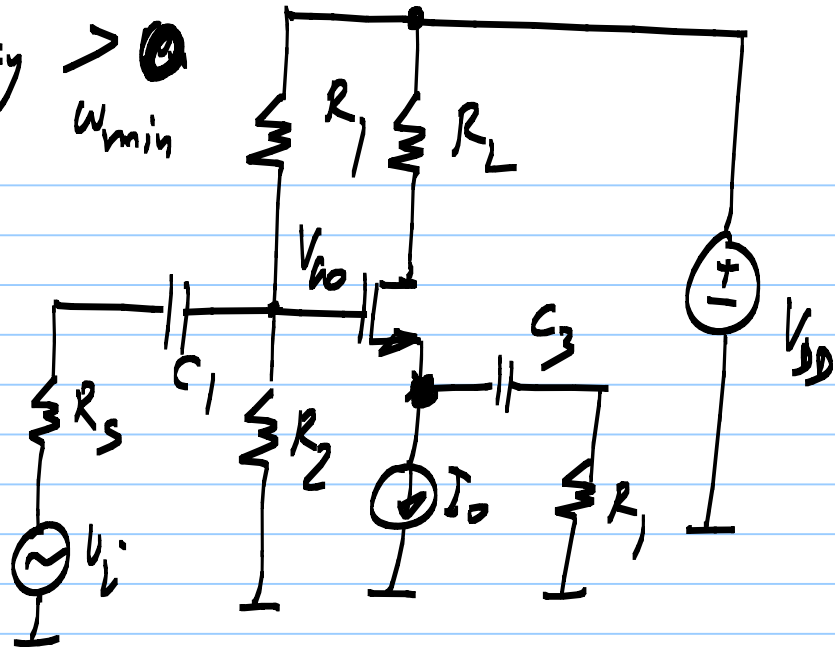


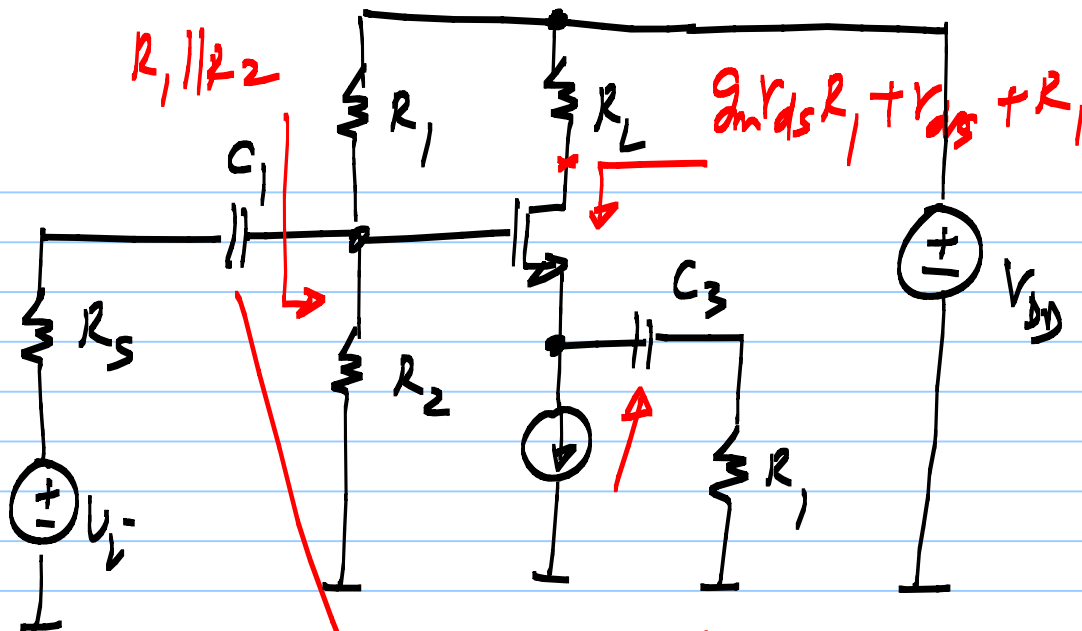
Diagram (a) shows a series circuit. A voltage source  $V_i$  is connected in series with a resistor  $R_S$ . This combination is connected to a load resistor  $R_L$ . The output voltage  $V_o$  is measured across  $R_L$ .

input signal frequency  $> \omega_{\min}$



defines the transconductance of the VCCS





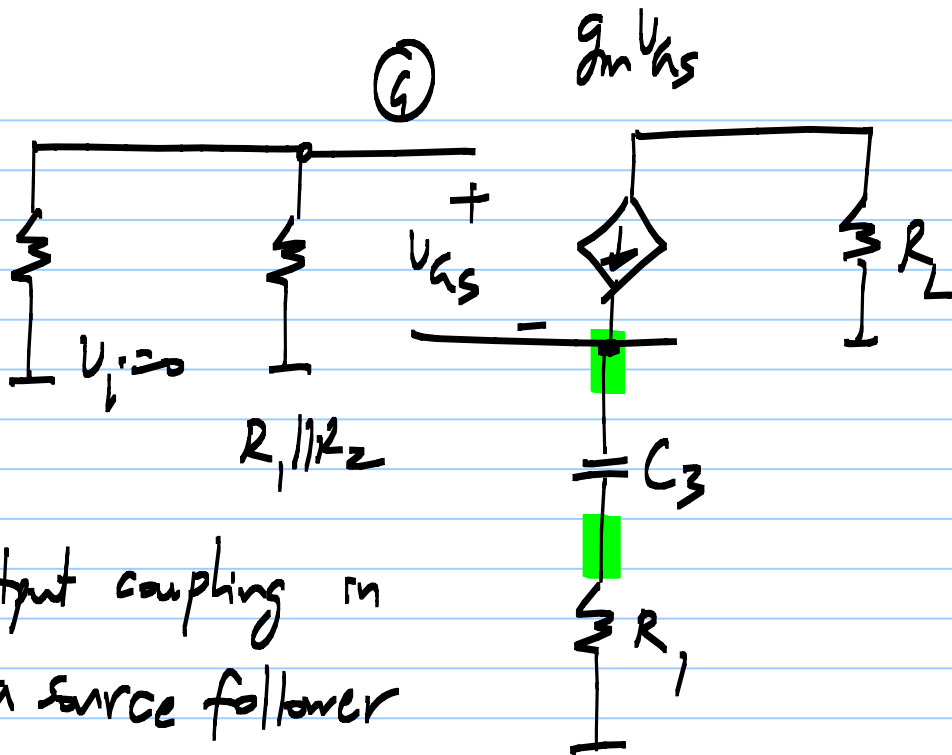
$R_1 || R_2 \gg R_s$   
 $C_1 \gg \frac{1}{\omega(R_s + R_1 || R_2)}$

Resistance across  $C_3$

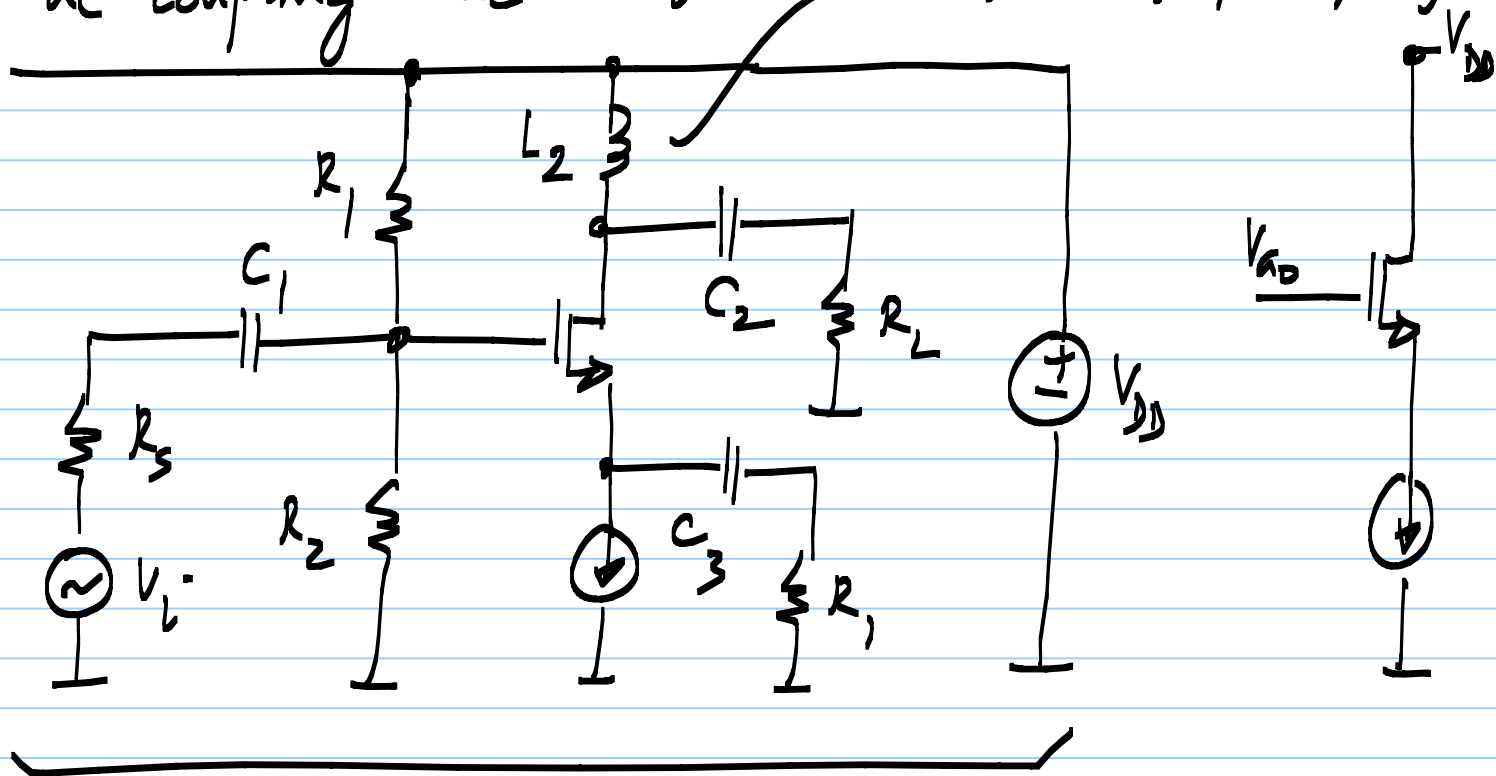
$$= \frac{1}{g_m} + R_1$$

$$C_3 \gg \frac{1}{\omega \left( \frac{1}{g_m} + R_1 \right)}$$

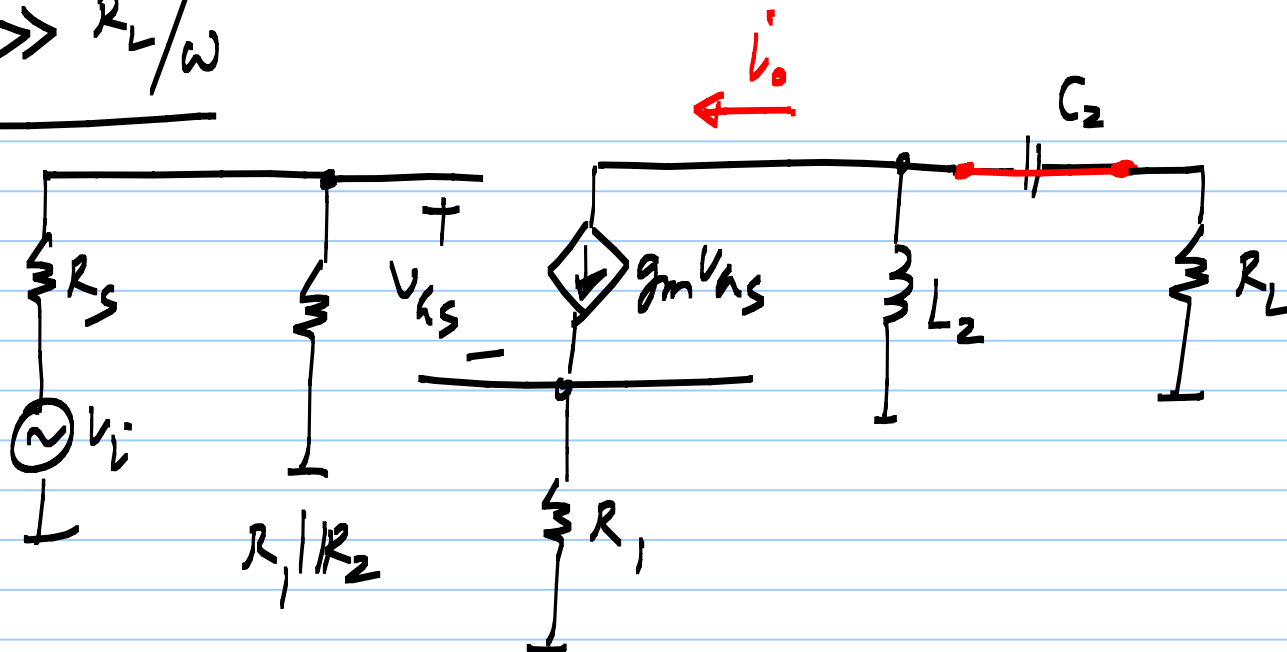
output coupling in  
a source follower



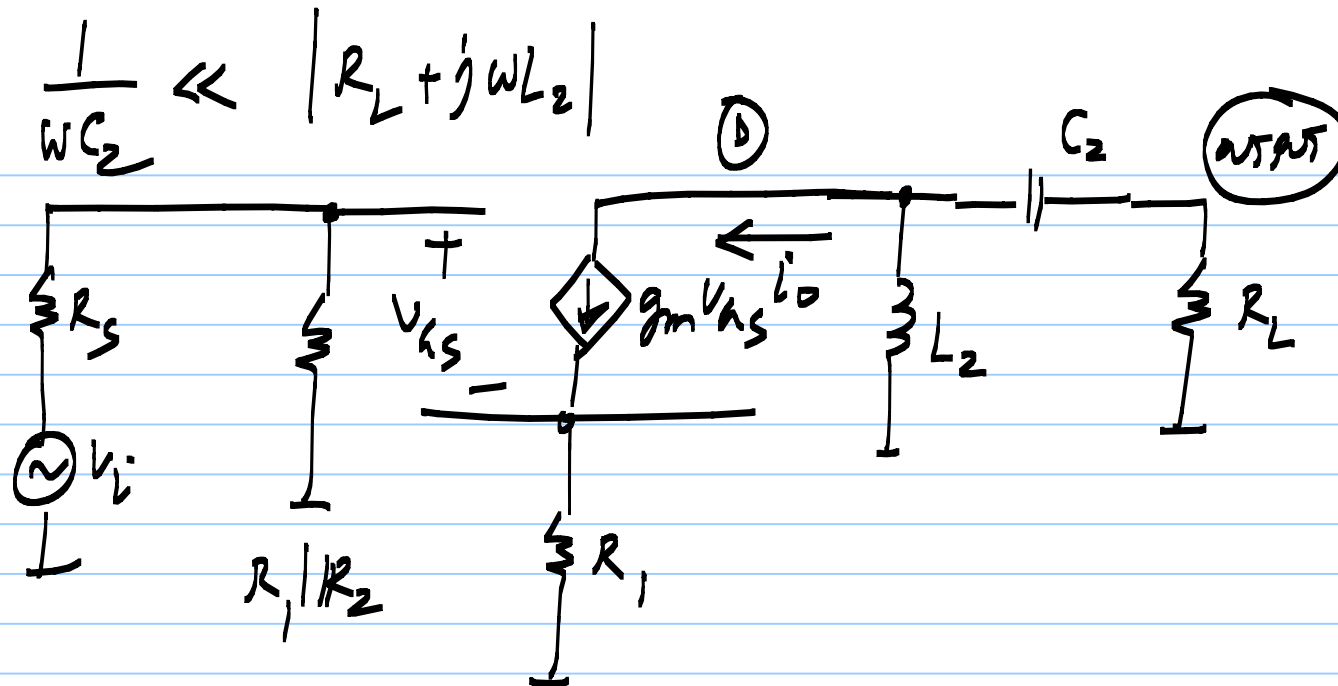
ac coupling the load. short circuit for dc, open for ac



$$\underline{L_2 \gg R_L/\omega}$$

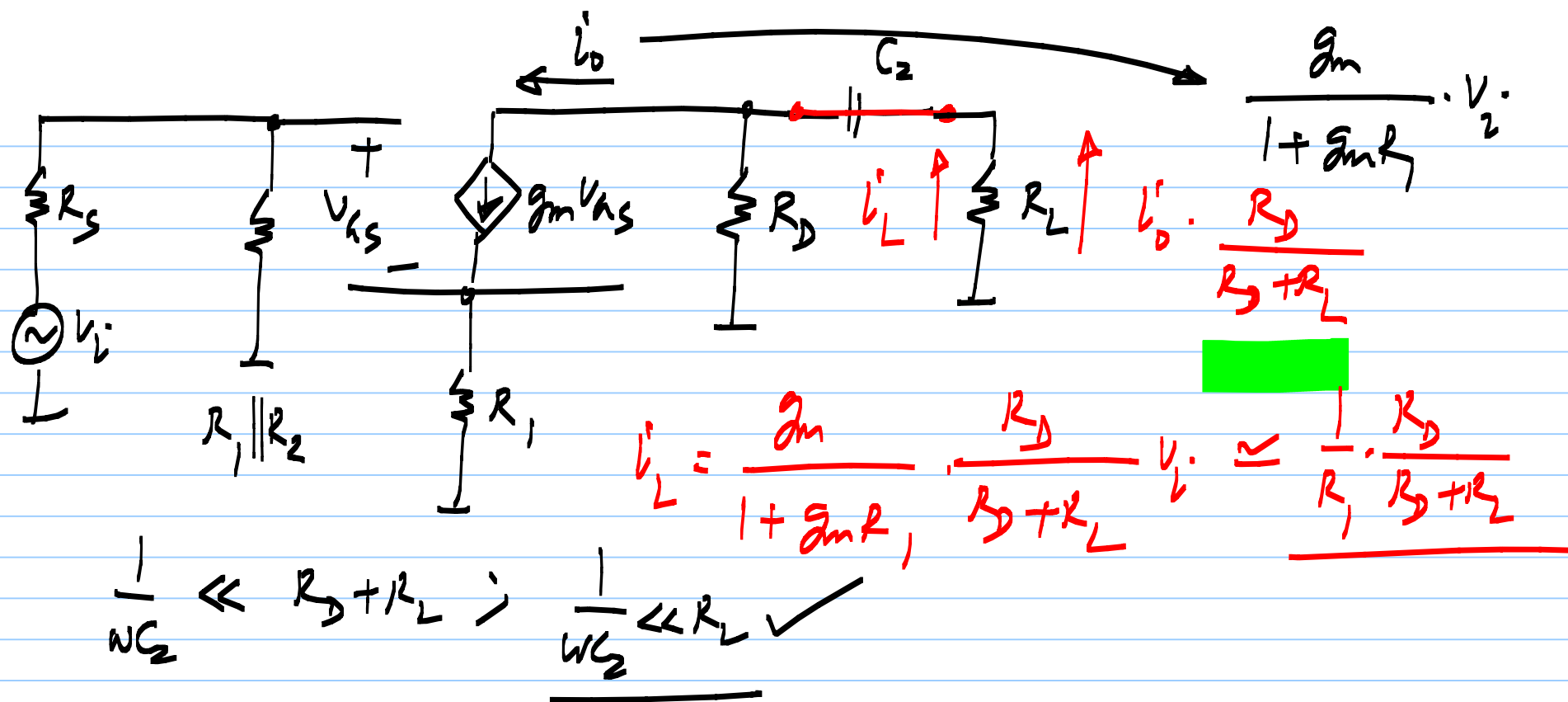


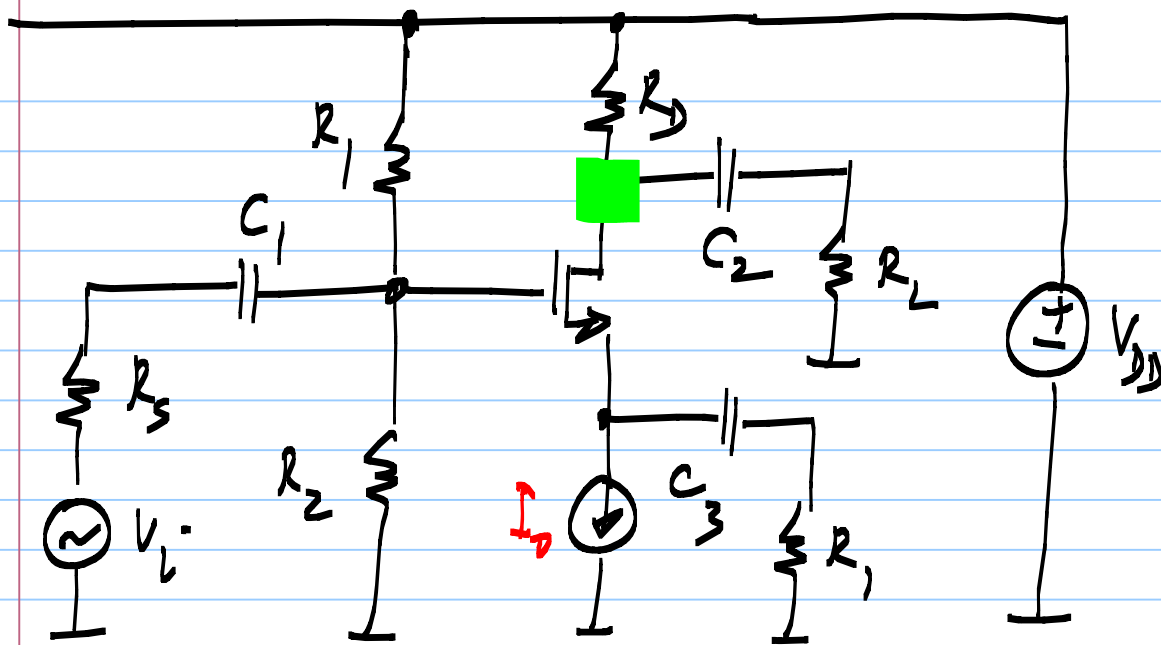
Almost all of  $i_o$  flows into  $R_L$  if  
 $\omega L_2 \gg R_L$



$$C_2 \gg \frac{1}{\omega R_L}$$

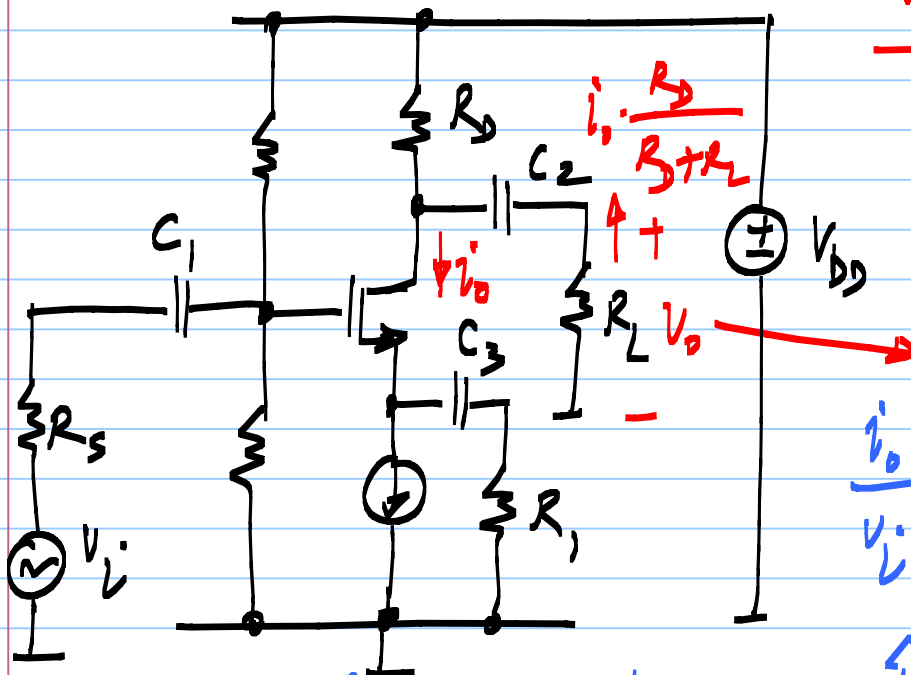
Reactance of  $C_2$   $\ll$  |impedance| across  $C_2$   
 $(1/\omega C_2)$





$R_D \uparrow \Rightarrow V_{DQ}$  has  
to be  $\uparrow$  to maintain  
the transistor in saturation

VCCS with a resistive load



$$\frac{i_o}{v_i} \approx \frac{1}{R_1} \text{ if } g_m R_1 \gg 1$$

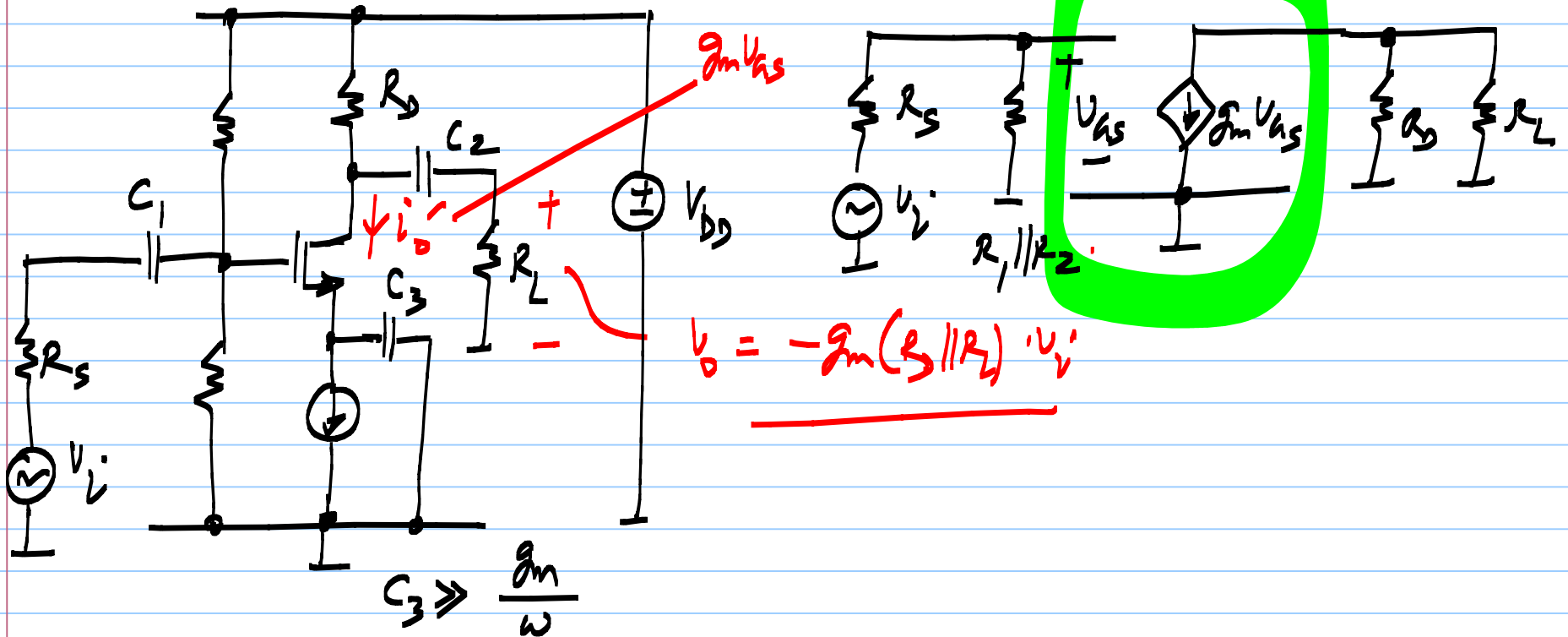
$$v_o = -i_o \left( \frac{R_D}{R_D + R_L} \cdot R_L \right)$$

$$= -\frac{g_m}{1 + g_m R_1} \cdot v_i \cdot (R_D \parallel R_L) \approx -v_i \cdot \frac{R_D \parallel R_L}{R_1}$$

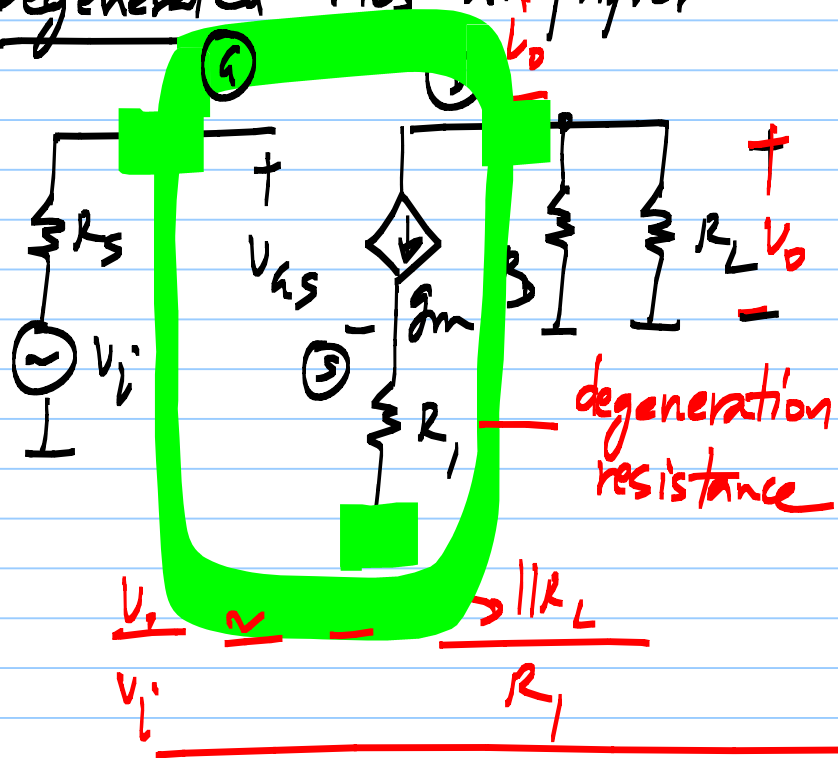
$$\frac{i_o}{v_i} = \frac{g_m}{1 + g_m R_1} \approx \frac{1}{R_1} < g_m$$

CS amplifier with source degeneration

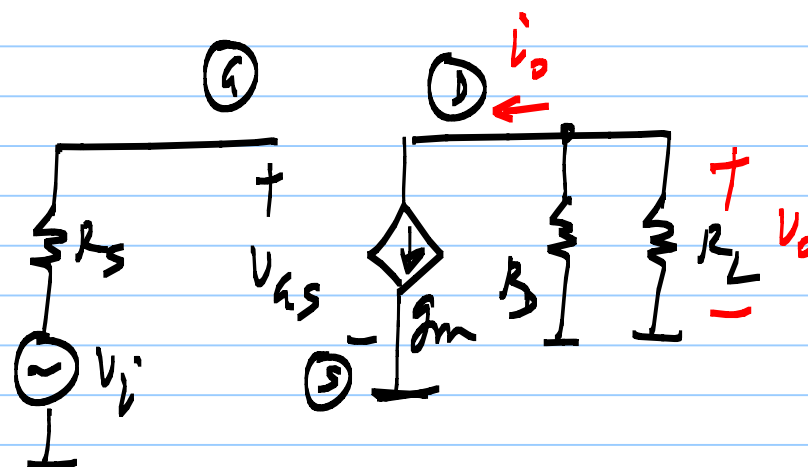
# CS amplifier w/ source feedback b1m



# VCCS w/ resistive load Degenerated MOS amplifier



# CS amplifier

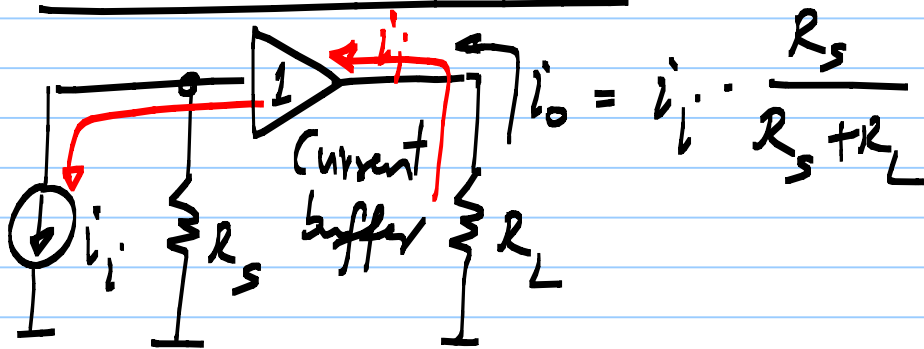


$$\frac{V_o}{V_i} = -g_m(R_D \parallel R_L)$$

## Current controlled current source (CCCS)

$$i_o = k i_i ; \quad \underline{k=1} \quad i_o = i_i \quad \text{Current buffer}$$

$$\underline{R_i \rightarrow 0 ; R_o \rightarrow \infty}$$



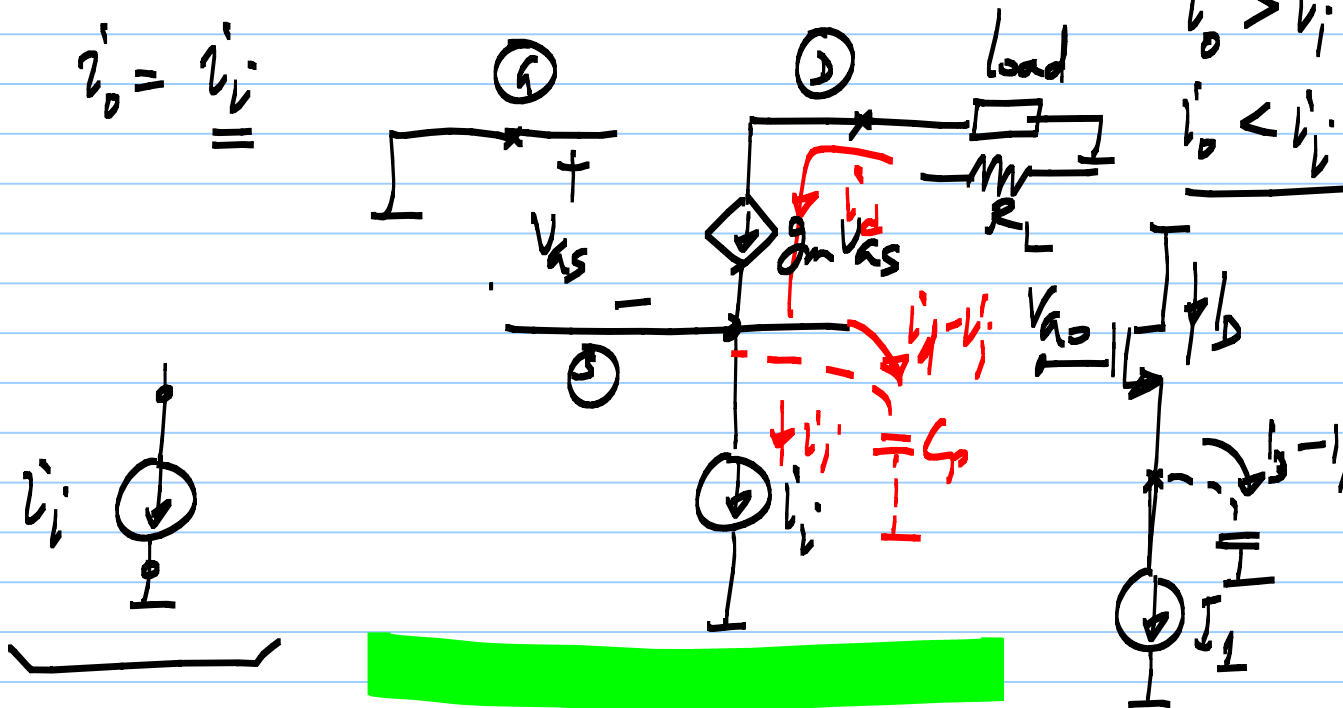
# CCCS using a MOS transistor

$$i_o = i_i$$

Compare  $i_o$  to  $i_i$

$i_o > i_i$  reduce  $V_{GS}$

$i_o < i_i$  increase  $V_{GS}$



# CCVS using a MOS transistor

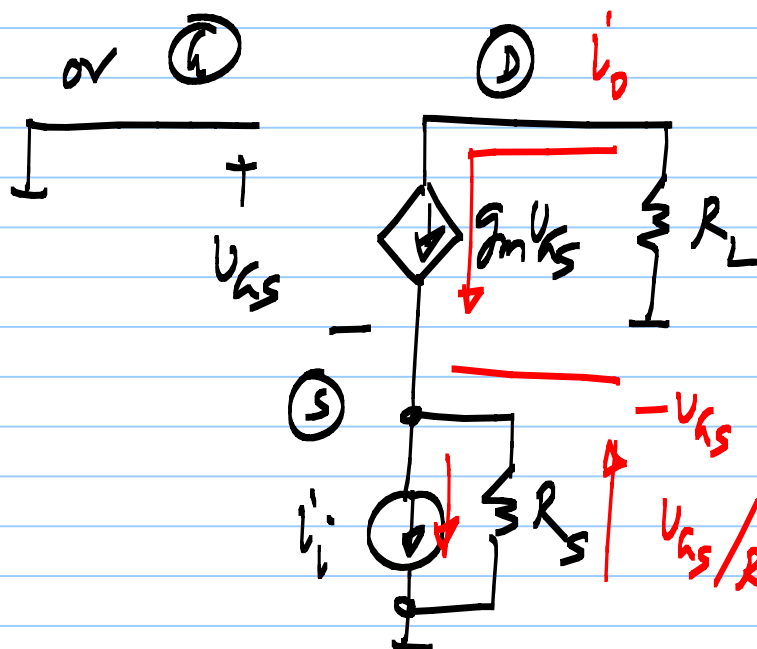
$$i_i = g_m v_{gs} + \underbrace{v_{gs}/R_s}_{v_{gs} \cdot g_s}$$

$$v_{gs} = \frac{i_i}{g_m + g_s}$$

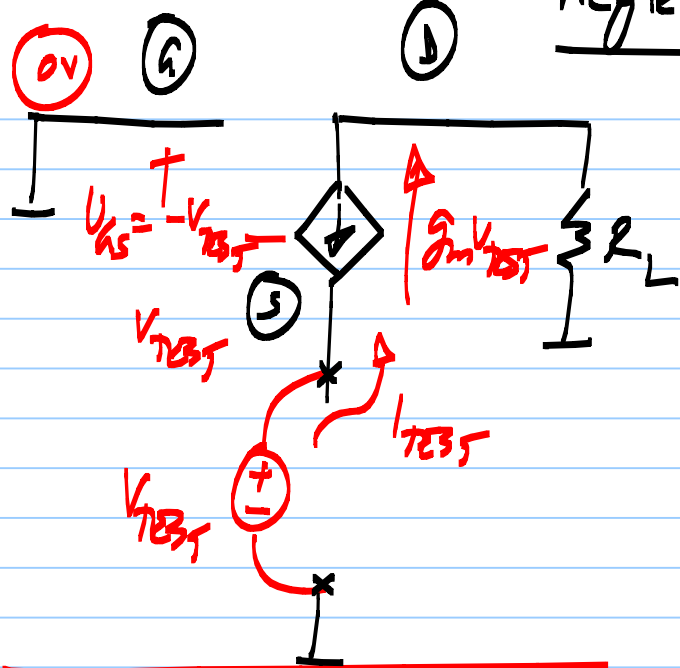
$$i_o = \frac{g_m}{g_m + g_s} \cdot i_i$$

$$i_o = i_i$$

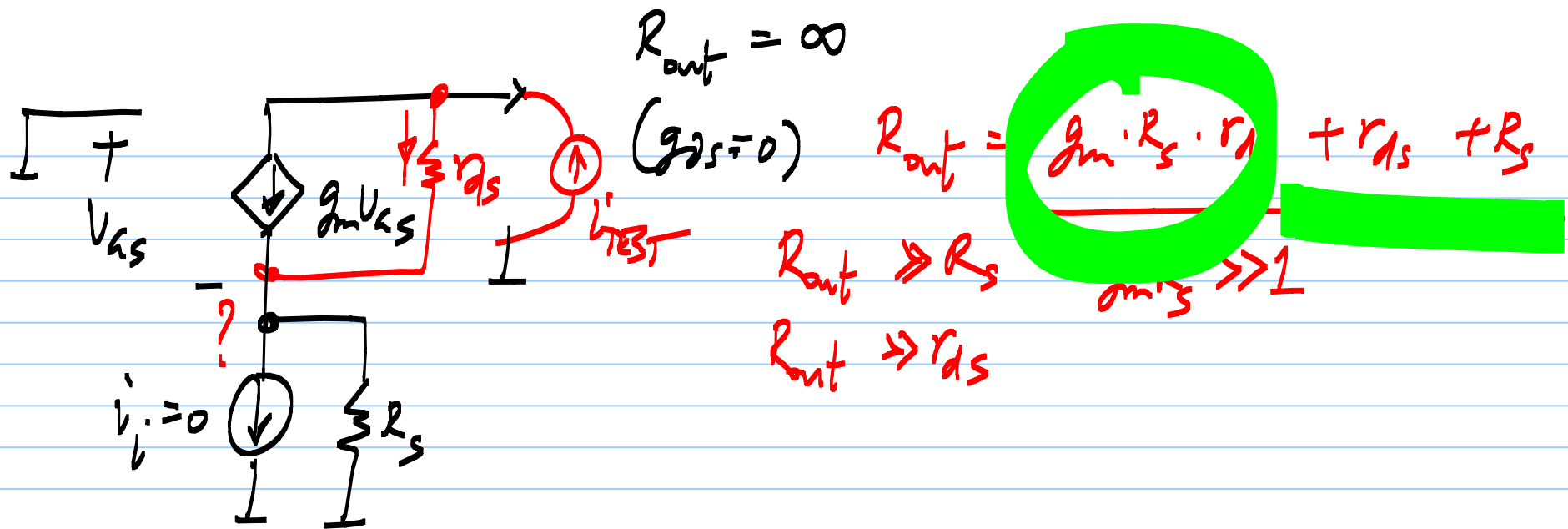
$$v_{gs}/R_s \approx i_i \quad \text{if } \underbrace{g_m R_s \gg 1}_{g_m \gg g_s}$$



neglected  $r_{ds}$

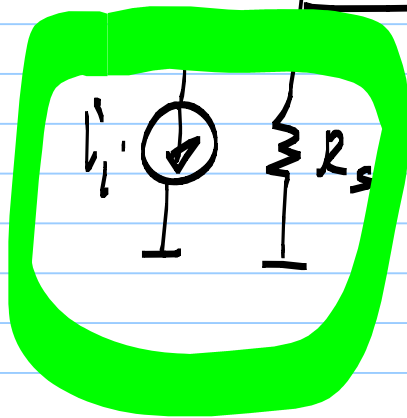
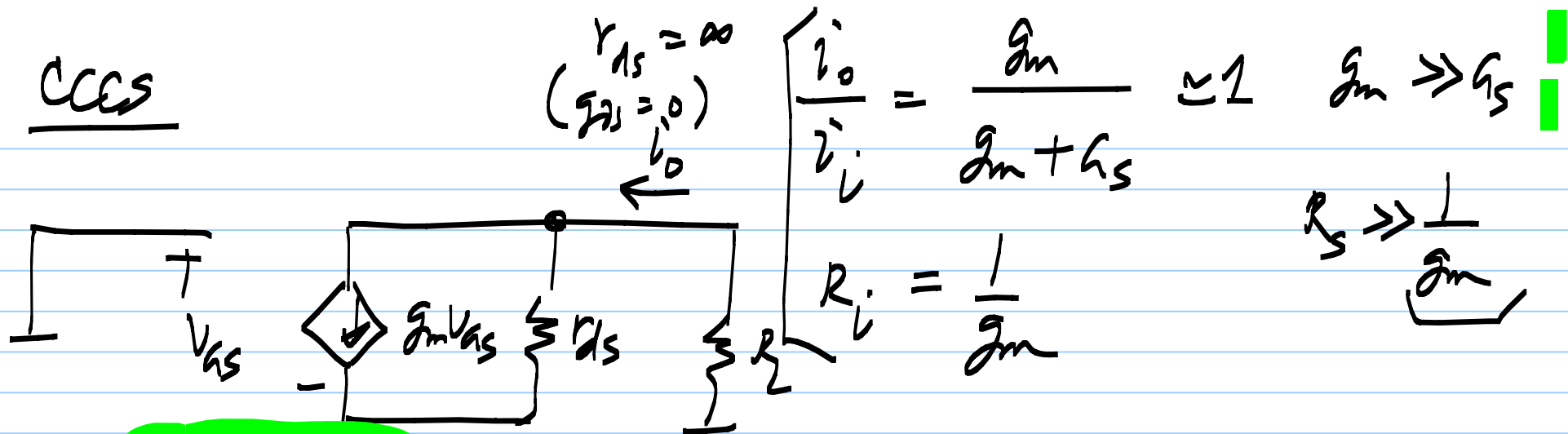


$$R_i = \frac{v_{gs}}{i_{gs}} = \frac{1}{g_m}$$



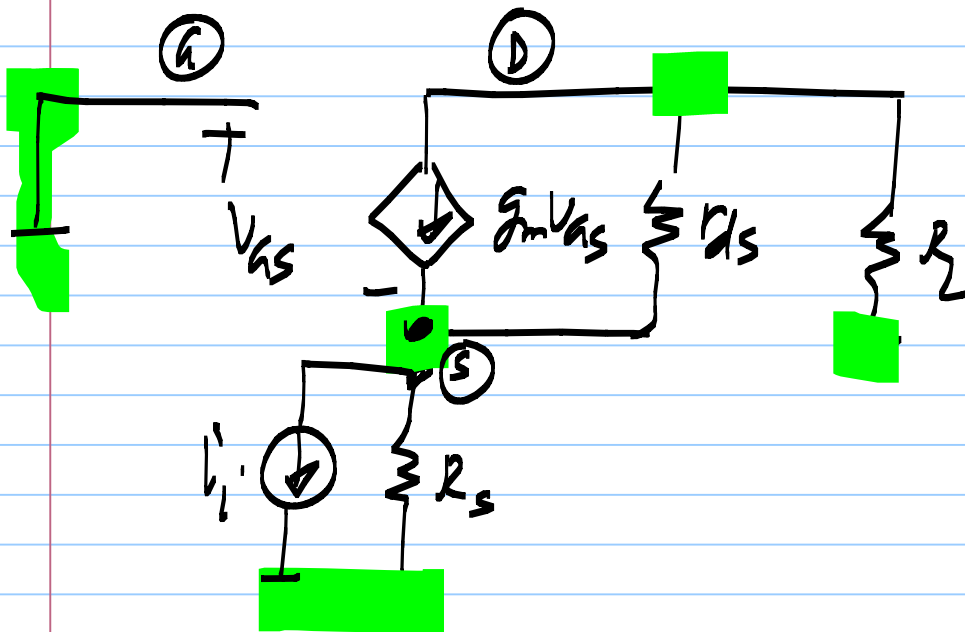
$R_{out}$  of a VCCS

CCCS



$$R_{out} = g_m R_s r_{ds} + R_s + r_{ds}$$

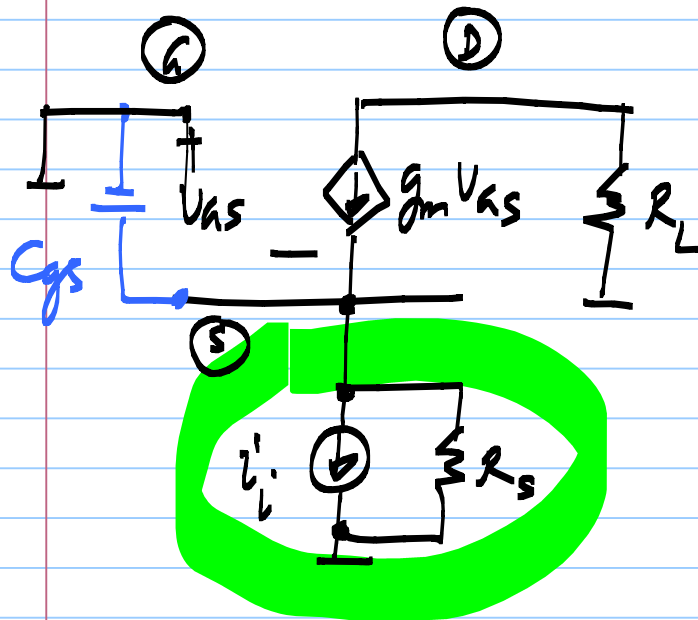
CCCS



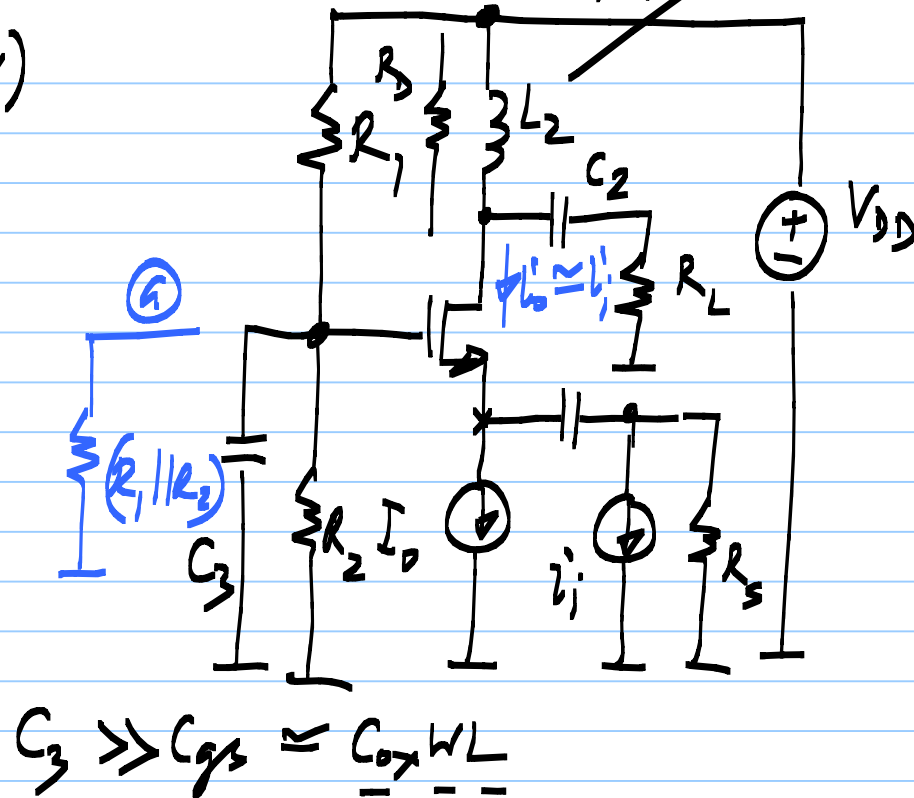
Input: source-gate  
output: drain-gate

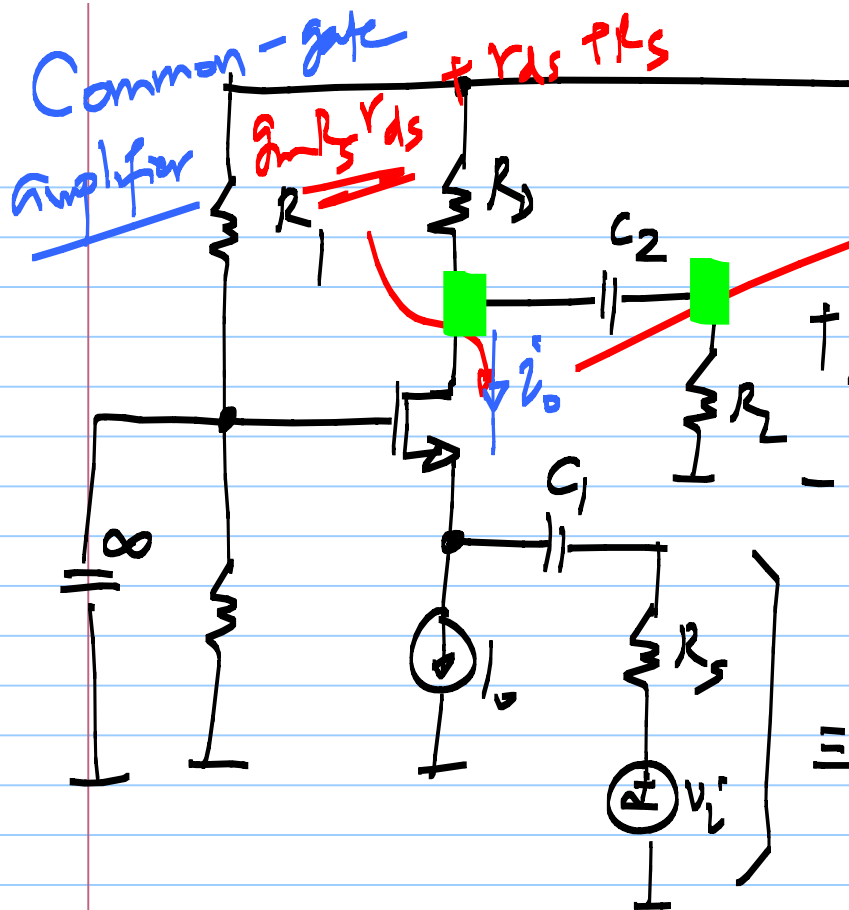
Common gate amplifier

CCCS with gain = 1  
(Common gate amplifier)



Common gate amplifier ~~choke~~





$$i_o \approx -\frac{v_i}{R_S}$$

$$i_o = -\frac{v_i}{R_S} \left[ \frac{g_m}{g_m + g_s} \right]$$

$$v_o = -i_o (R_D \parallel R_L) = v_i \cdot \frac{R_D \parallel R_L}{R_S}$$

$$= v_i \cdot \frac{R_D \parallel R_L}{R_S} \left( \frac{g_m}{g_m + g_s} \right)$$

$$\frac{g_m R_S}{g_m R_S + 1}$$

neglecting  $r_{ds}$

if  $g_m R_S \gg 1$

# Transimpedance amplifier Current controlled voltage source (CCVS) Using a MOS transistor

$$V_o = i_i \cdot R_m$$

Transresistance

must be  
current drawn  
from the o/p  
node

$$V_o - i_i R_m > 0$$

output  $V_o$  must be pulled down

$$V_o - i_i R_m < 0$$

output  $V_o$  must be pushed up

Current must  
be pushed into  
the o/p node.



CCVS Error	o/p voltage
$V_o - i_i R_m > 0$	must be reduced
$V_o - i_i R_m < 0$	must be increased

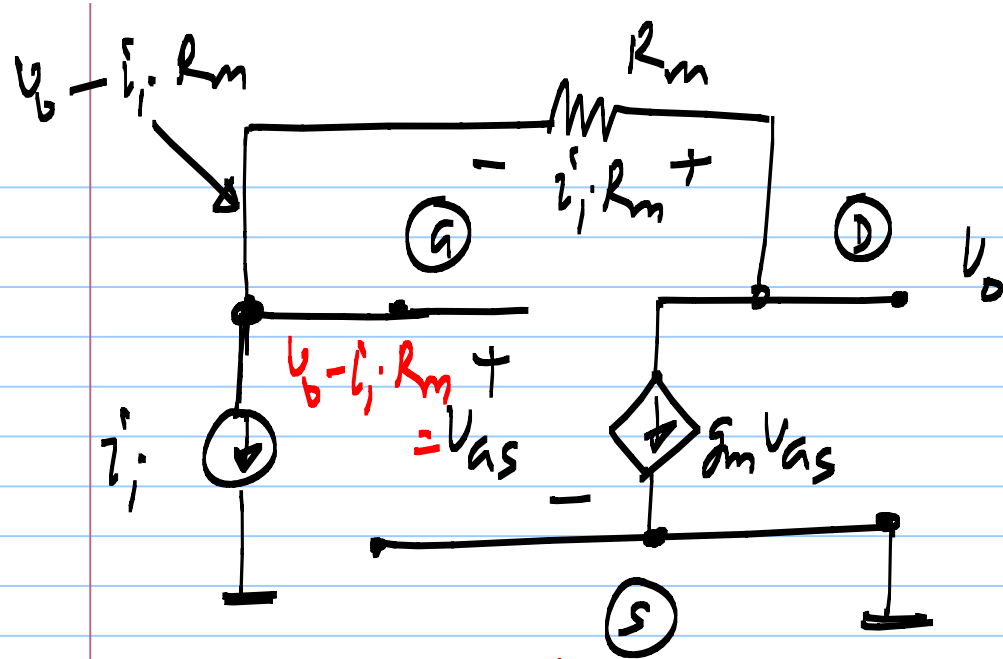
$$V_{as} = V_o - i_i R_m$$

o/p : drain terminal

Transistor:

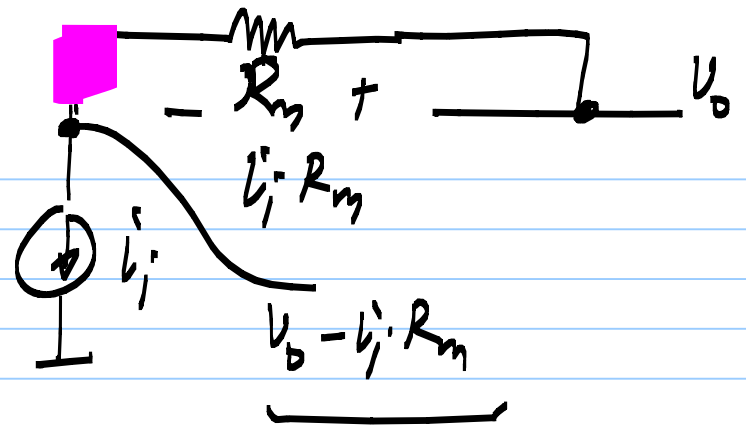
$$V_{as} > 0$$

pulls current from the drain;  
pushes current out of the source;

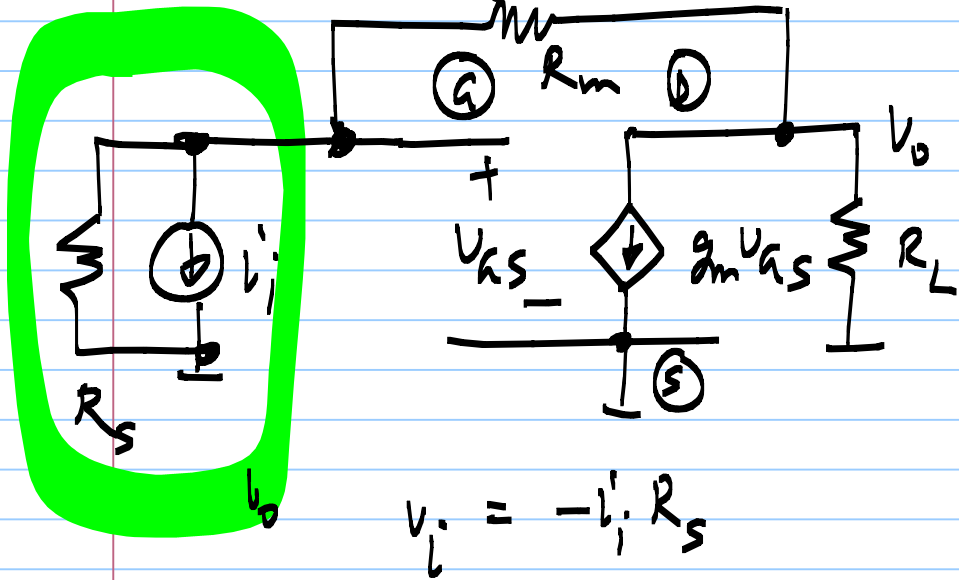


$$\underline{V_o - i_i \cdot R_m}$$

CCVS using a MOS transistor

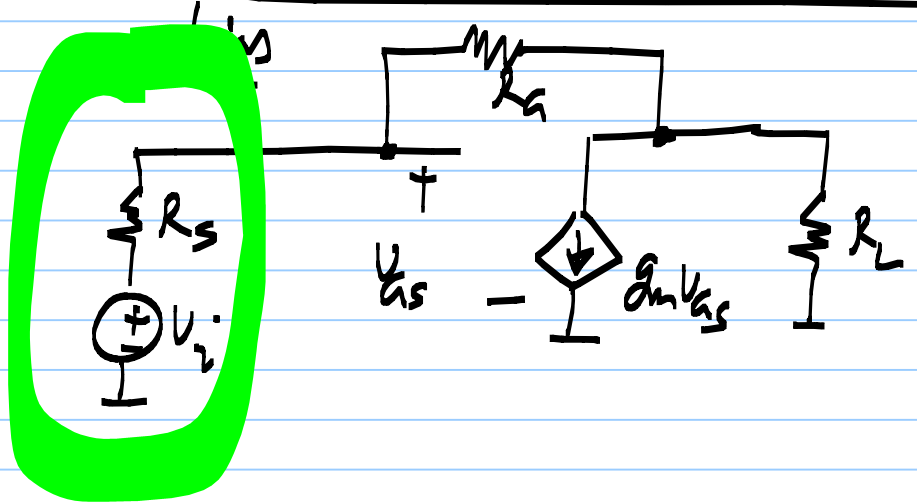


## CCVS using a MOS transistor



$$v_o = i_i' R_m$$

## CS amplifier using drain feedback



CS amp. w/ drain fb bias,

$$\frac{v_o}{\underbrace{v_i}_{-i_i R_s}} = - \left( \frac{g_m R_a R_L - R_L}{g_m R_L R_s + R_s + R_a + R_L} \right)$$

$$\frac{v_o}{i_i} = \frac{(g_m R_m R_L - R_L) R_s}{g_m R_L R_s + R_s + R_m + R_L} \approx R_m$$

$$\frac{v_o}{i_i} = R_m$$

$$g_m R_m \gg 1; g_m R_L R_s \gg R_s, R_m, R_L$$

$$\frac{V_o}{i_i} = \frac{(g_m R_m R_L - R_L) R_s}{g_m R_L R_s + R_s + R_m + R_L}$$

$$\frac{g_m R_m R_L - R_L}{g_m R_L + 1 + \frac{R_m + R_L}{R_s}}$$

$R_s = \infty$  (ideal input current source).

$$g_m R_m \gg 1$$

$$g_m R_L \gg 1$$

$$\frac{R_m - 1/g_m}{1 + 1/g_m R_L} \approx R_m$$

$$R_s \rightarrow \infty$$

$$\frac{v_o}{i_i} = \frac{(g_m R_m R_L - R_L) R_S}{g_m R_L R_S + R_S + R_m + R_L}$$

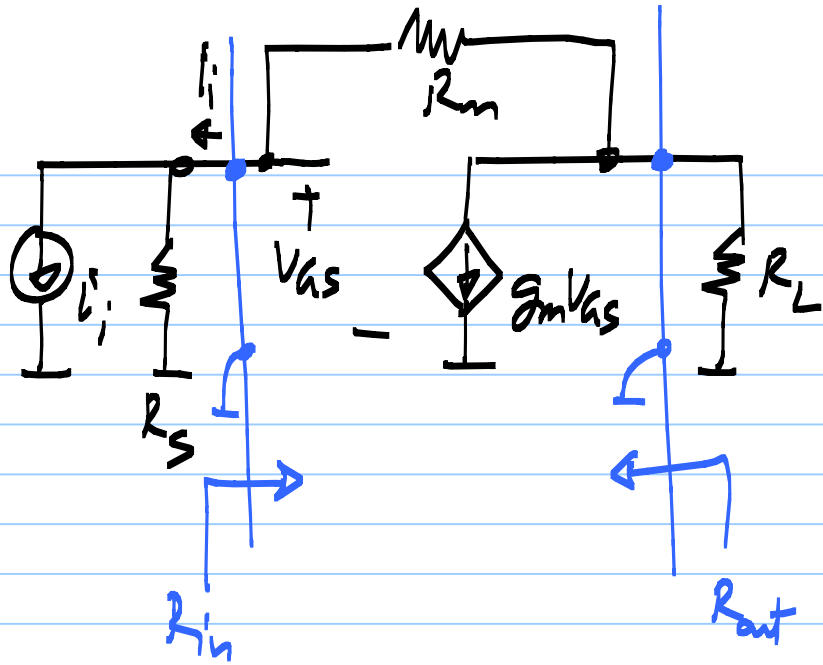
CCVS

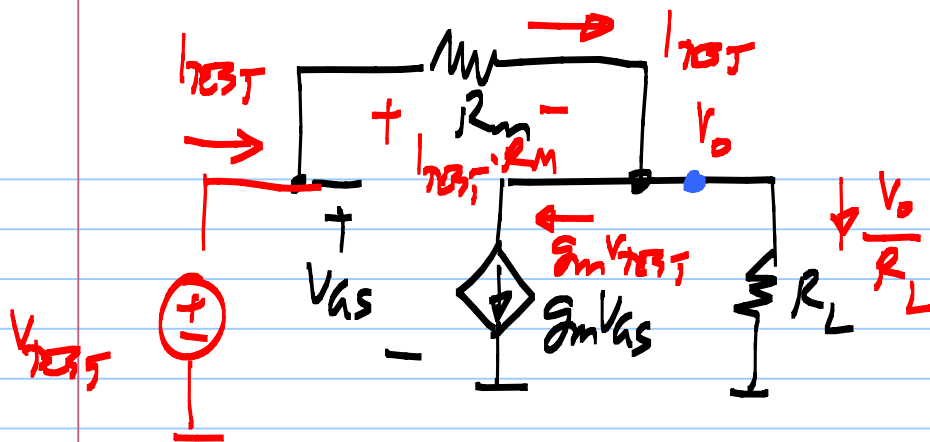
dominant  $\Rightarrow \frac{v_o}{i_i} \approx R_m$

$$\frac{v_o}{v_i} = - \left( \frac{g_m R_a R_L - R_L}{g_m R_L R_S + R_S + R_a + R_L} \right)$$

CS amplifier w/ drain fb. bias dominant

$$\frac{v_o}{v_i} \approx -g_m R_L$$

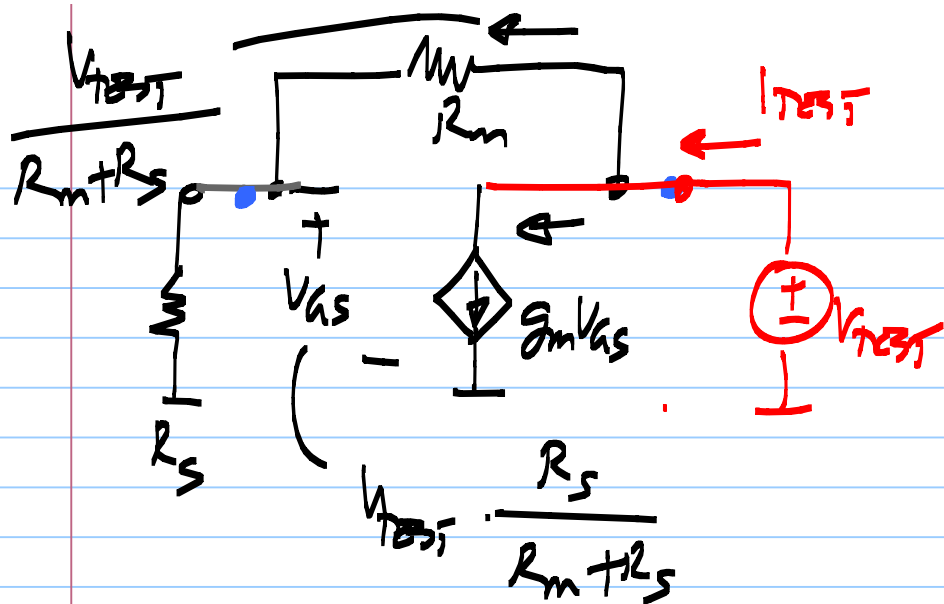




$$V_o = V_{TEST} - I_{TEST} R_m$$

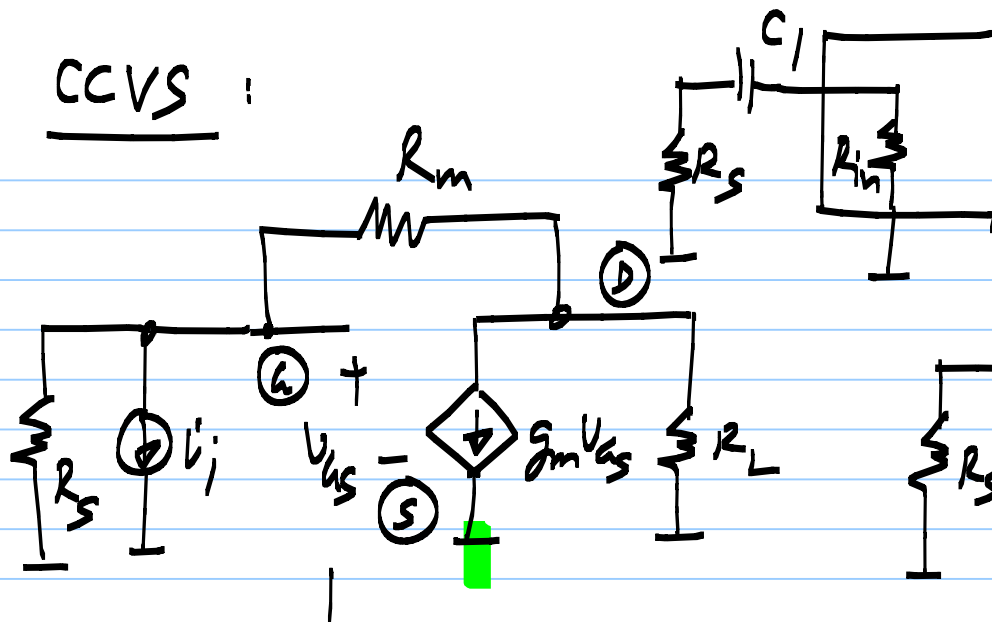
$$I_{TEST} = g_m V_{TEST} + \frac{V_o}{R_L}$$

$$R_{in} = \frac{V_{TEST}}{I_{TEST}} = \frac{R_L + R_m}{g_m R_L + 1} \rightarrow 0 \text{ if } g_m \rightarrow \infty$$



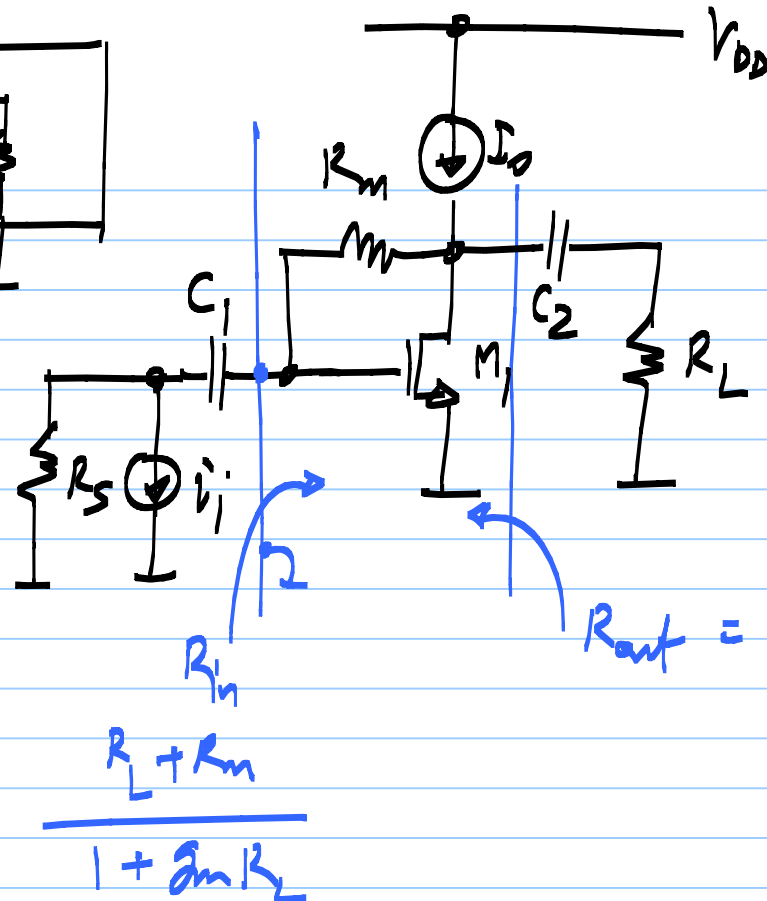
$$R_{out} = \frac{V_{test}}{I_{test}} = \frac{R_s + R_m}{g_m R_s + 1} \rightarrow 0 \quad \text{as } g_m \rightarrow \infty$$

CCVS :



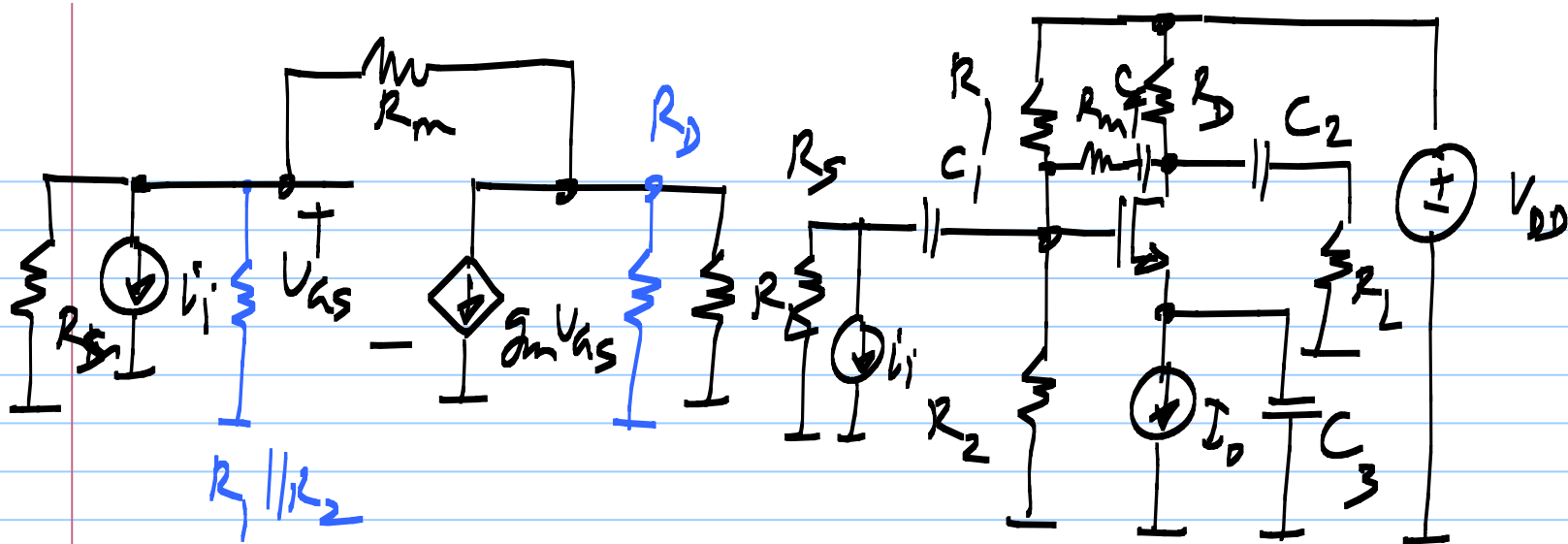
$$C_1 \gg \frac{1}{\omega (R_S + R_{in})}$$

$$C_2 \gg \frac{1}{\omega (R_{out} + R_L)}$$



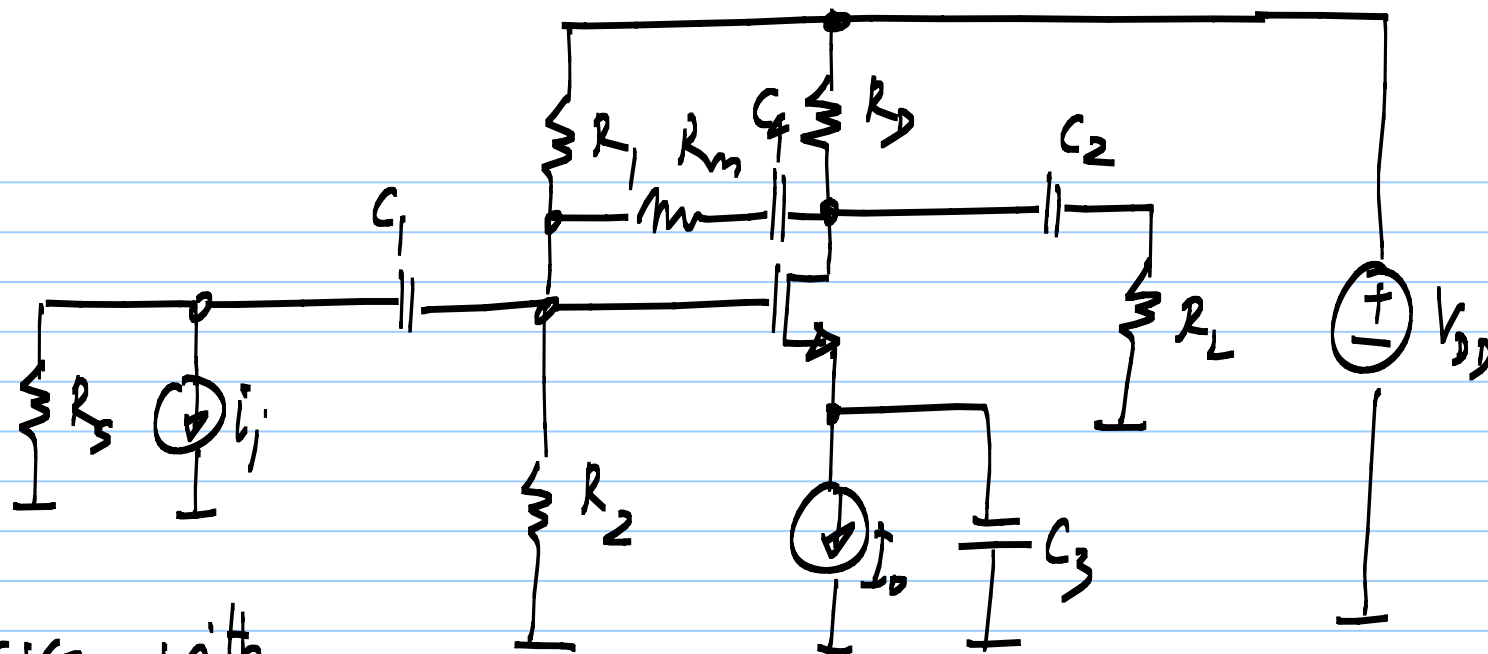
$$R_{out} = \frac{R_S + R_m}{1 + g_m R_S}$$

$$\frac{R_L + R_m}{1 + g_m R_L}$$



$$R_S \rightarrow R_1 || R_2 || R_S$$

$$R_L \rightarrow R_2 || R_D$$



CCVS with

source feedback bias