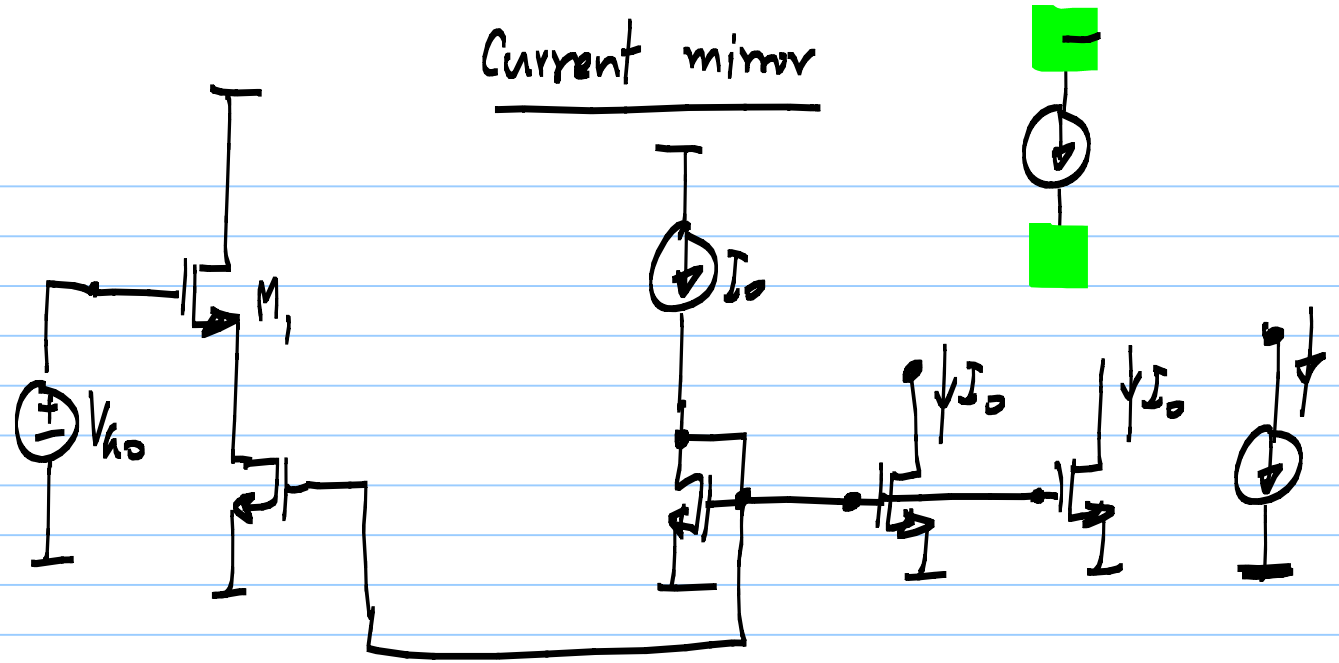
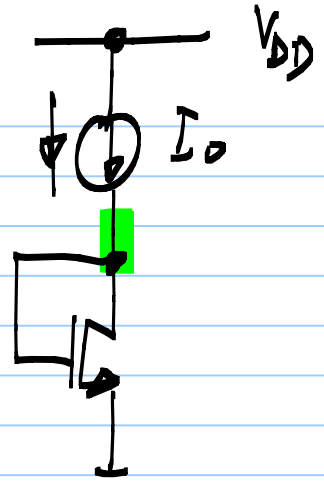
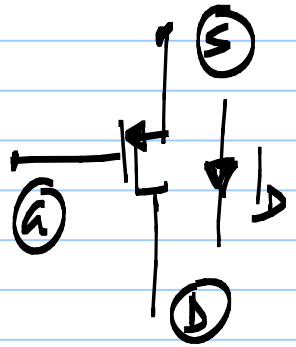
Current mirror

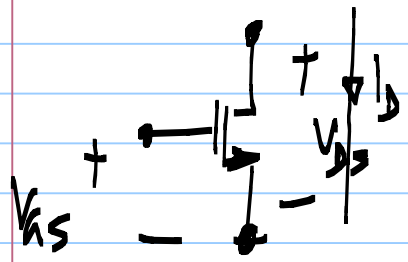




"p" MOS transistor

pMOS transistor

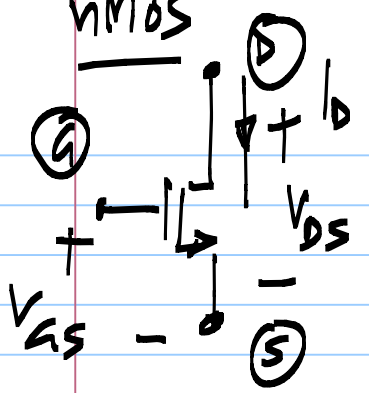




"n" MOS

nMOS

nMOS

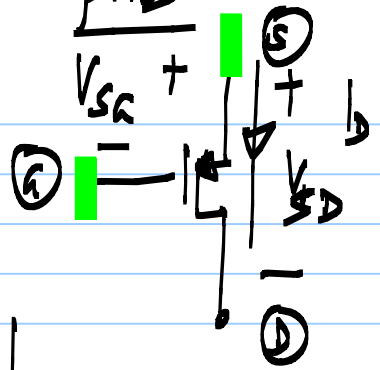


$V_{GS} > 0$, $V_{DS} > 0$,

$I_D > 0$

V_{Tn}

pMOS



$V_{SG}, V_{SD} > 0$

$I_D > 0$

$V_{Tp} > 0$

$I_D = 0$ $\quad V_{SG} < V_{Tp}$

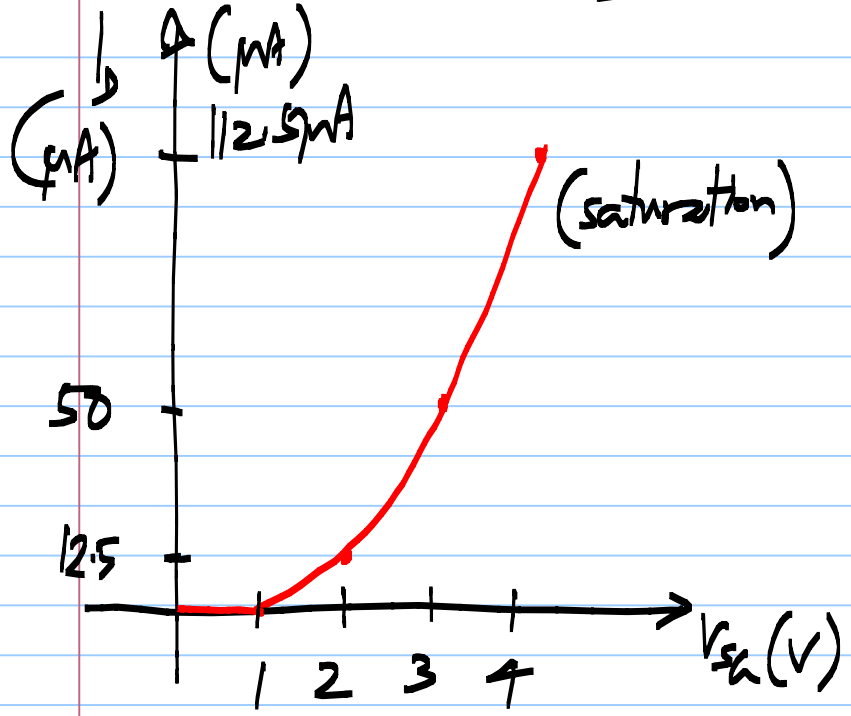
$= \mu_p C_{ox} \frac{W}{L} \left((V_{SG} - V_T) \cdot V_{SD} - \frac{V_{SD}^2}{2} \right)$ $\quad V_{SG} > V_{Tp}$, $V_{SD} < V_{SG} - V_{Tp}$

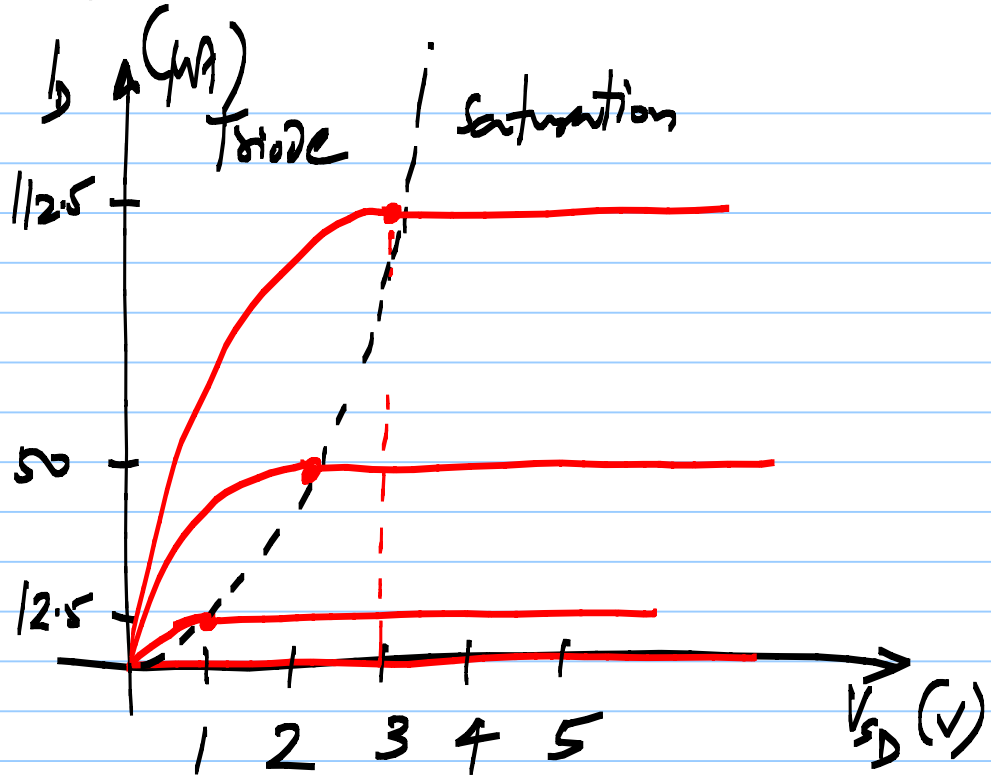
(Linear/triode region)

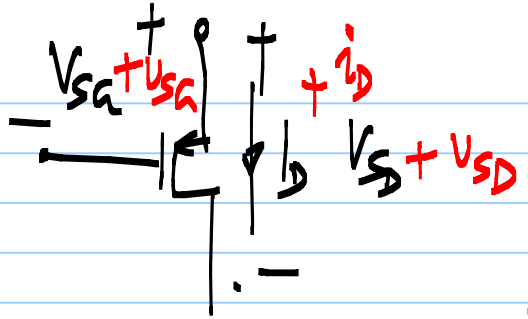
$= \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{SG} - V_T)^2$ $\quad V_{SG} > V_{Tp}$, $V_{SD} > V_{SG} - V_{Tp}$

(Saturation region)

$\mu_p C_x = 25\,\mu A/V^2$; $\frac{W}{L} = 1$; $V_{tp} = 1V$







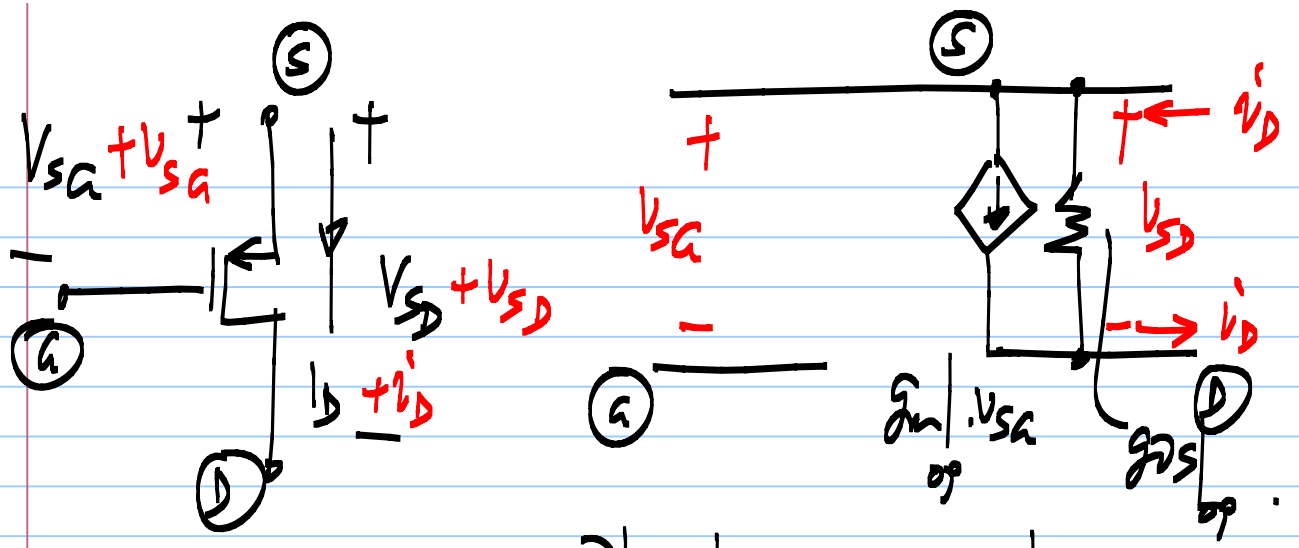
$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W}{L} (V_{SG} - V_{TP})^2 (1 + \lambda V_{SD})$$

saturation region

$$I_2 = f(V_1, V_2)$$

$$I_2 + i_2 = f(V_1 + v_1, V_2 + v_2)$$

$$i_2 = \left.\frac{\partial I_2}{\partial V_1}\right|_{op} \cdot v_1 + \left.\frac{\partial I_2}{\partial V_2}\right|_{op} \cdot v_2$$



$$i_D' = \left.\frac{\partial I_D}{\partial V_{SG}}\right|_{op} \cdot v_{SG} + \left.\frac{\partial I_D}{\partial V_{SD}}\right|_{op} \cdot v_{SD} = g_m|_{op} \, v_{SG} + g_{DS} \cdot v_{SD}$$

$$I_D = \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{SG} - V_{TP})^2 (1 + \lambda V_{SD})$$

(saturation)

$$g_m = \frac{\partial I_D}{\partial V_{SG}} = \mu_p C_{ox} \frac{W}{L} (V_{SG} - V_{TP}) (1 + \lambda V_{SD})$$

$$\simeq \mu_p C_{ox} \frac{W}{L} (V_{SG} - V_{TP})$$

$$I_D = \frac{\mu_p C_{ox}}{2} \frac{W}{L} (V_{SG} - V_{TP})^2 (1 + \lambda V_{SD})$$

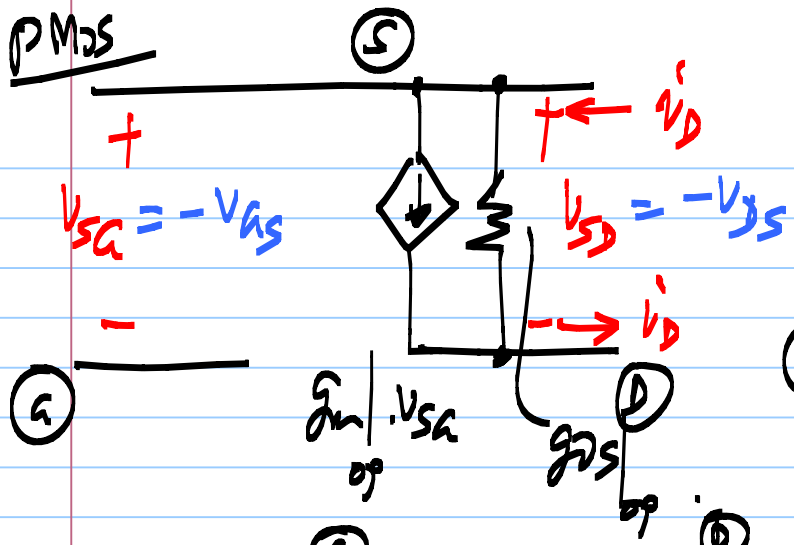
(saturation)

$$g_{DS} = \frac{\partial I_D}{\partial V_{SD}} = \underbrace{\frac{\mu_p C_{ox}}{2} \cdot \frac{W}{L} (V_{SG} - V_{TP})^2}_{\simeq I_D} \cdot \lambda$$

(o/p conductance)

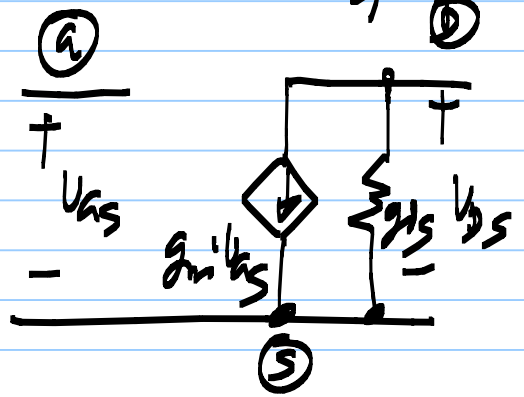
$$\simeq \lambda \cdot I_D$$

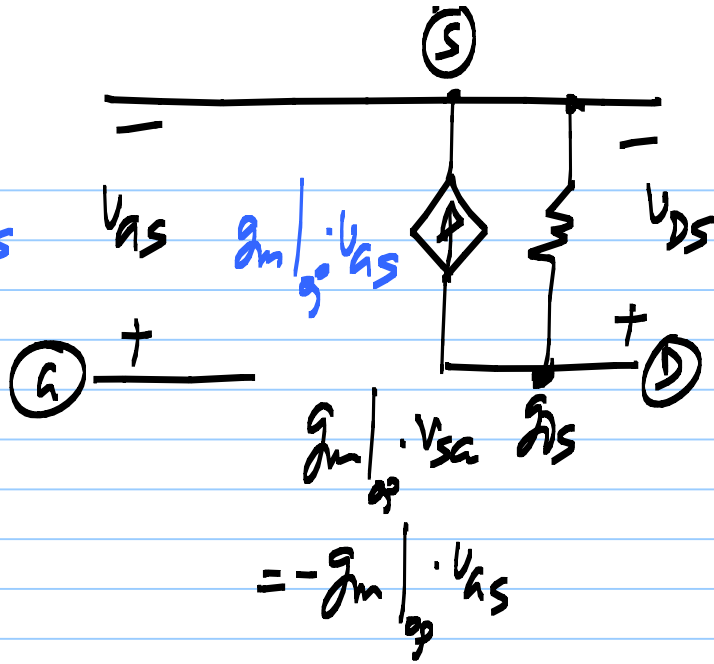
pMOS



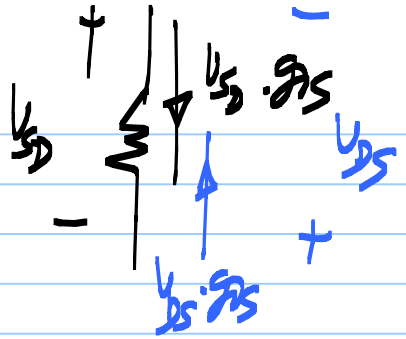
nMOS:

= pMOS

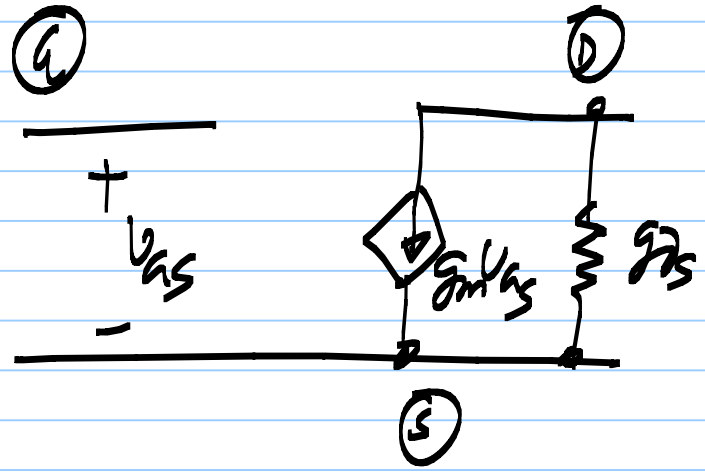




$= -g_m|_{op} \cdot v_{GS}$

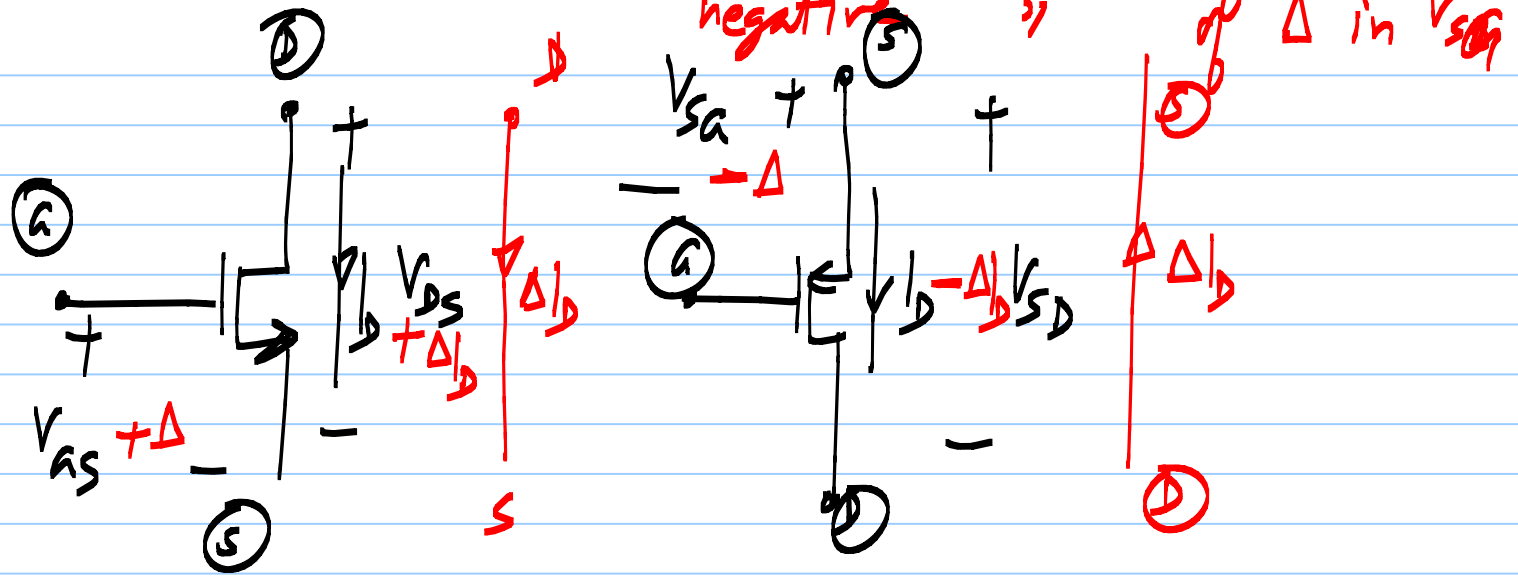


Incremental small-signal models of pMOS & nMOS are the same



positive increment of Δ in V_{GS}

negative " " Δ in V_{SG}

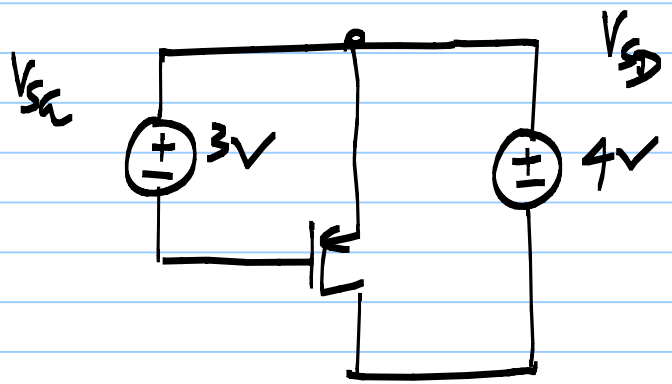


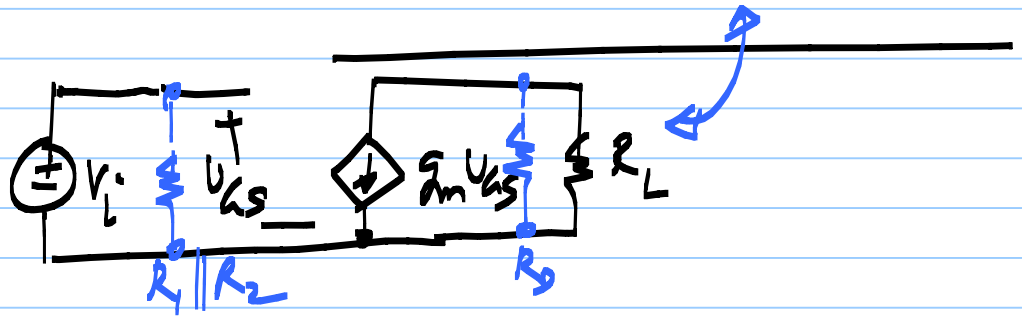
CS amplifier using a pMOS transistor.

$g_m = 200\mu S$

$V_{SG} = 3V$

$V_{SD} \geq 2V$

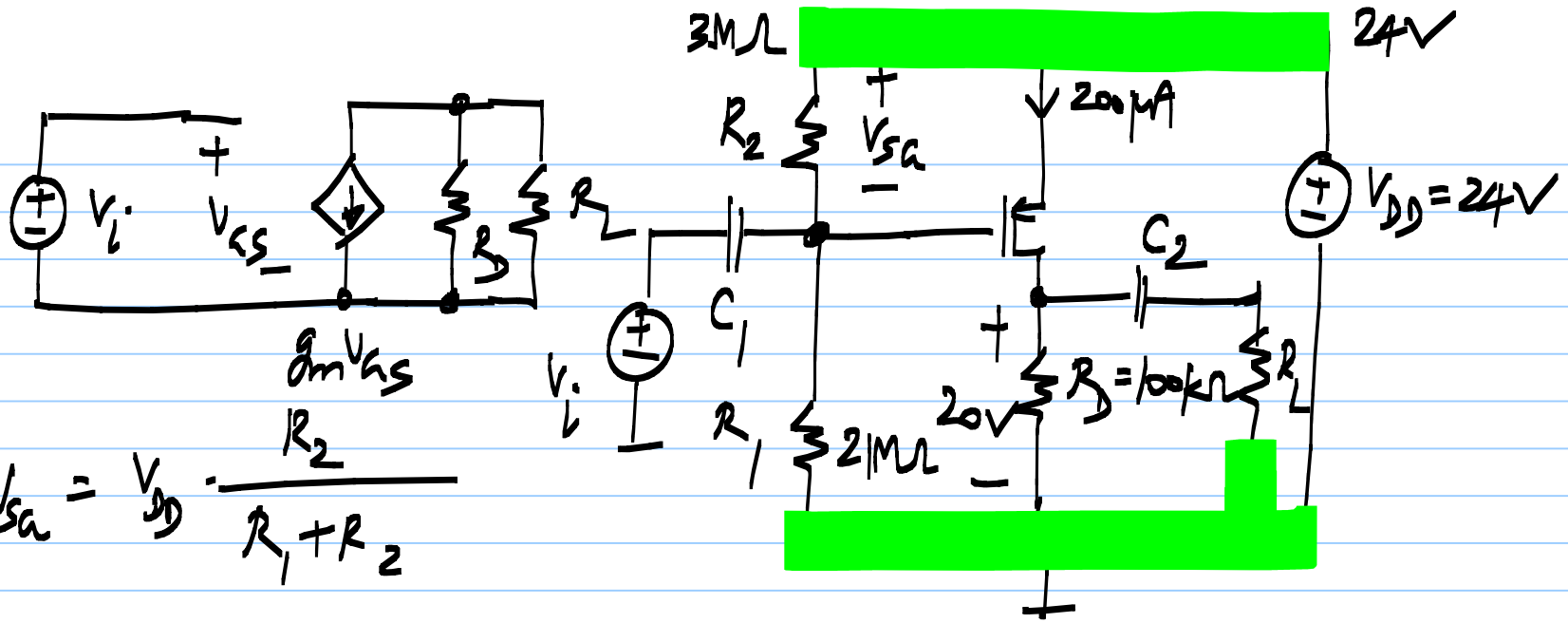




$\mu_p C_{ox} = 25\mu A/V^2, \quad \frac{W}{L} = 4$

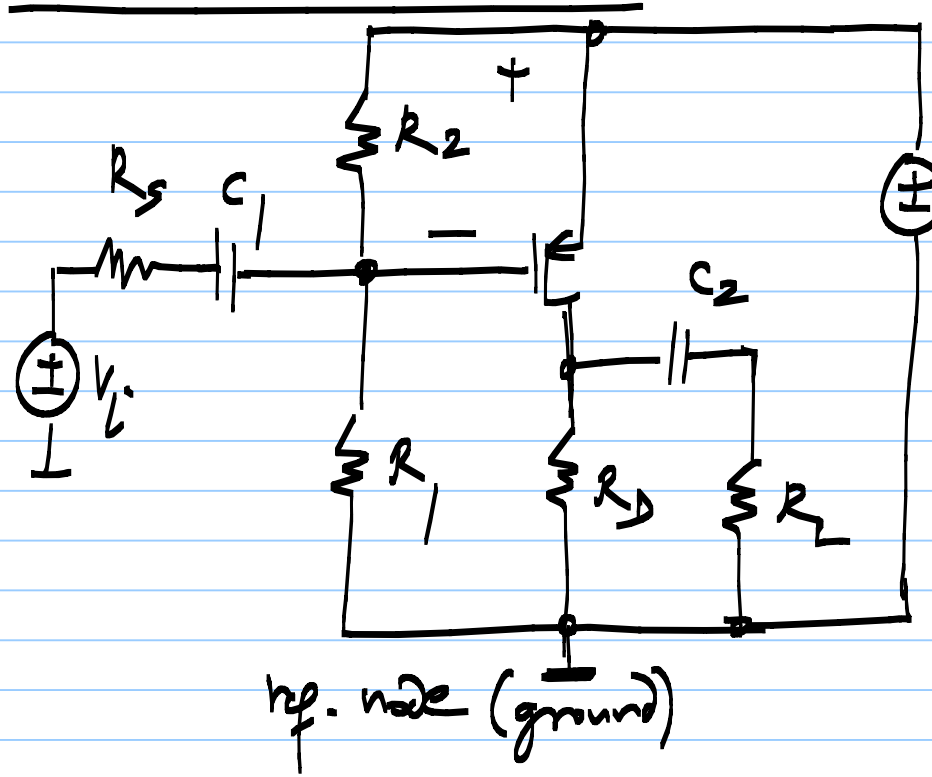
$\mu_p C_{ox} \frac{W}{L} = 100\mu A/V^2; \quad V_{Tp} = 1V$

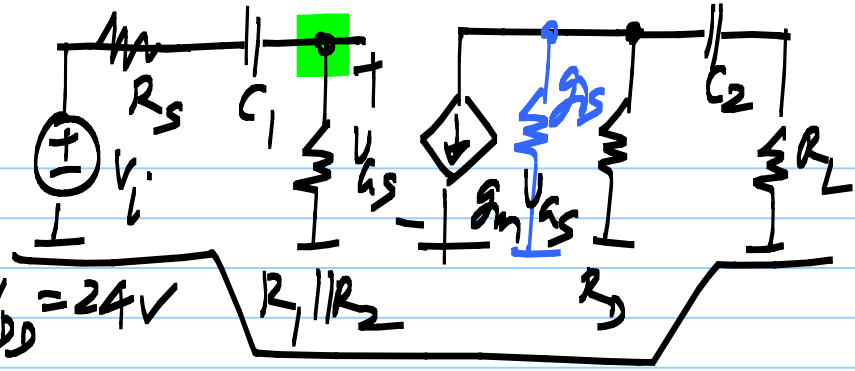
$K_n = 100\mu A/V^2$

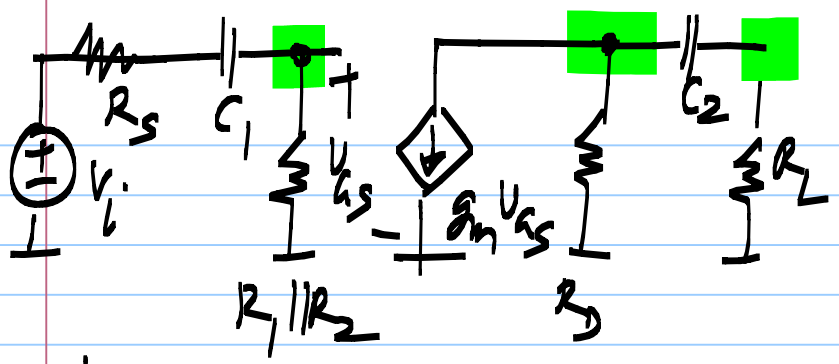


$$V_{GS} = V_{DD} \cdot \frac{R_2}{R_1 + R_2}$$

pMOS CS amplifier





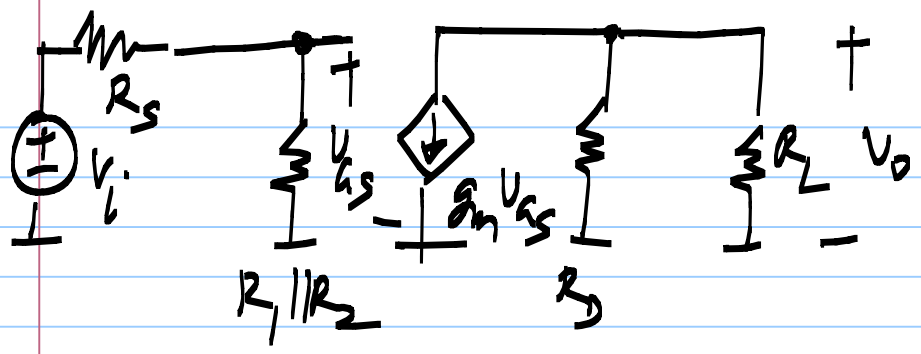


Small signal picture: exactly the same as nMOS CS amplifier

$$\frac{1}{\omega C_1} \ll R_s + R_1 \| R_2 \; ; \; C_1 \gg \frac{1}{\omega (R_s + R_1 \| R_2)}$$

$$\frac{1}{\omega C_2} \ll R_D + R_L \; ; \quad C_2 \gg \frac{1}{\omega (R_D + R_L)}$$

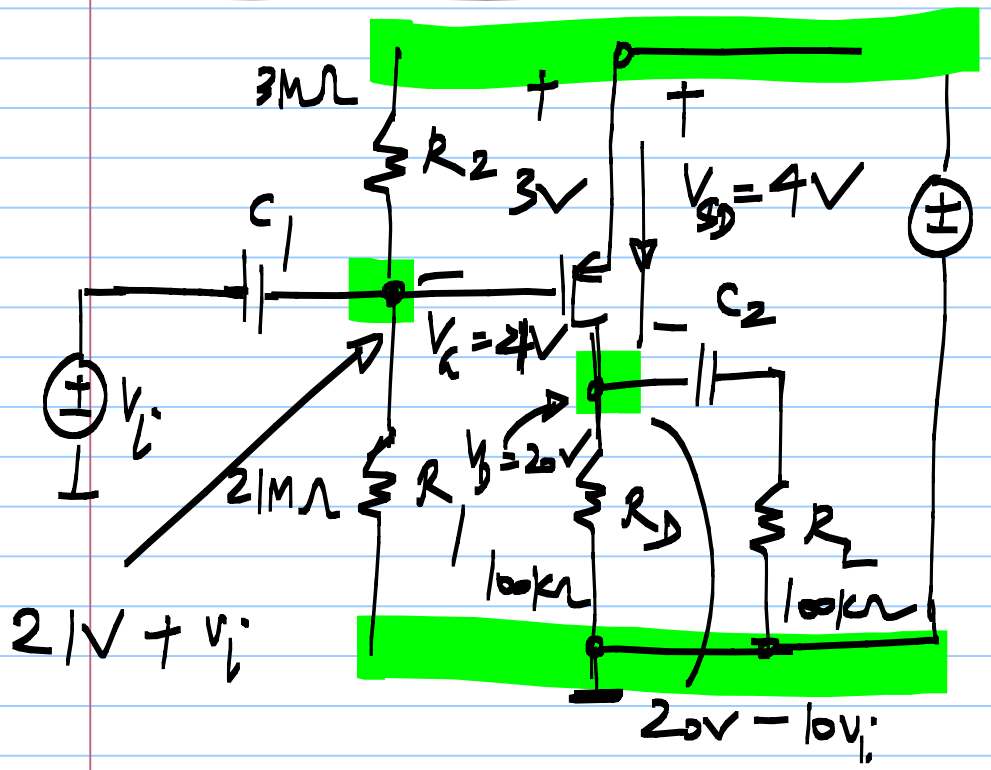
$$\frac{1}{\omega C_2} \ll R_L \; ; \quad C_2 \gg \frac{1}{\omega R_L}$$



$$\frac{v_o}{v_i} = -g_m (R_D \| R_L) \cdot \frac{R_1 \| R_2}{R_s + R_1 \| R_2}$$

$$R_1 \| R_2 \gg R_s \quad \simeq -g_m (R_D \| R_L)$$

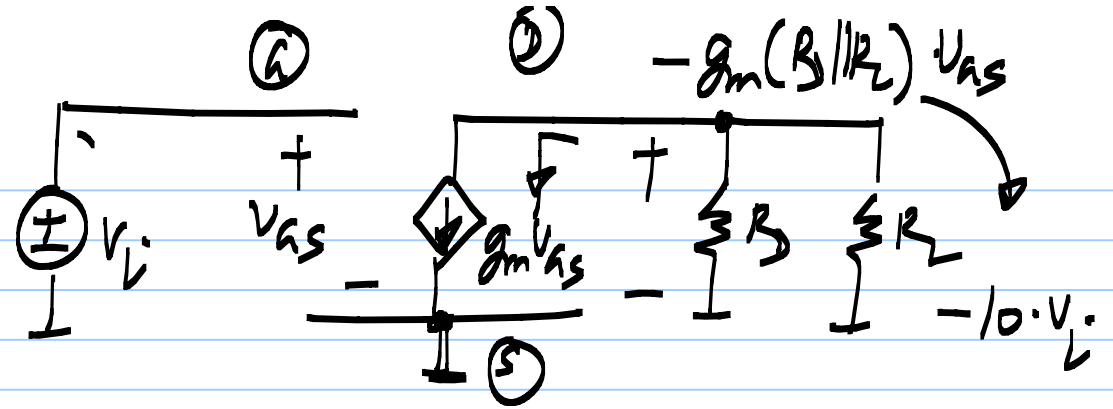
Swing limits of a pMOS CS amplifier



Saturation: $V_{SD,tot} \geq V_{SG,tot} - V_{TP}$

not. cutoff: $I_{D,tot} > 0$

	op point	total
	$V_{SG} = 3V$	$V_{SG,tot} = 3V - V_i$
	$V_{SD} = 4V$	$V_{SD,tot} = 4V + 10v_i$
	$I_D = 200\mu A$	$I_{D,tot} = 200\mu A - 200\mu S \cdot v_i$



$g_m = 200mS$

$R_D = R_L = 100k\Omega$

Saturation: $V_{SD,M2} > V_{SG,M2} - V_{Tp}$

$4V + 10v_i > 3V - v_i - 1V$

$V_{SD,Q} + g_m(R_D \| R_L)\, v_i > V_{SG,Q} - v_i - V_{Tp}$

$\| v_i \geq 3V - 1V - 4V = -2V$

$v_i \geq \frac{-2}{\|} V$

$$v_i \geq \frac{V_{SG,Q} - V_{SD,Q} - V_{Tp}}{1 + g_m(R_D \| R_L)}$$

Cutoff: $I_{D,NZ} \geq 0$

$200\mu A - 200\mu S \cdot v_i \geq 0$

$v_i \leq 1V$

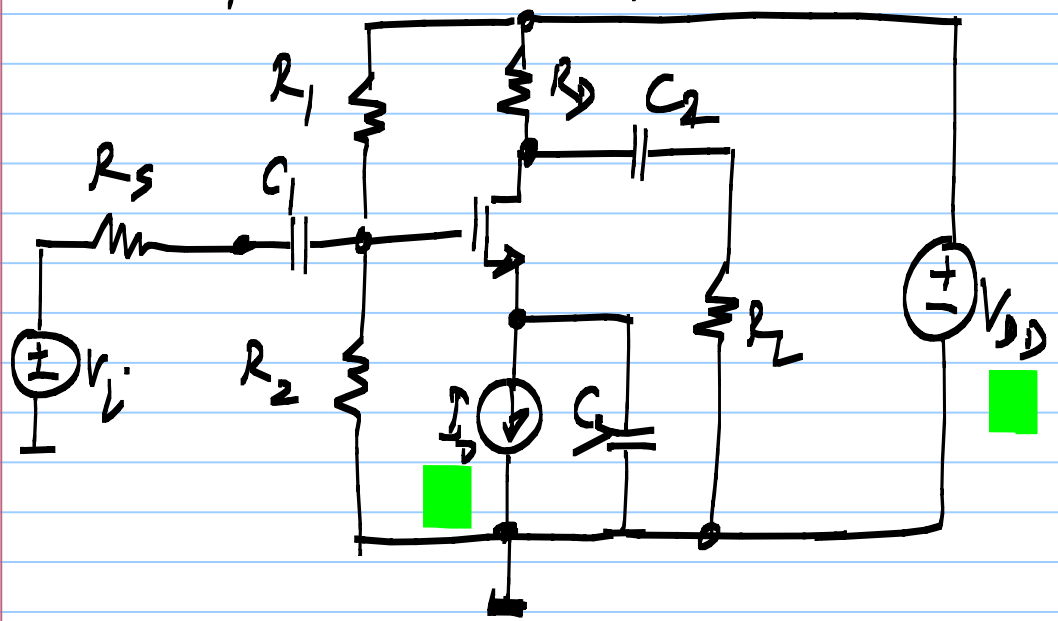
v_i

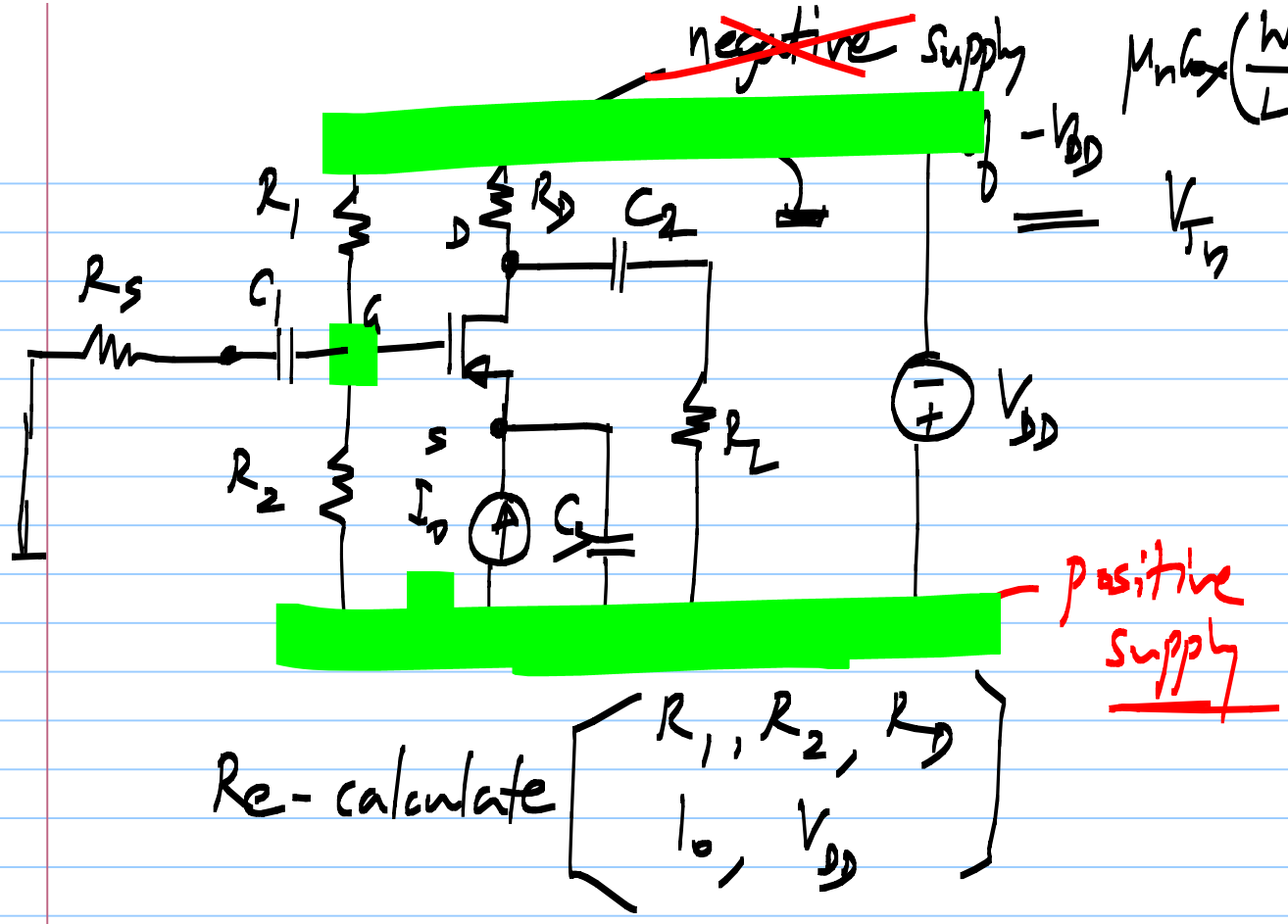
$I_{D,Q} - g_m \cdot v_{GS} \geq 0$

$v_i \leq \frac{I_{D,M}}{g_m}$

Converting nMOS circuits to pMOS

CS amp. with source feedback bias

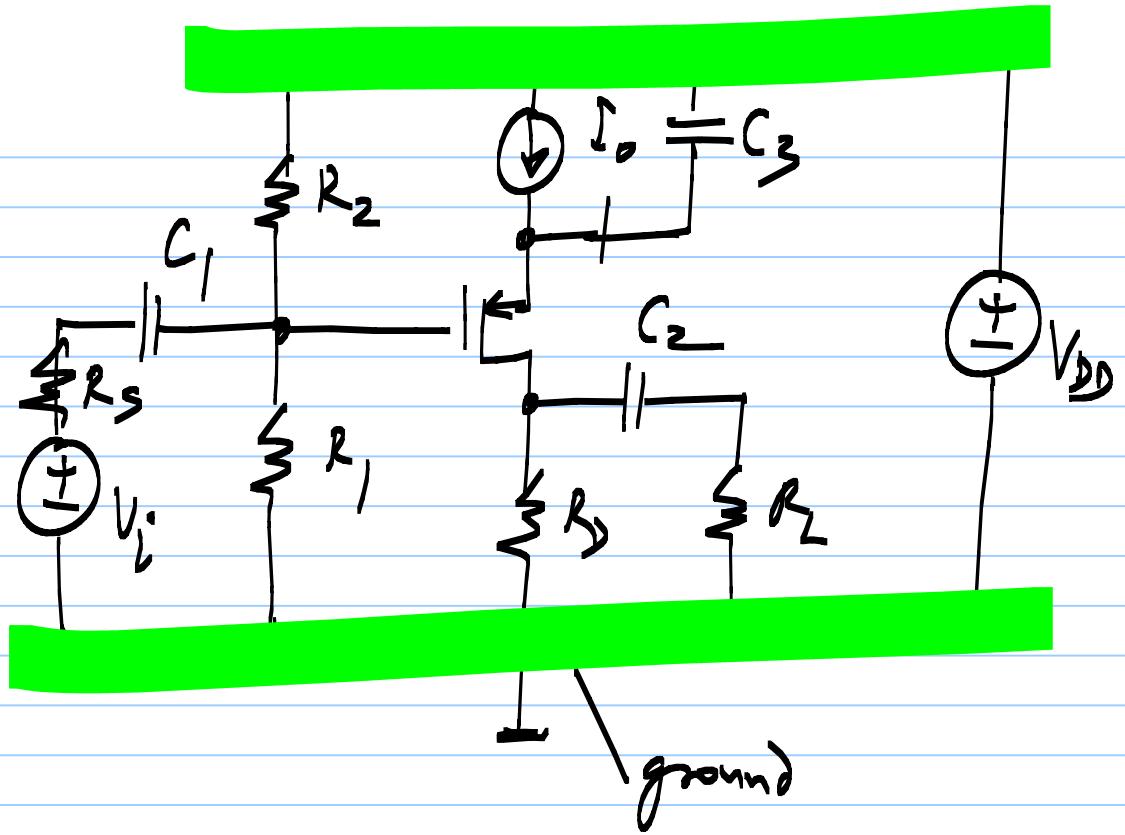




$$\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \mu_p C_{ox}\left(\frac{W}{L}\right)_p$$

$$|V_{Tn}| = |V_{Tp}|$$

Re-calculate $\begin{bmatrix} R_1, R_2, R_D \\ I_D, V_{DD} \end{bmatrix}$


I_0
C_3
R_2
C_1
C_2
V_{DD}
R_S
R_1
V_i
R_3
R_L
ground

Converting nMOS circuits to pMOS

* Reverse the polarity of sources used to establish the op. point
* Substitute pMOS for nMOS
* To have a +ve supply change the ground (reference)
* Draw the circuit upside down

Input source & load are connected to the com. reference node

May have to re-calculate component values

Small signal behavior : same as nMOS

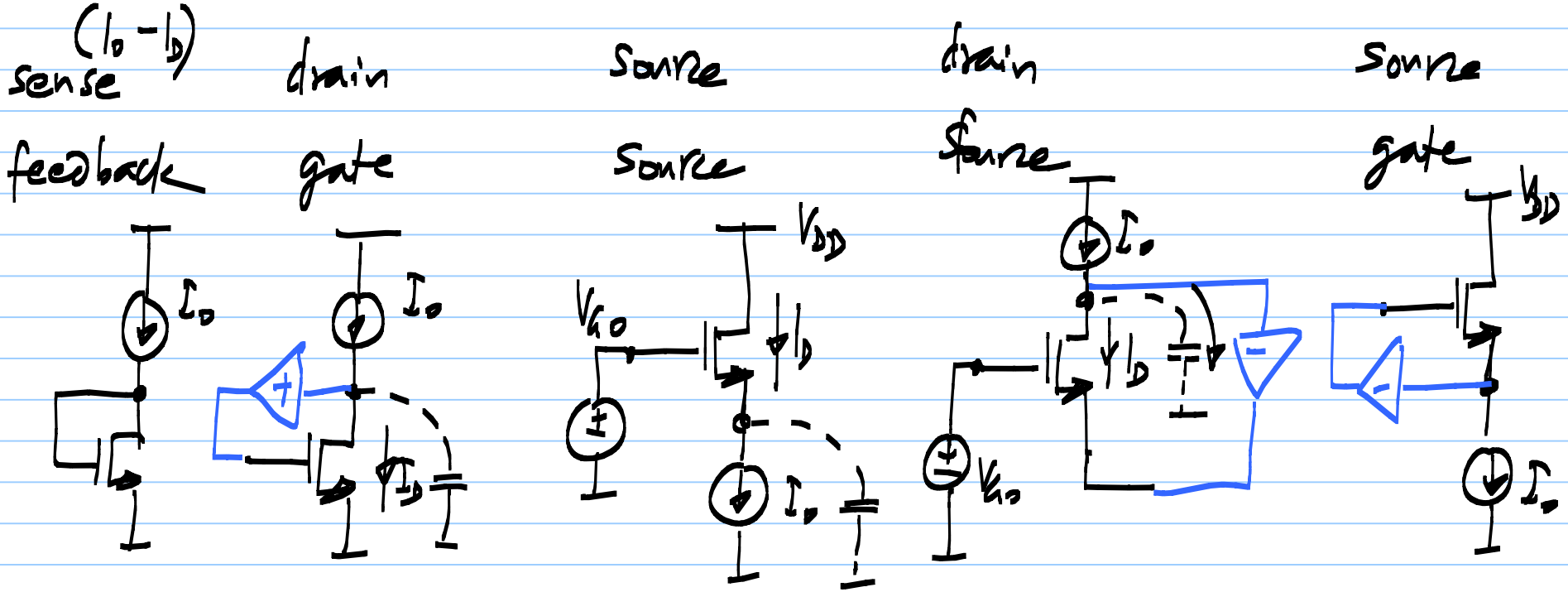
Large signal behaviour: Swing limits : opposite

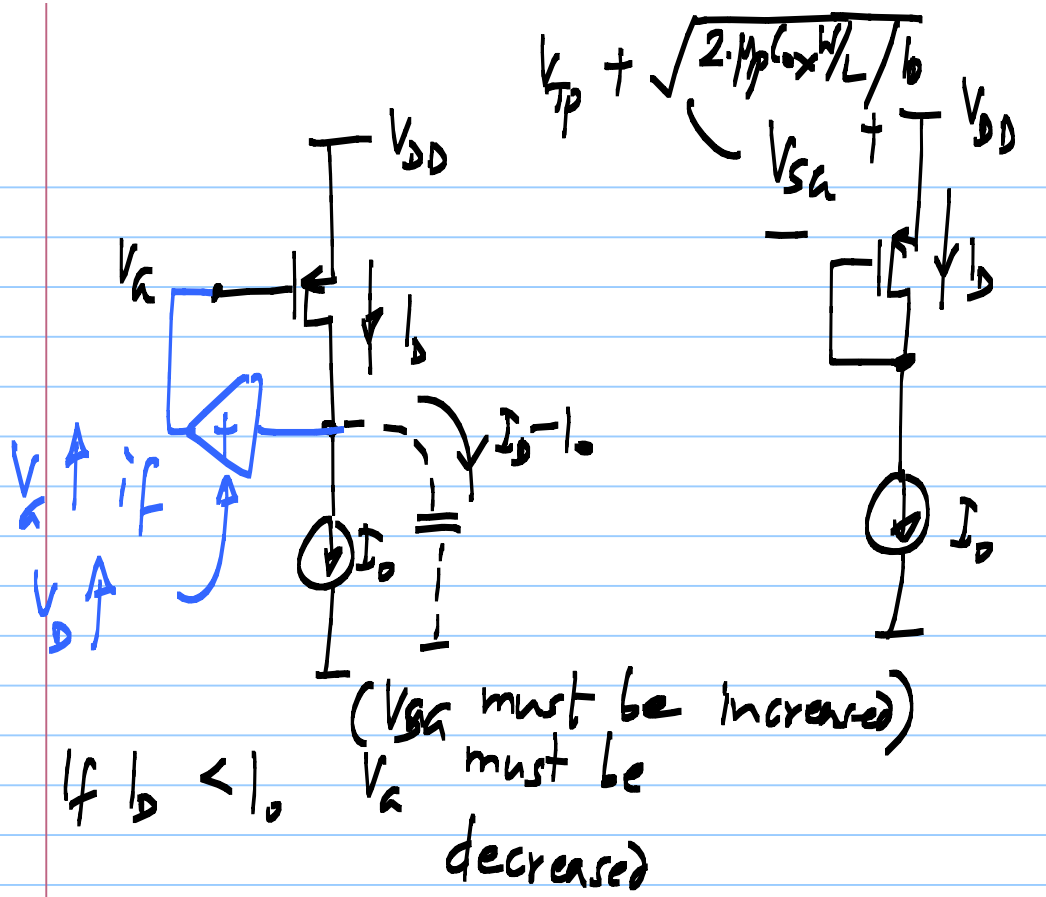
$$\mu_n C_{ox}\left(\frac{W}{L}\right)_n = \mu_p C_{ox}\left(\frac{W}{L}\right)_p \;;\; V_{tn} = V_{tp}$$

small signal parameters : same

$-2V \leq V_i \leq 0.5V$ $\qquad$ $-0.5V \leq V_i \leq 2V$

Biasing a pMOS transistor at a given current.



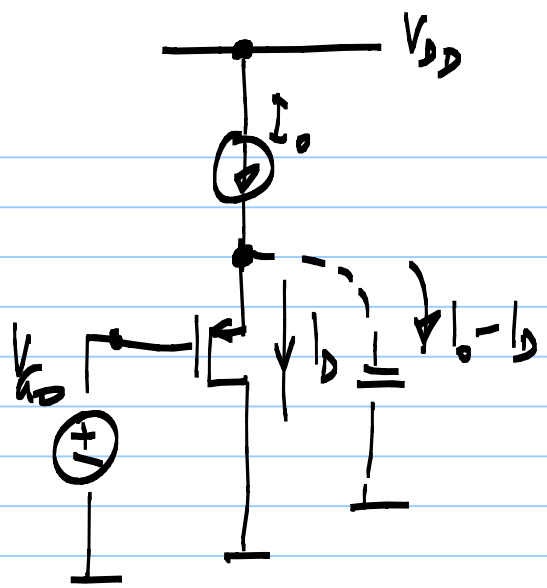


$V_{SD} > V_{SG} - V_{TP}$

saturation if $V_{TP} > 0$

(V_{SG} must be increased)

If $I_D < I_0$ V_G must be decreased



Sense @ source

fb to source

(source feedback bias)

$I_D < I_o \Rightarrow V_S \uparrow$

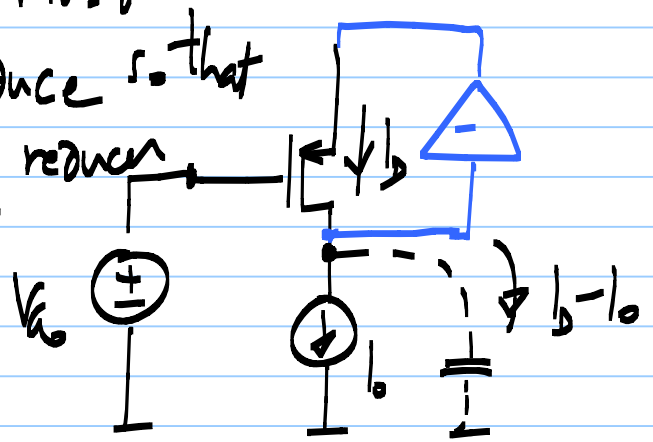
$\hookrightarrow V_{SG}$ must be $\uparrow$

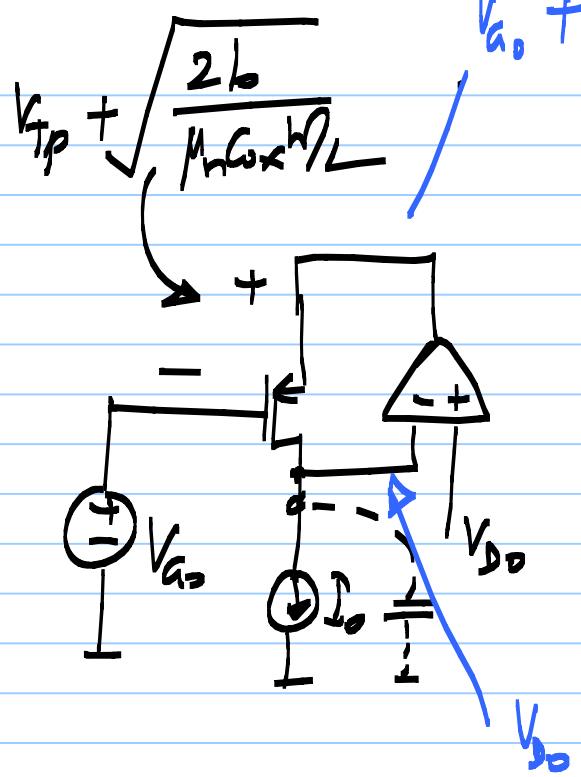
Sense @ drain

I_b to source

If $I_b > I_0$,

V_S must reduce so that V_{SG} reduces

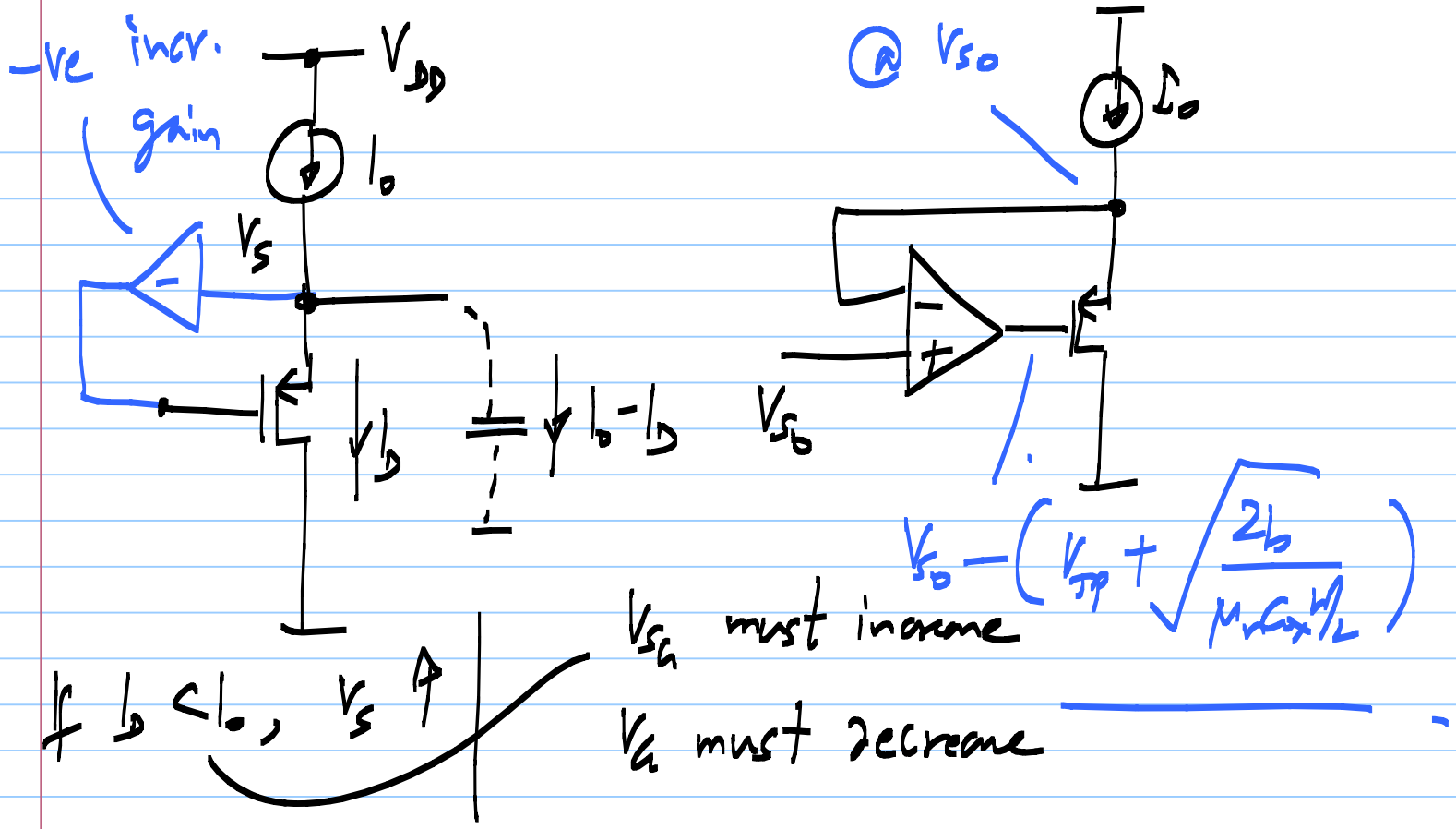




$V_{G0} + V_{Tp} + \sqrt{\frac{2I_0}{\mu_n C_{ox} W/L}}$

gate overdrive voltage

$(V_S - V_{Tn})$ $(V_{SG} - V_{Tp})$



$$V_{S0} = \left(V_{TP} + \sqrt{\frac{2I_D}{\mu_n C_{ox} W/L}} \right)$$

If $I_D < I_0$, V_S ↑

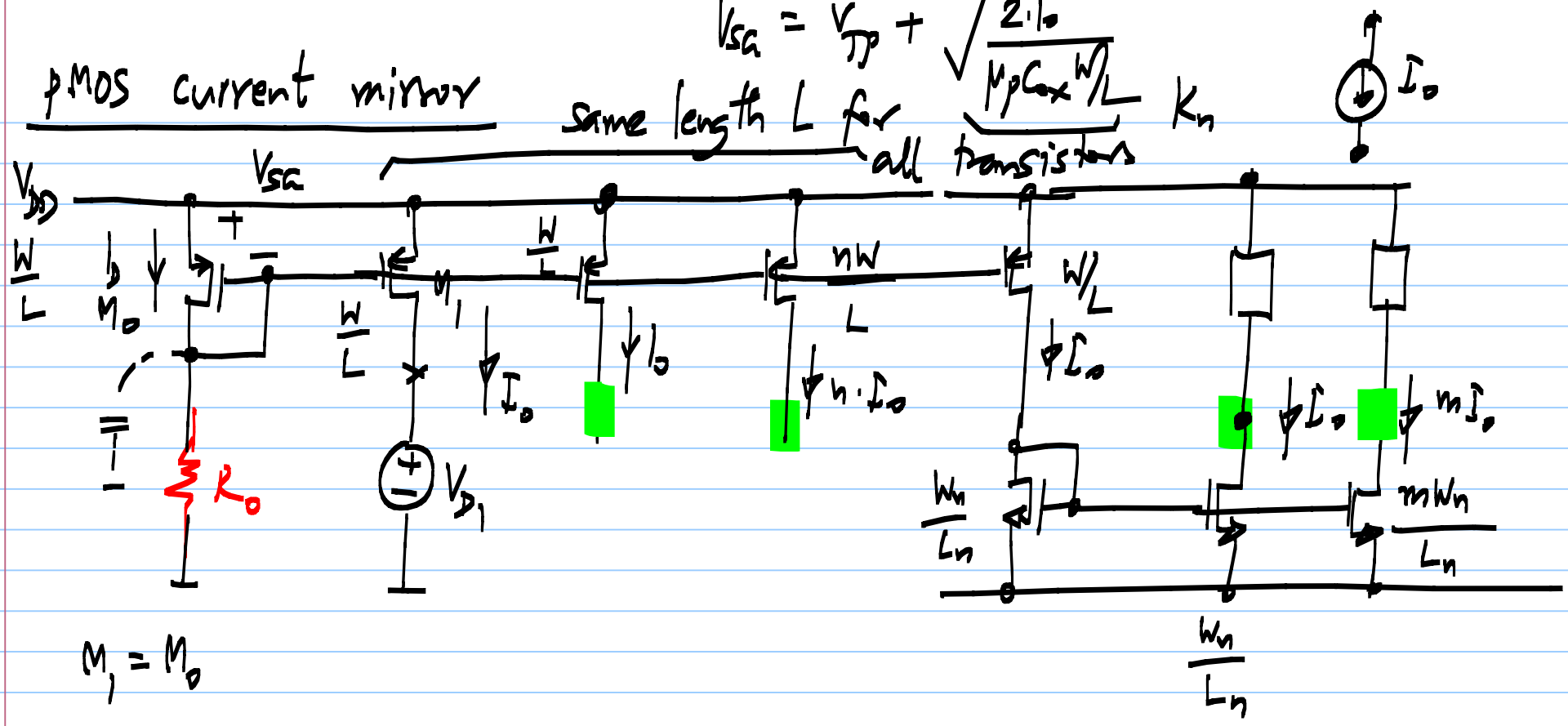
V_{SG} must increase

V_G must decrease

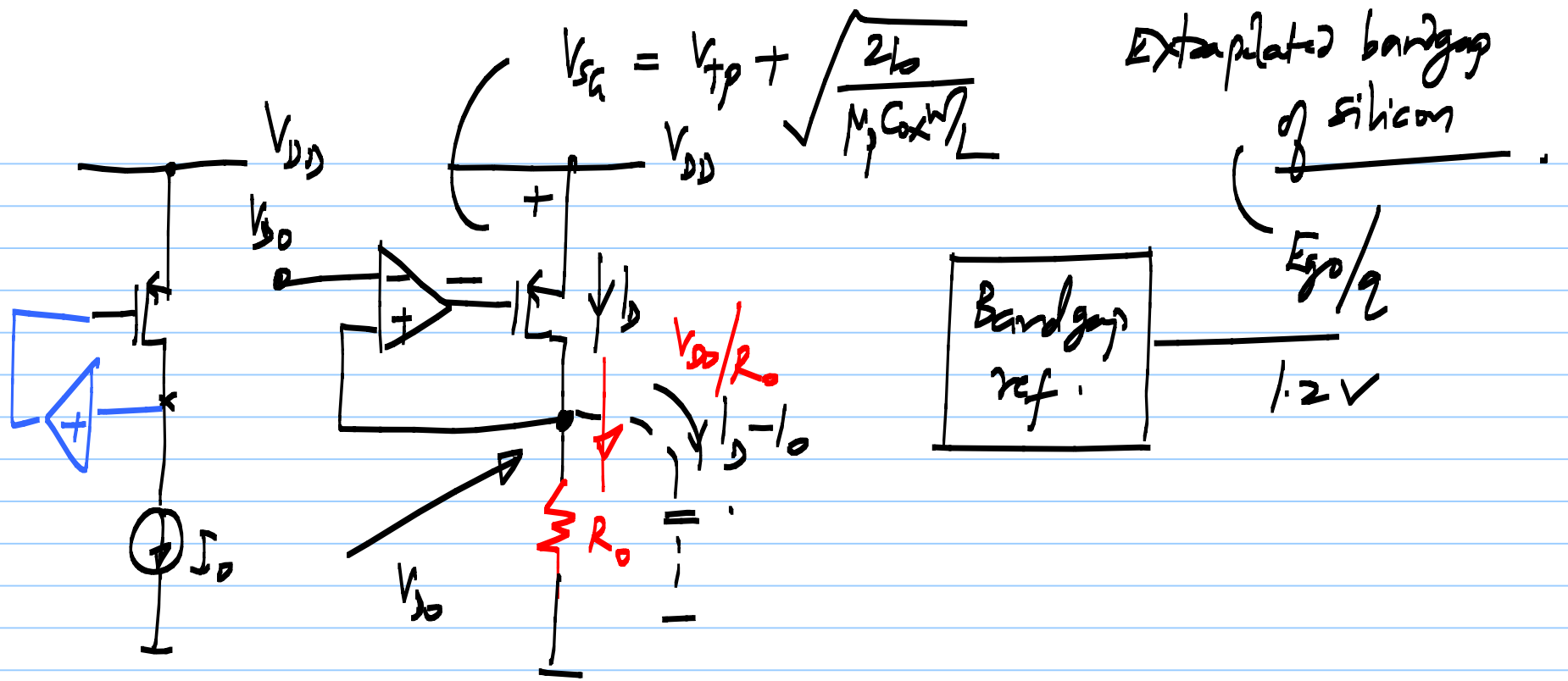
pMOS current mirror

$$V_{SG} = V_{TP} + \sqrt{\frac{2 \cdot I_0}{\mu_p C_{ox} \frac{W}{L}}} \qquad K_n$$

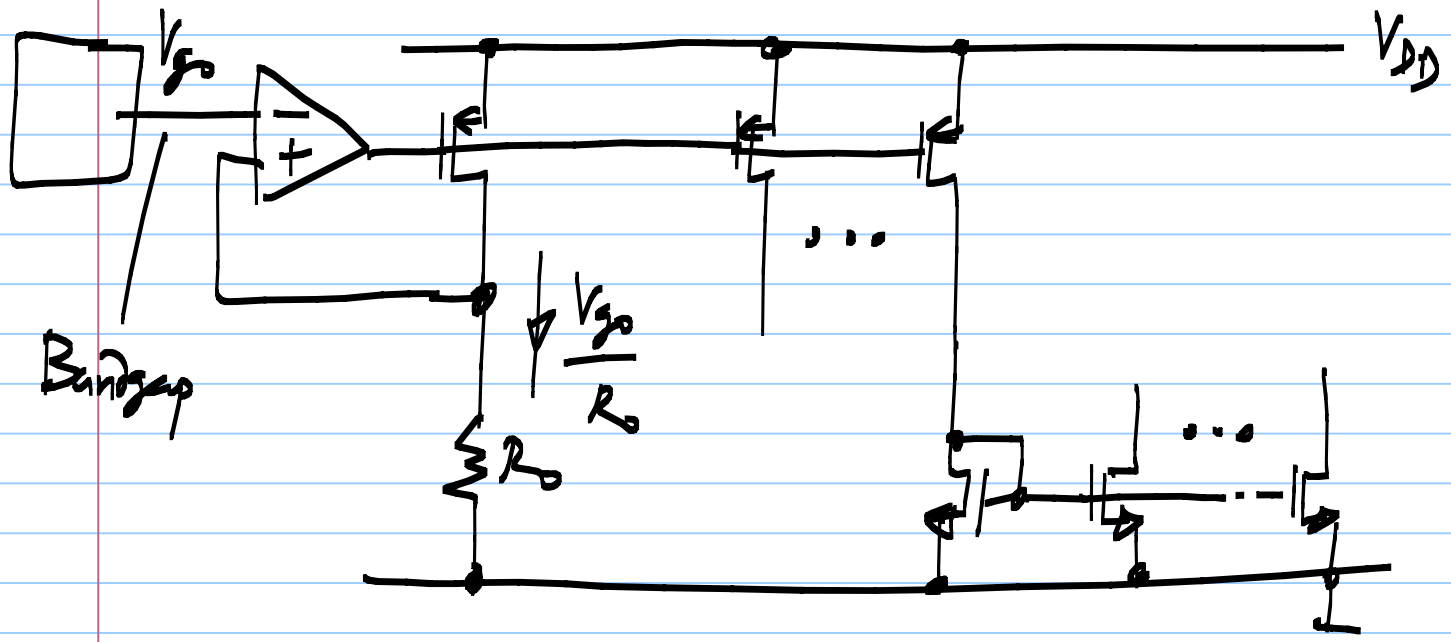
same length L for all transistors



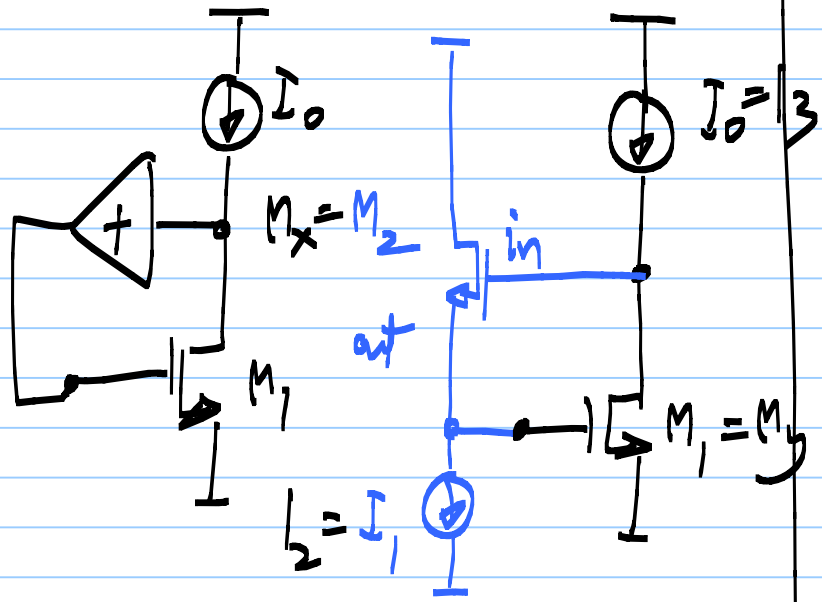
$M_1 = M_0$


$V_{SG} = V_{tp} + \sqrt{\frac{2I_D}{\mu_p C_{ox} W/L}}$
V_{DD}
V_{DD}
V_{bp}
V_{bn}
V_{bn}
I_D
V_{DD}/R_0
$I_D - I_0$
R_0
I_0
Extrapolated bandgap of silicon
E_{g0}/q
1.2 V
Bandgap ref.

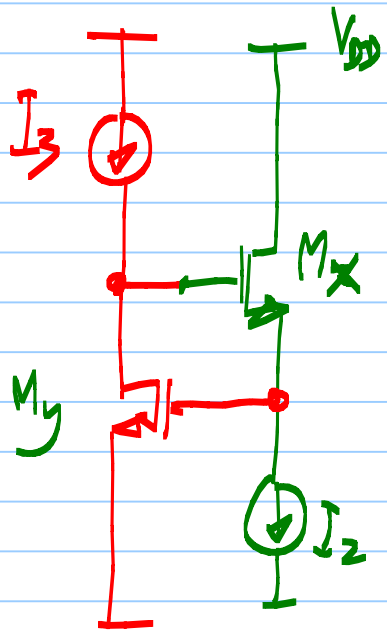
Bias current generation on an integrated circuit



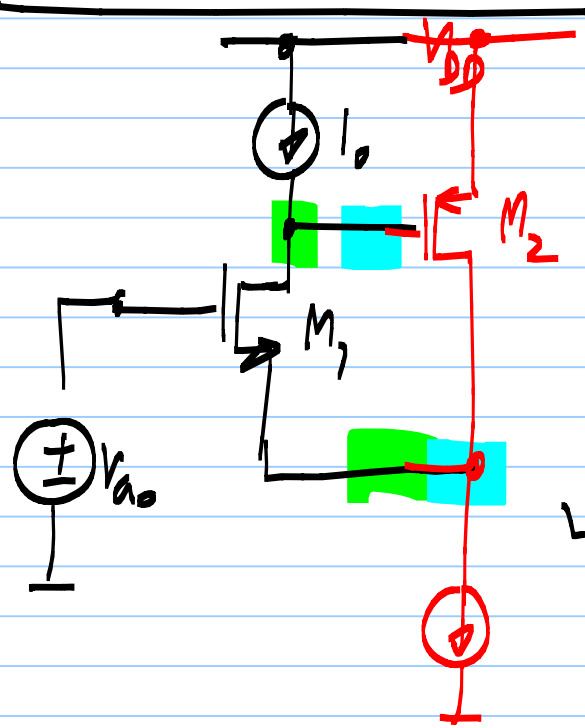
Drain feedback bias.



Sense @ Source, fb. to the gate



Sense @ drain, fb to source



Feedback around M_1 provided by M_2

from drain to source

CS amp.

Feedback around M_2 provided by M_1

from drain to gate

CG amplifier