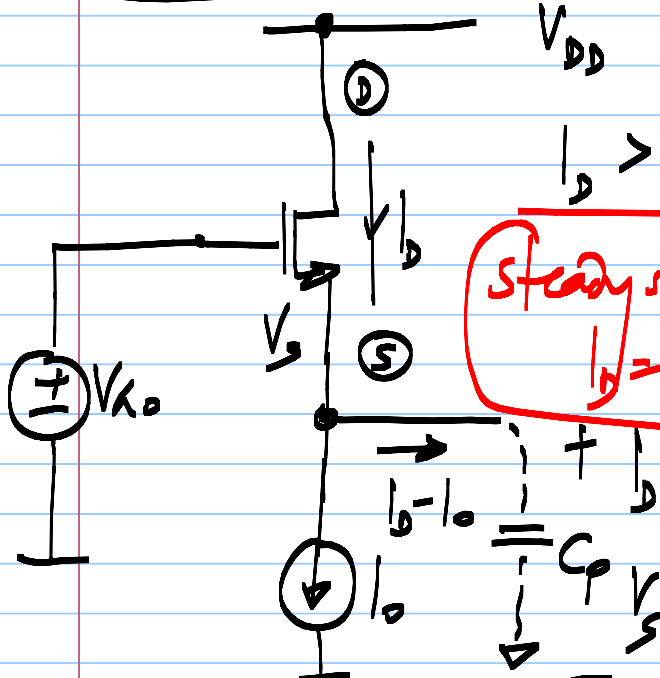
Biasing @ I_o: Sense at the source and feedback to the source



Want I_D to be equal to I_o

$I_D > I_o$: I_D must be reduced $\Rightarrow$

V_{GS} must be reduced $V_{GS} = V_{GO} - V_S$

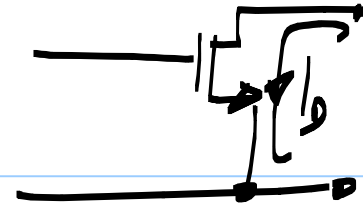
V_S must be increased

Steady state
$I_D = I_o$

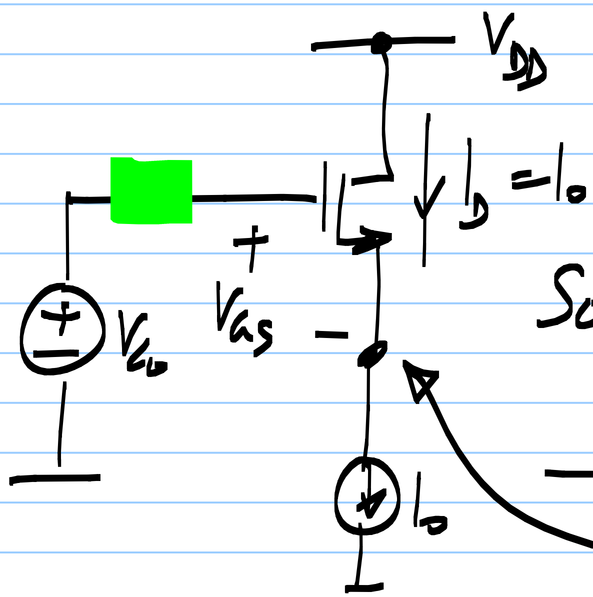
$I_D > I_o$: V_S increases

Because I_o is connected to the source of the transistor.

Controlling part: {gate, source}



Controlled part: {drain, source}



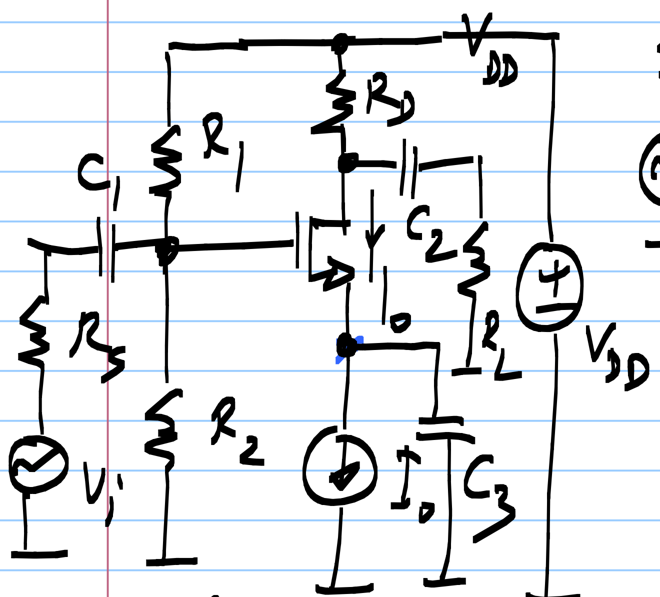
$$V_{GS}\Big|_{I_0} = V_T + \sqrt{\frac{2I_0}{\mu_n C_{ox} W/L}}$$

Source feedback bias

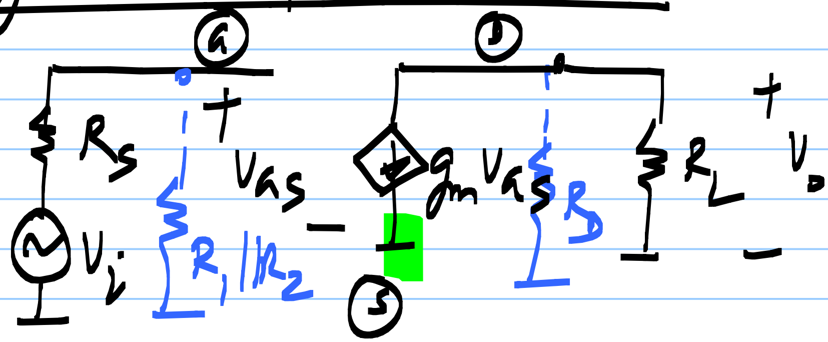
$$V_{G0} - V_T - \sqrt{\frac{2I_0}{\mu_n C_{ox} W/L}}$$

CS amplifier using source feedback bias

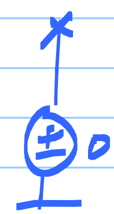
$$\frac{v_o}{v_i} = -g_m R_L$$

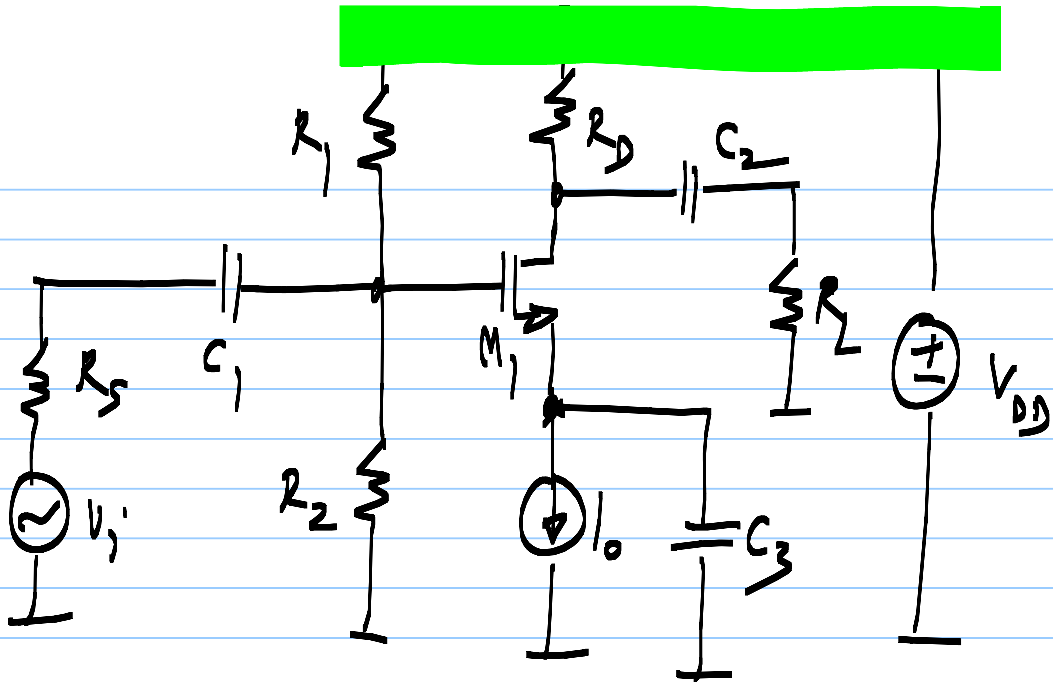


$$V_{DD}\frac{R_2}{R_1+R_2}$$

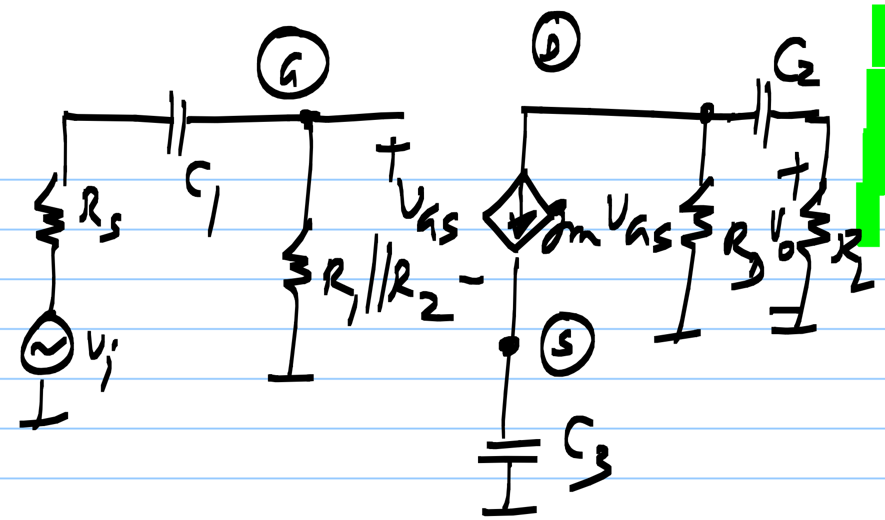


"Applying a zero signal"

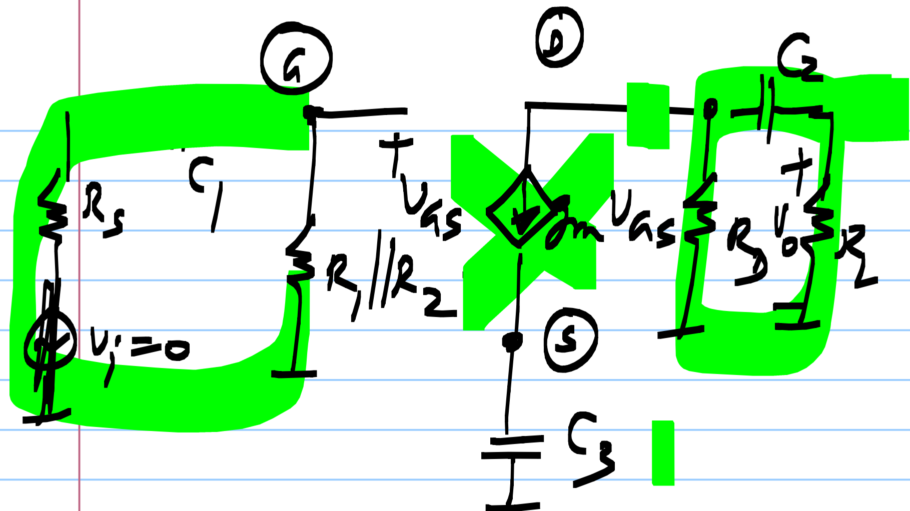




R_1
R_D
C_2
R_L
V_{DD}
C_1
R_S
v_i'
M_1
R_2
I_0
C_3

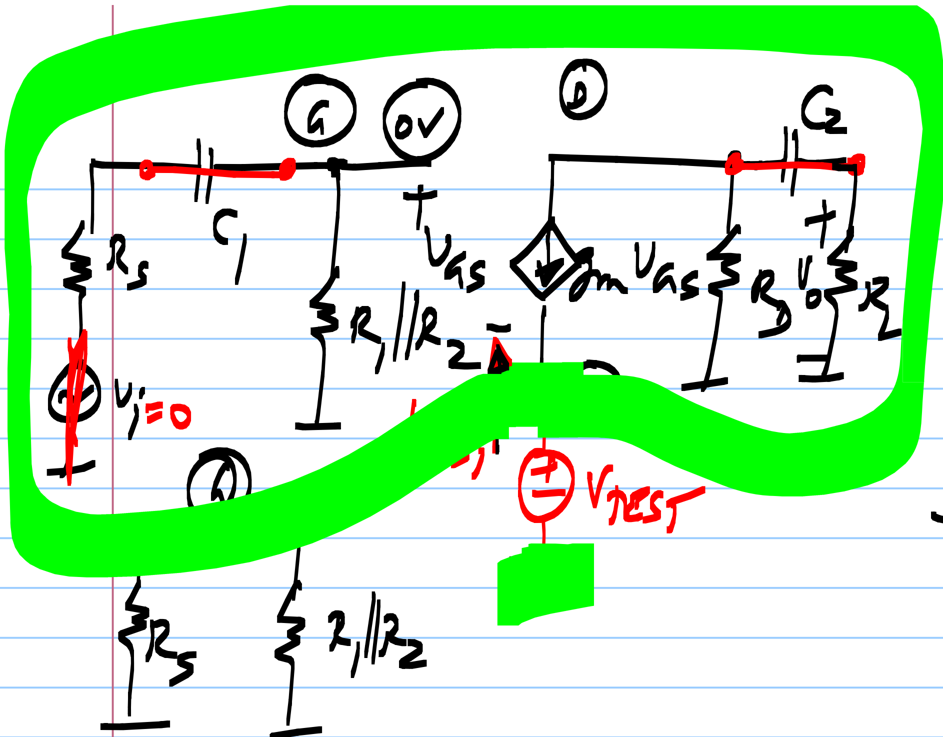


G
D
C_2
C_1
R_S
v_{GS}
$g_m v_{GS}$
R_D
v_o
R_L
$R_1 || R_2$
S
C_3
v_i



$$\frac{1}{\omega C_1} \ll R_s + (R_1 \| R_2)$$

$$\left.\frac{1}{\omega C_2} \ll R_D + R_L\right] \quad \frac{1}{\omega C_2} \ll R_L$$



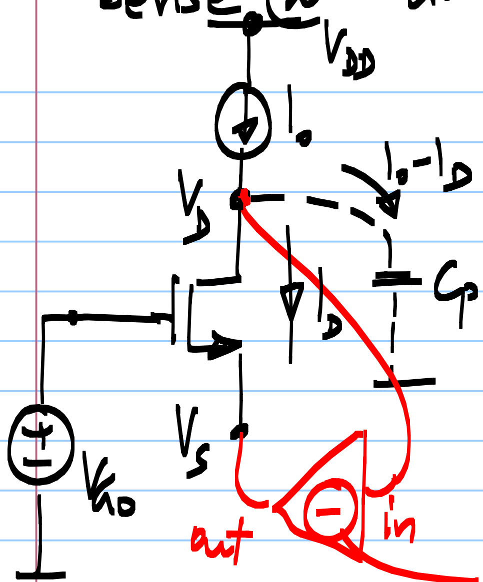
$$V_{GS} = -V_{TEST}$$

$$I_{TEST} = -g_m V_{GS} = g_m V_{TEST}$$

$$\frac{V_{TEST}}{I_{TEST}} = 1/g_m$$

$$\frac{1}{\omega C_3} \ll 1/g_m$$

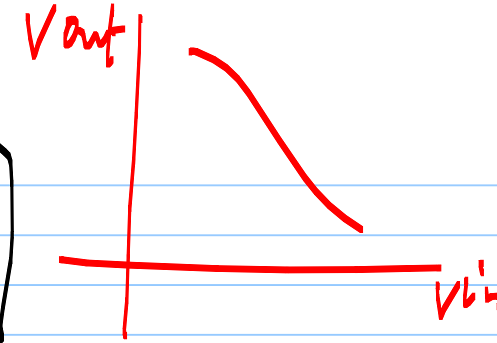
Sense @ drain, feedback to source



If $I_D > I_o$, we must reduce V_{GS}

$V_{GS} = V_{G0} - V_S \Rightarrow$ increase V_S

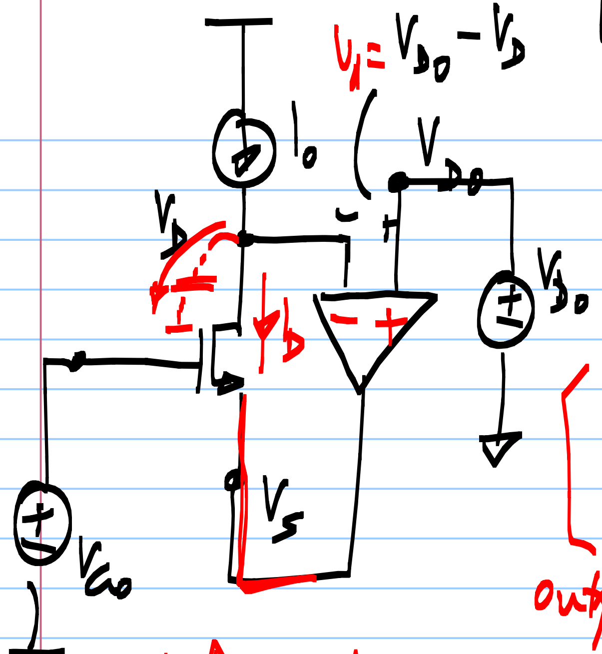
V_D reduces



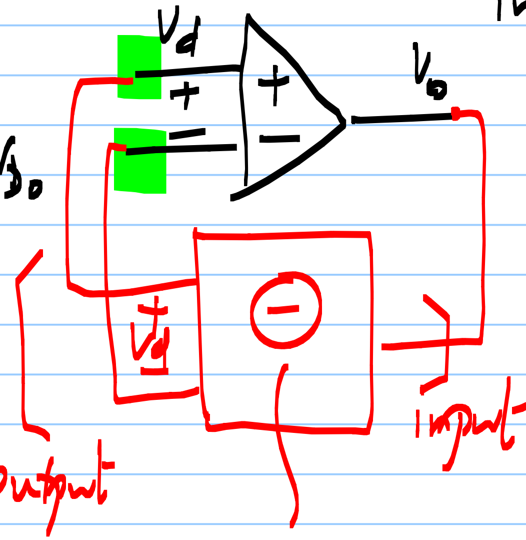
-negative incremental gain

If V_D reduces $\Rightarrow I_D > I_o \rightarrow V_S$ must increase

" increases $\Rightarrow I_D < I_o \Rightarrow$ " decrease



ideal opamp:



If the opamp is arranged to be in negative feedback, $v_d \to 0$

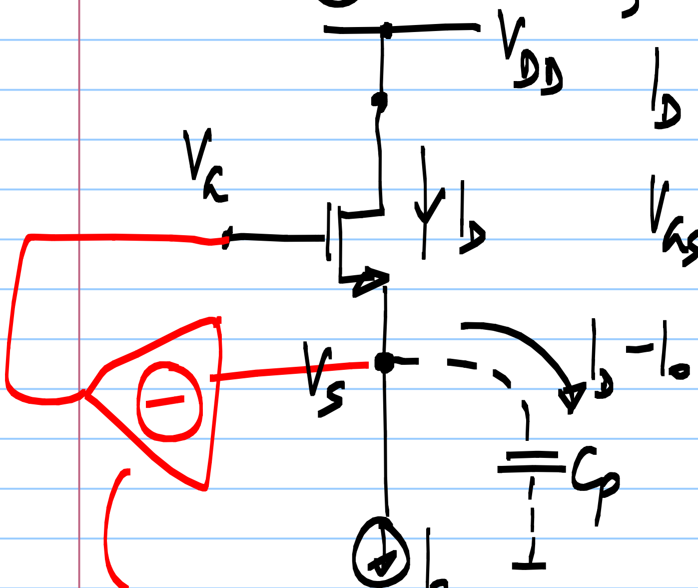
virtual short

$V_S \uparrow \Rightarrow I_D \downarrow \Rightarrow V_D \uparrow$

$v_d = V_{DO} - V_D \downarrow$

v_d reduces if v_o increases

Sense @ source, fb to gate



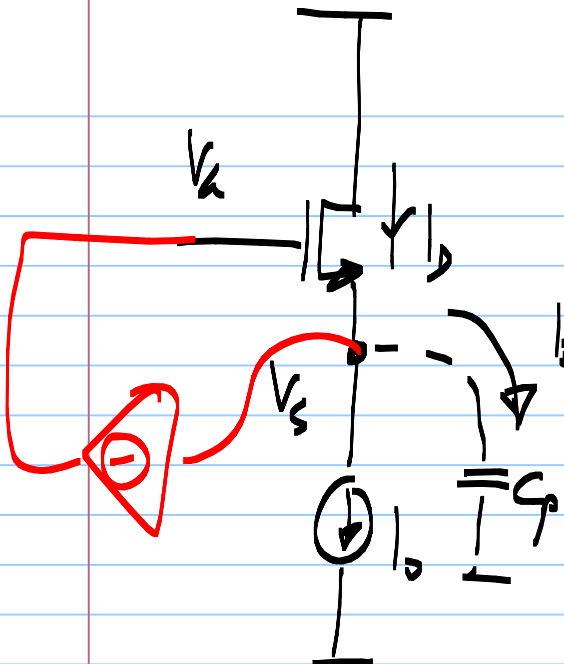
$I_D > I_o \Rightarrow V_{GS}$ must reduce

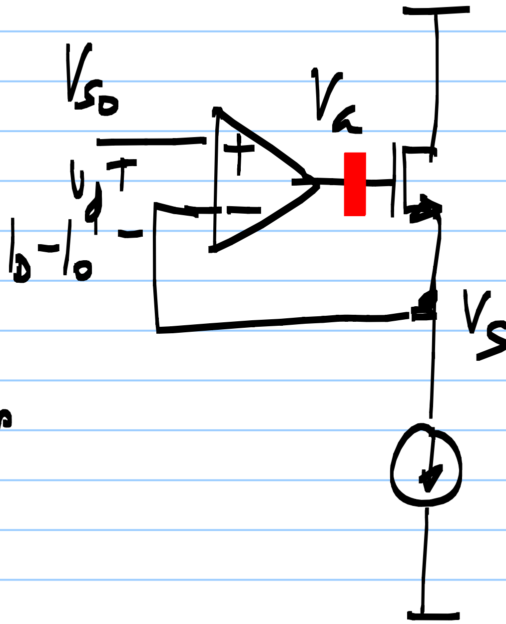
$V_{GS} = V_G - V_S \Rightarrow V_G$ must reduce

$I_D > I_o \Rightarrow V_S$ increases

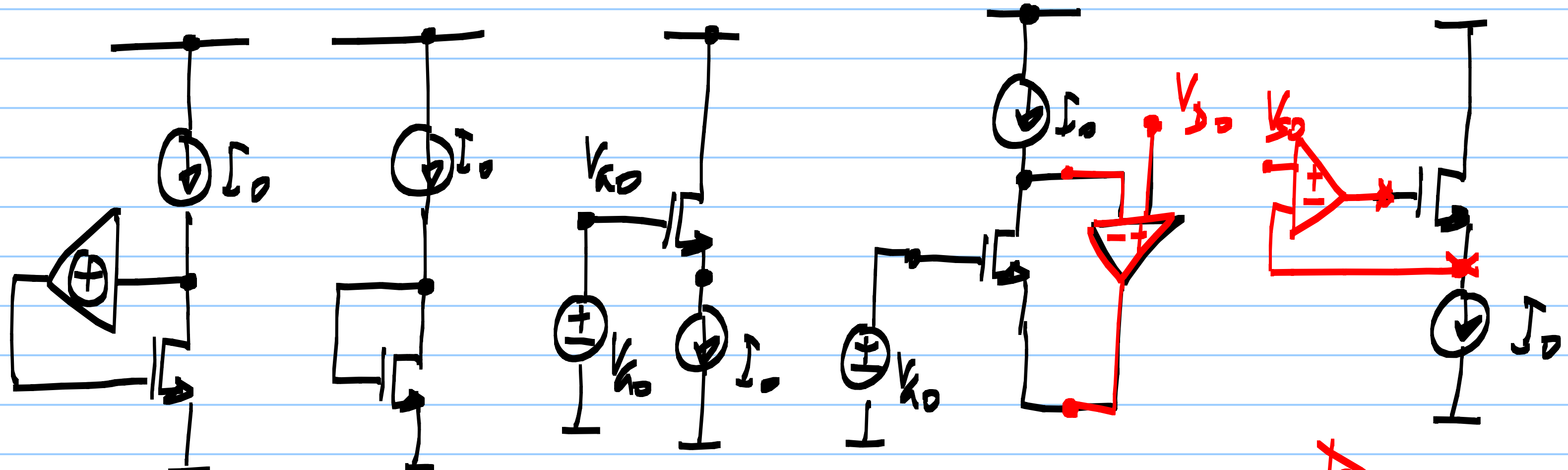
negative incremental gain

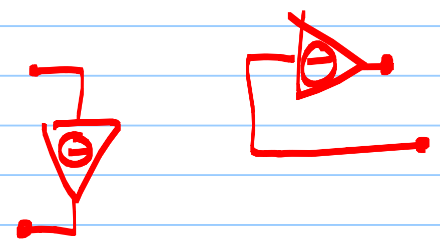
$I_D > I_0 \Rightarrow V_S \uparrow$





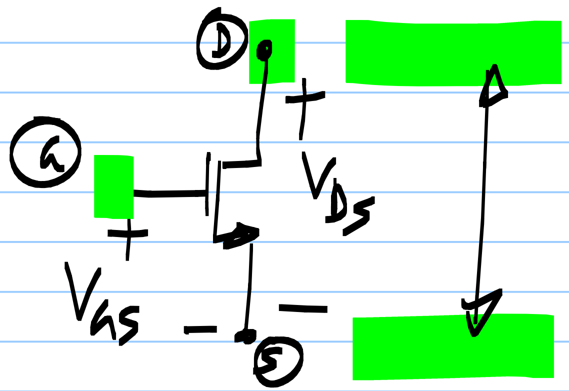
sense :	drain	source	drain	source
fb :	gate	source	source	gate





$$\underline{V_{DS} > V_{GS} - V_T}$$

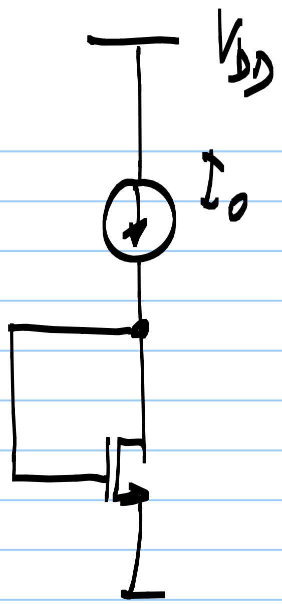
Saturation region

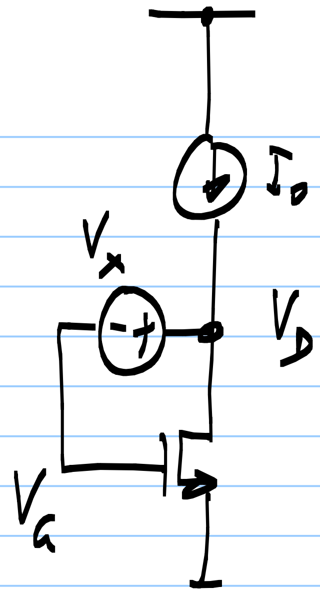


$V_{DS} > V_{GS} - V_T$; $V_D > V_G - V_T$

$V_G - 1V$ $\qquad$ $V_{GD} < V_T$

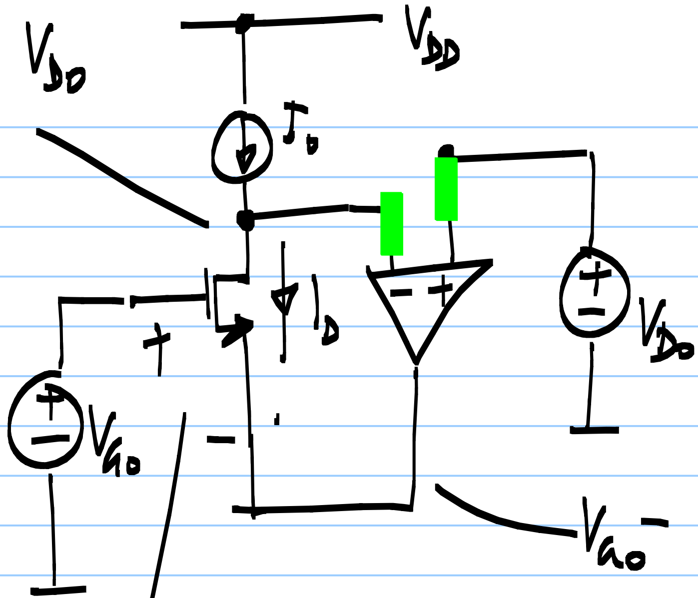
$V_D - \cancel{V_S} > V_G - \cancel{V_S} - V_T$ $\qquad$ $3V - 1V$





$$\left.\begin{aligned} V_D &= V_G + V_x \\ V_D &> V_G - V_T \end{aligned}\right] \quad \underline{V_x > -V_T}$$

$$V_{D0} > V_{G0} - V_T$$

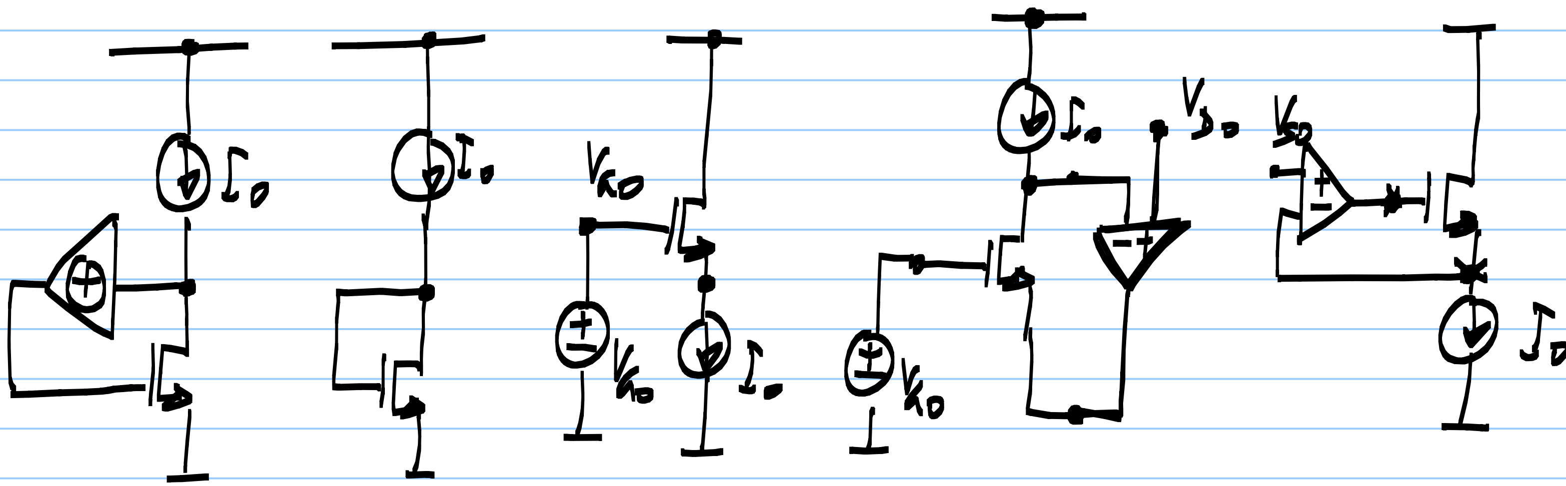


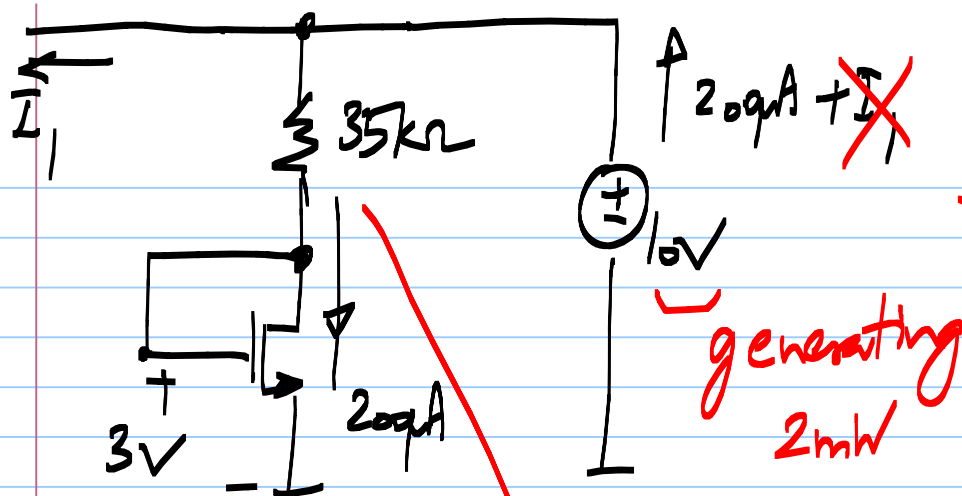
$$V_{G0} - V_T - \sqrt{\frac{2 \cdot I_D}{\mu_n C_{ox} W/L}}$$

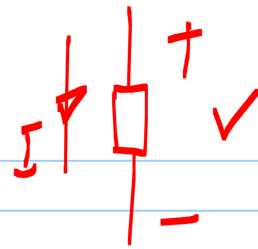
$$V_{GS} = V_T + \sqrt{\frac{2 \cdot I_D}{\mu_n C_{ox} W/L}}$$

sense : drain source drain source

fb : gate source source gate

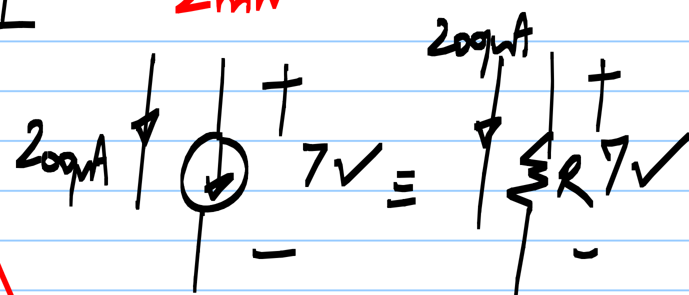






Power dissipated = $V \cdot I$

Substitution theorem



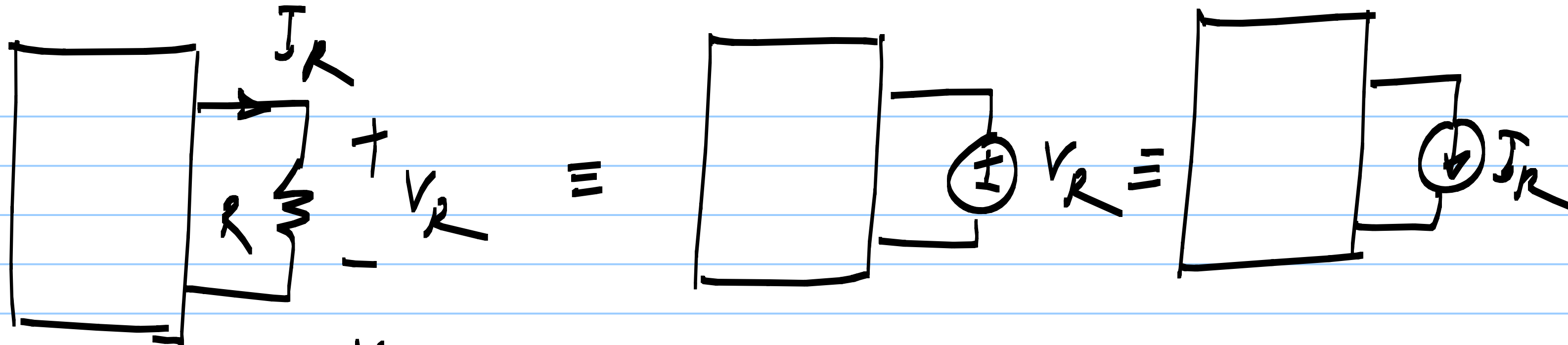
$\mu_n C_{ox} \frac{W}{L} = 100\mu A/V^2$

$V_T = 1V$

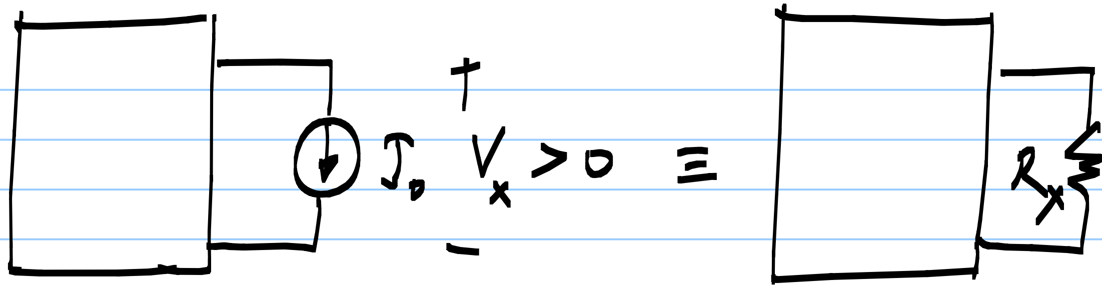
$V_{GS} = 3V$

dissipating 1.4mW

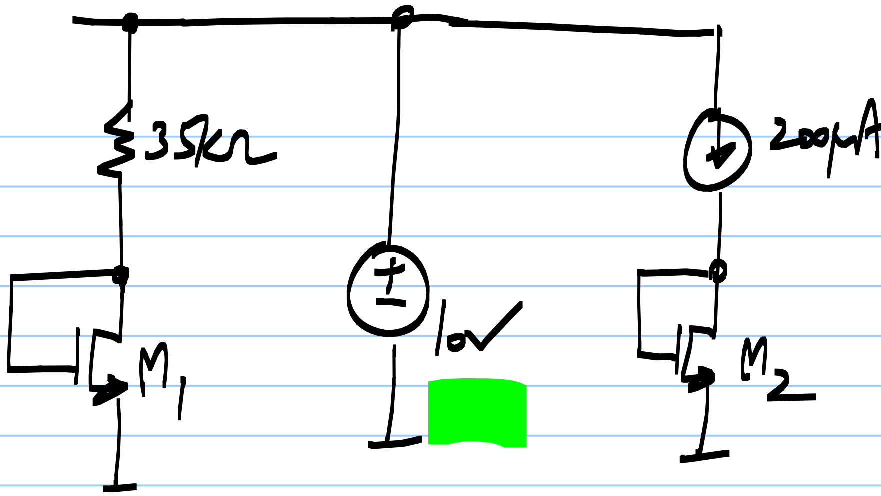
$R = \frac{7V}{200\mu A} = 35k\Omega$



$$R = \frac{V_R}{I_R}$$



$$R_x = \frac{V_x}{I_o}$$



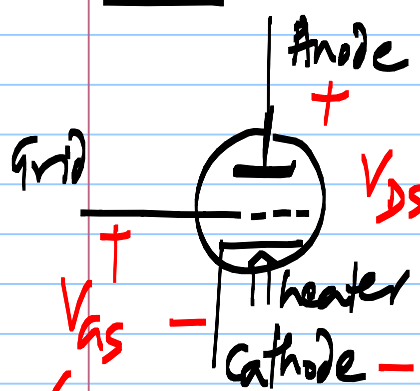
$V_T \uparrow$: M_2 : $I_D = 200\mu A$; $g_m = 200\mu S$

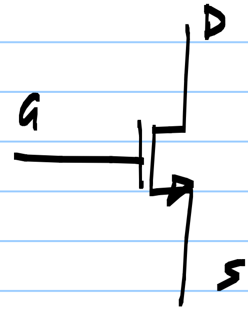
(no change)

$V_T \uparrow$: M_1 : $I_D \downarrow$; $g_m \downarrow$

Other electronic devices.

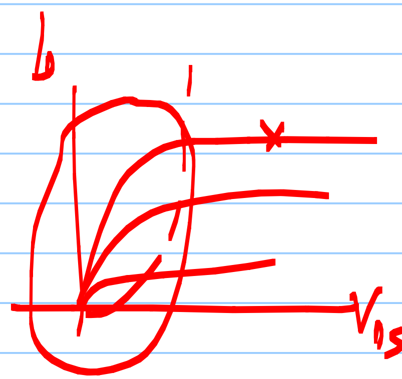
Triode (plate)





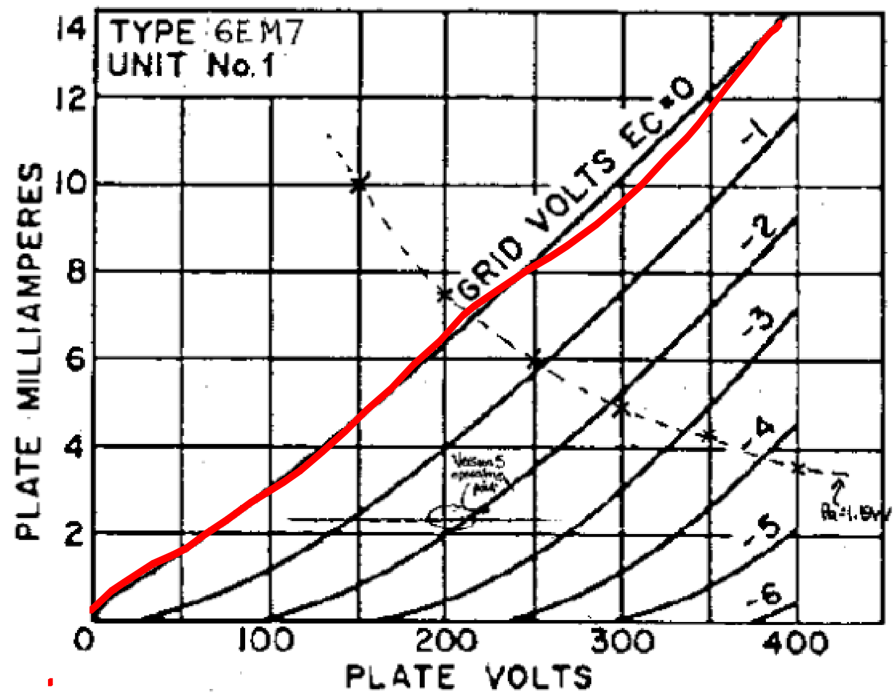
$V_{GS} < 0$

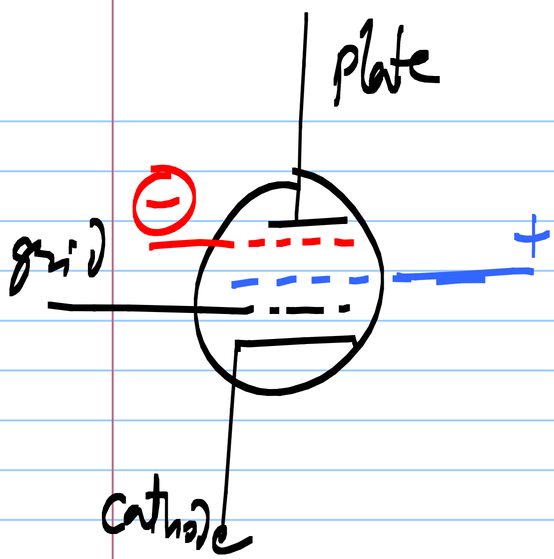
$V_{DS} \sim$ 100s of V



I_D V_G V_{DS}

Triode: I_{out} vs. V_{out}

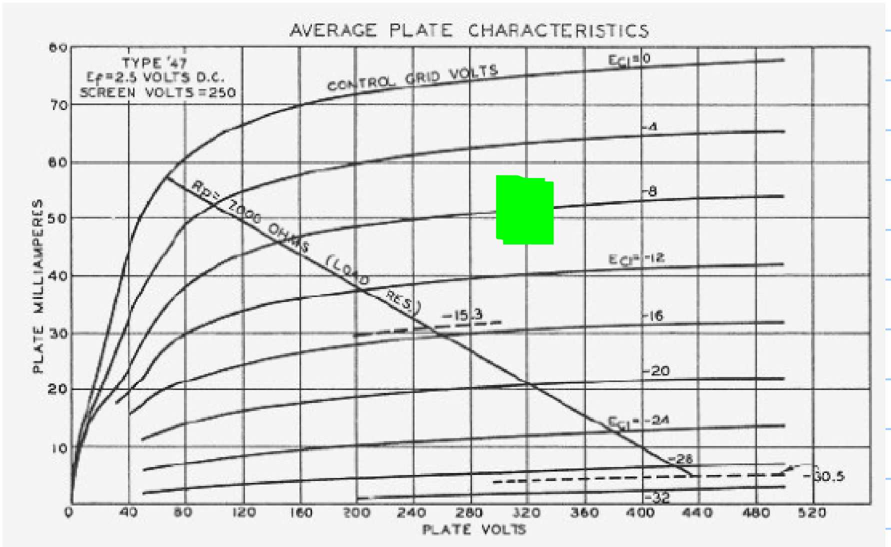


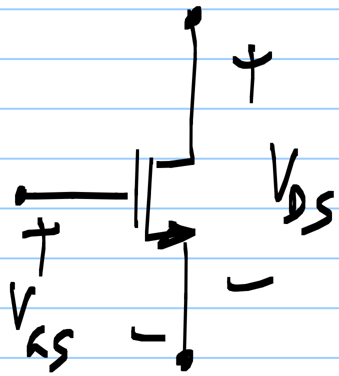


Tetrode

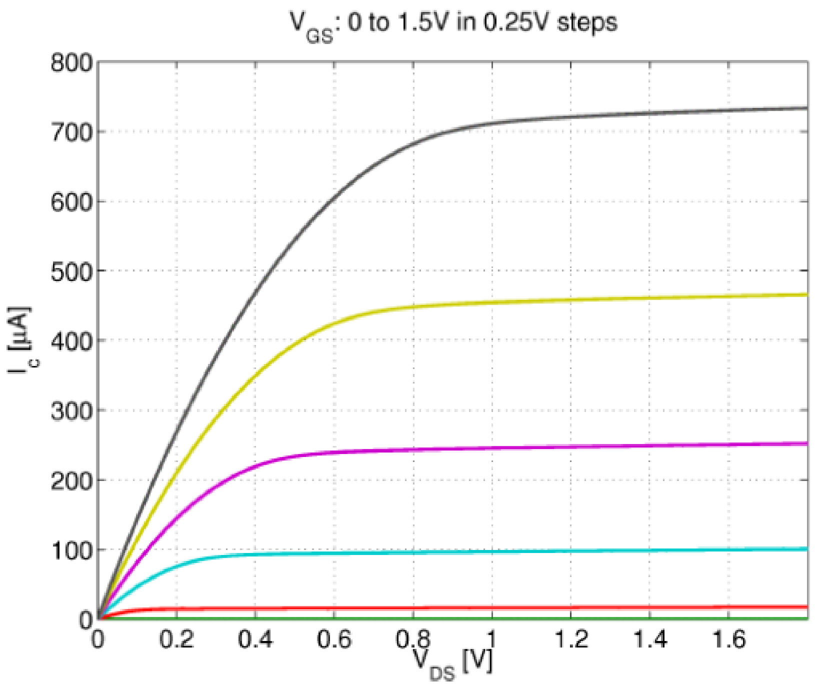
Pentode

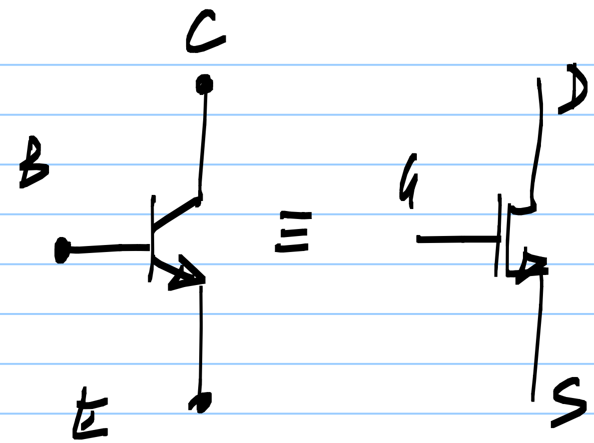
Pentode: I_{out} vs. V_{out}



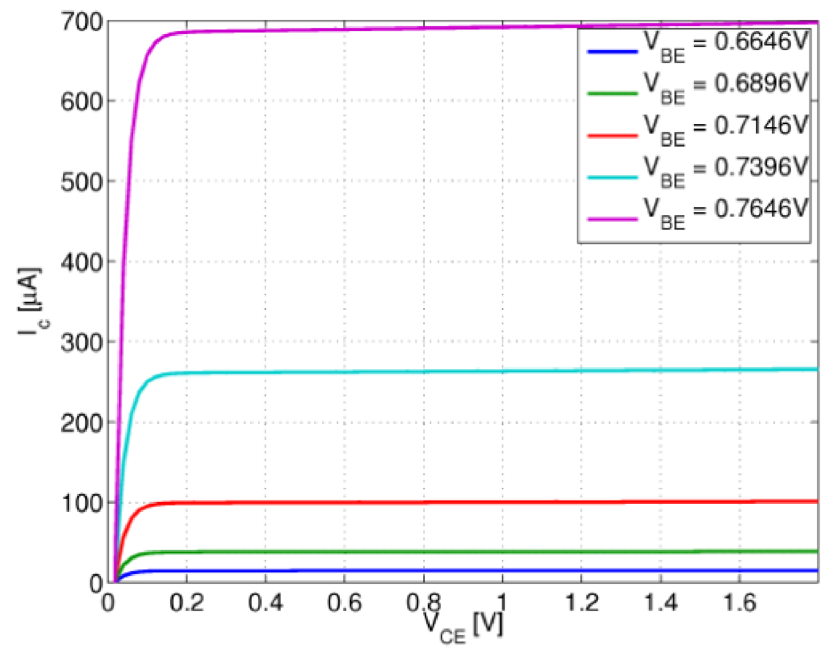


nMOS: I_{out} vs. V_{out}





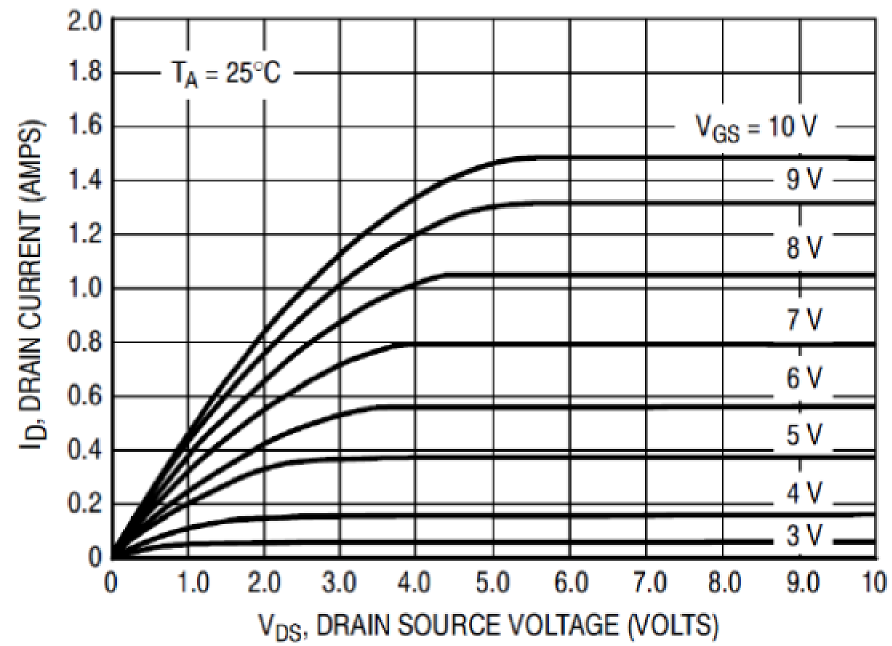
NPN: I_{out} vs. V_{out}



2N7000 (MOS): I_{out} vs. V_{out}

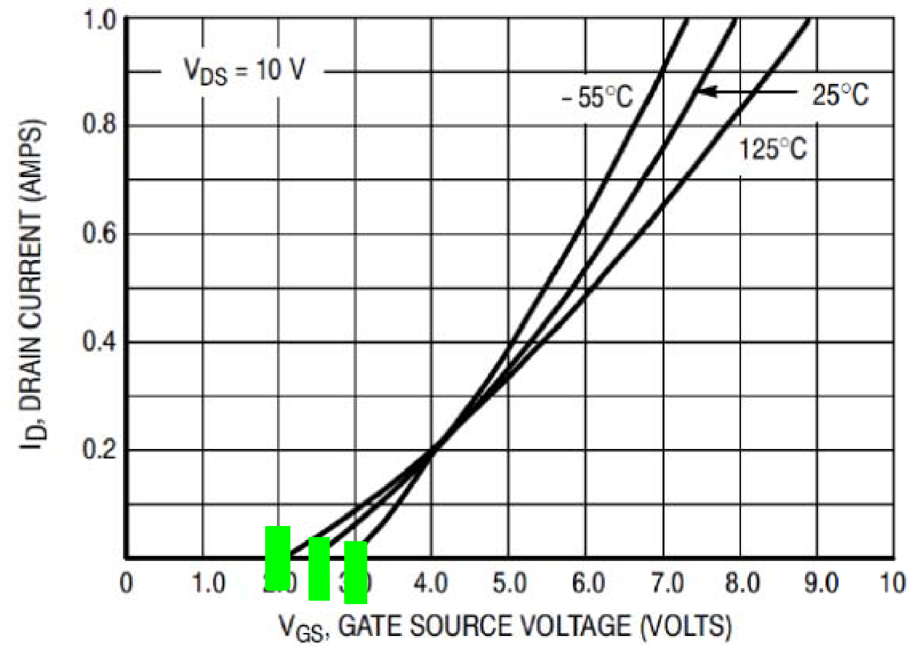
Commercially available

I_D vs V_{DS}

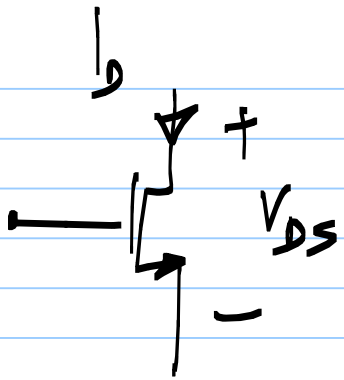


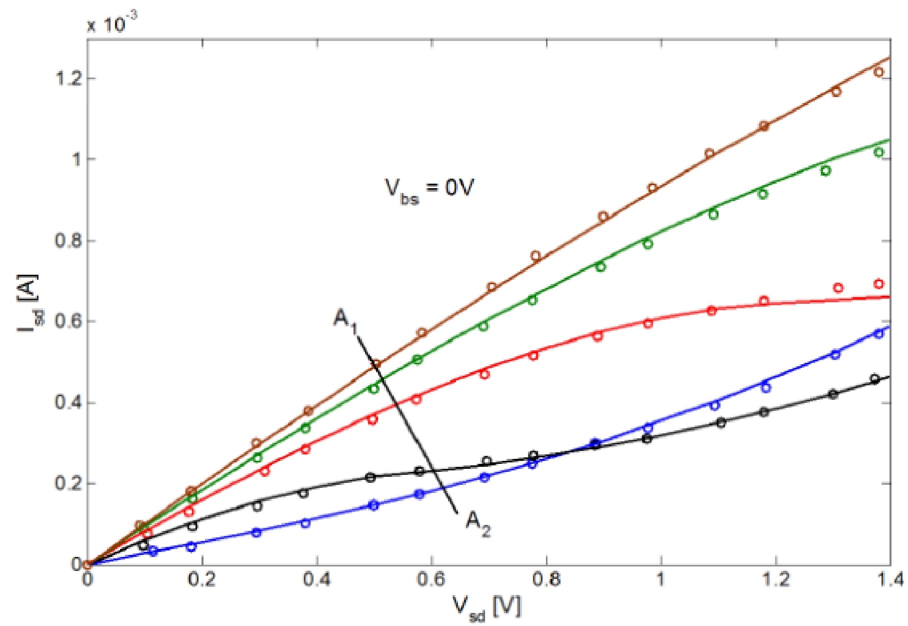
I_D vs V_{GS}

2N7000 (MOS): I_{out} vs. V_{in}



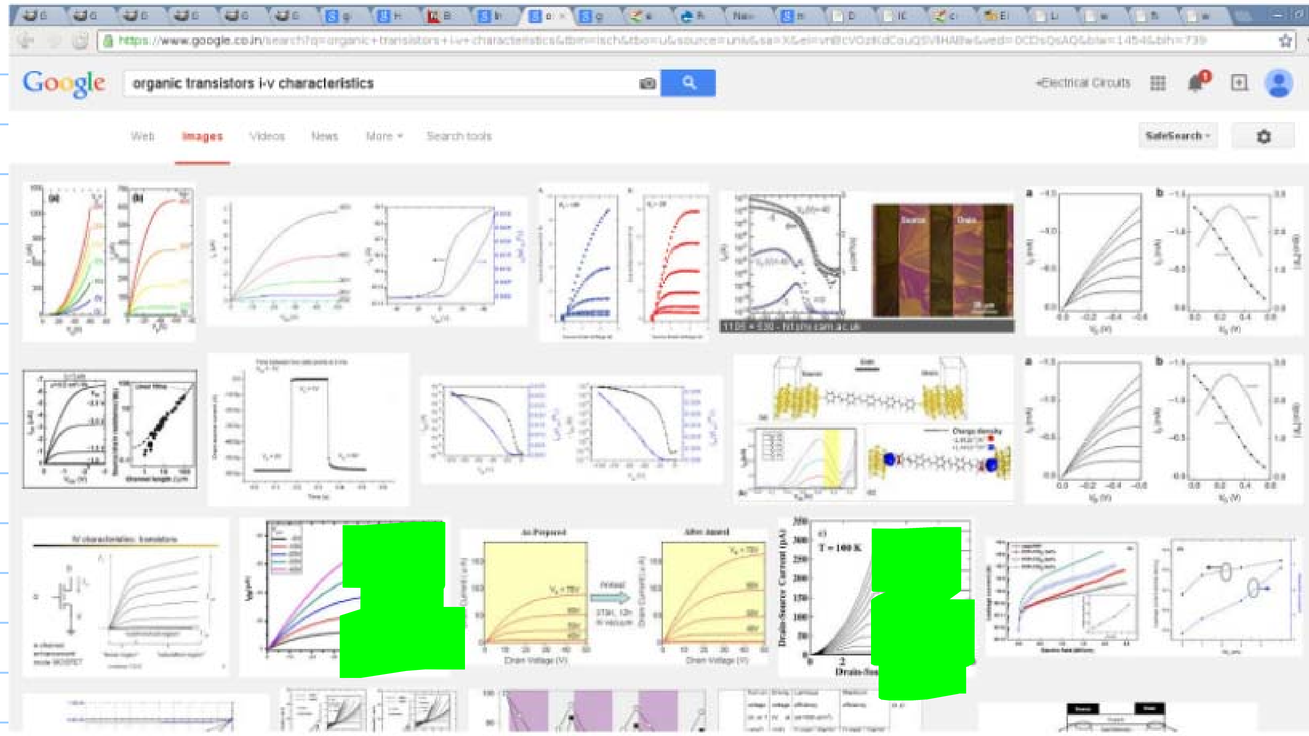
Graphene FET: I_{out} vs. V_{in}





Source: http://www.cnt.ecs.soton.ac.uk/gfet_web/model.htm

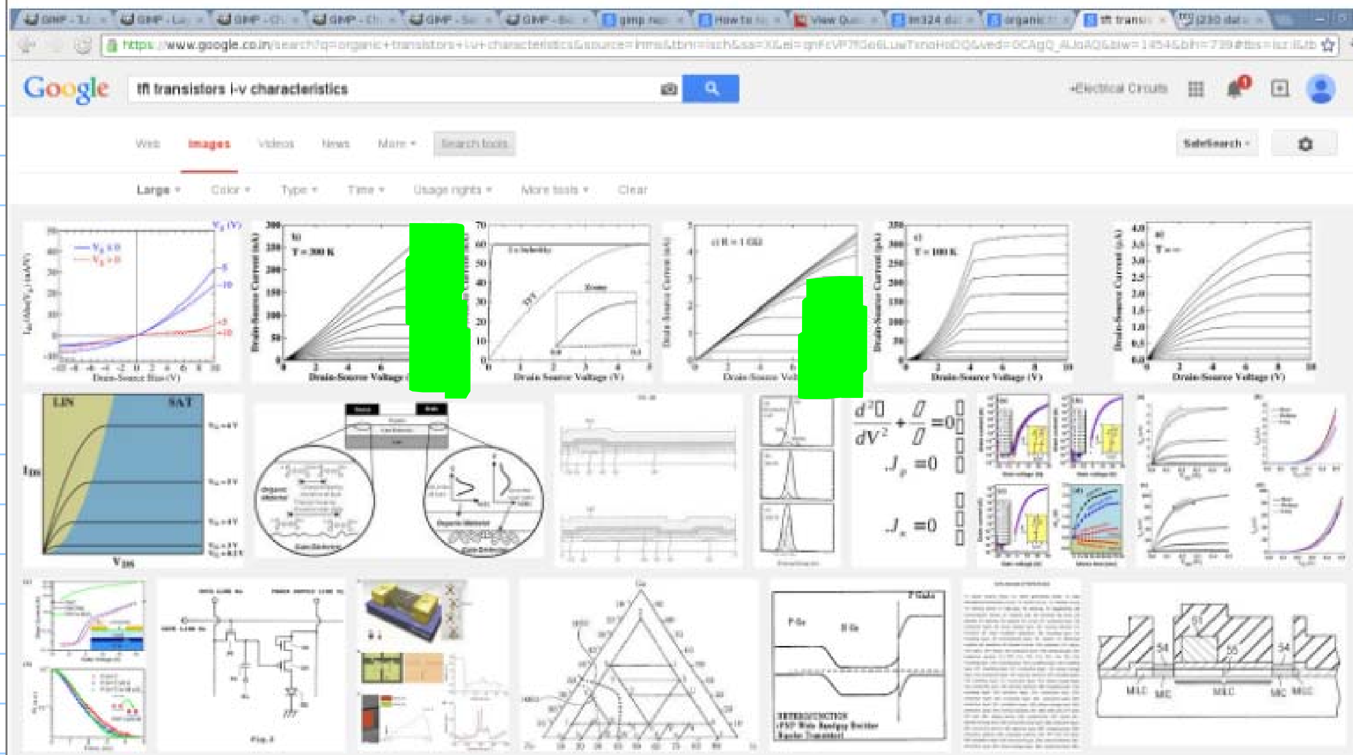
Organic transistors



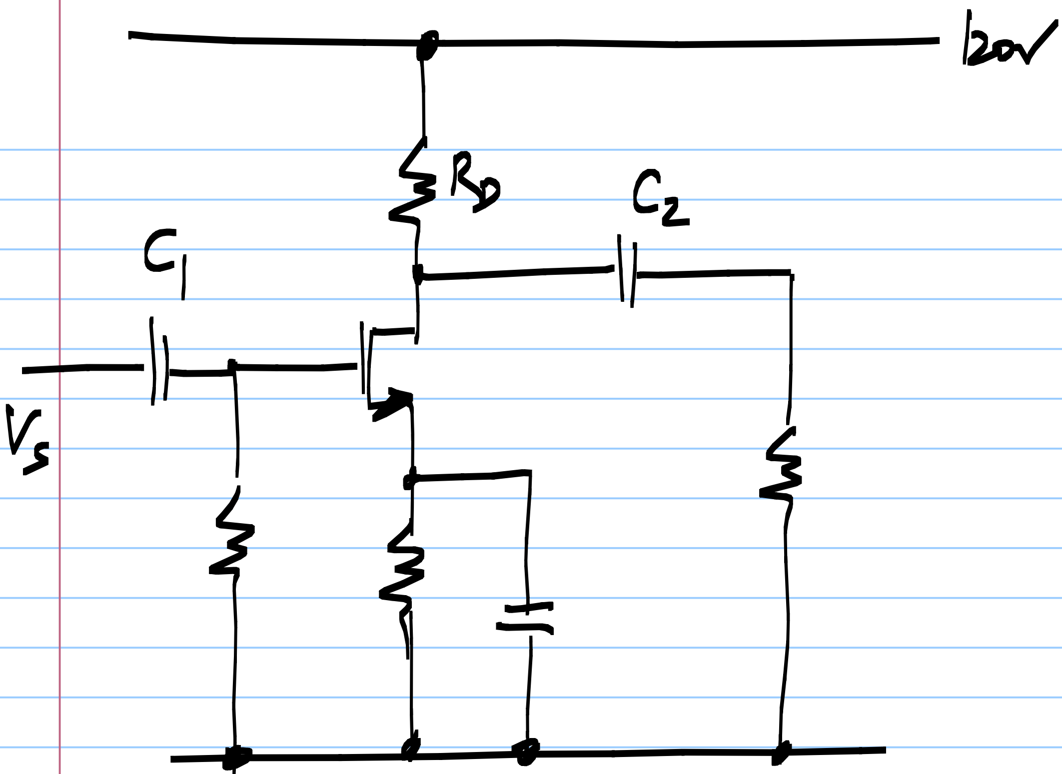
Source: Google image search "organic transistors i-v characteristics"
https://www.google.co.in/search?q=organic+transistors+i-v+characteristics&tbm=isch&tbo=u&source=univ&sa=X&ei=vnBcVOzlKdCouQSVIIHABw&ved=0CDsQsAQ&biw=1454&

I_D vs V_{DS}

TFT transistors



Source: Google image search "tft transistor i-v characteristics" https://www.google.co.in/search?q=tft+transistor+i+v+characteristics&source=lnms&tbm=isch&sa=X&ei=EatgVJiAHIPVuQT45IKYAQ&ved=0CAgQ_AUoAQ&biw=1454&bih=739



$V_{GS} = -2.5V$

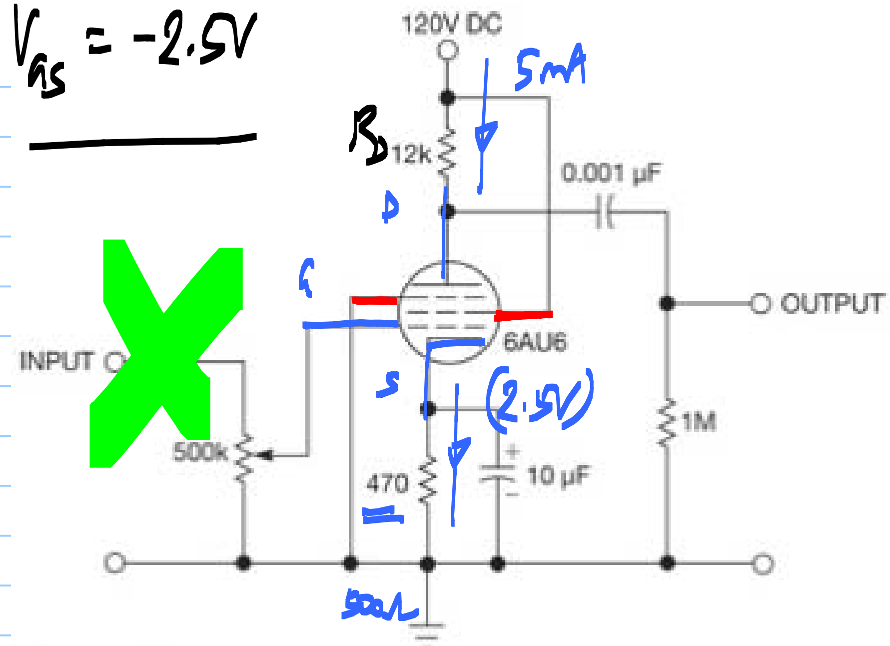
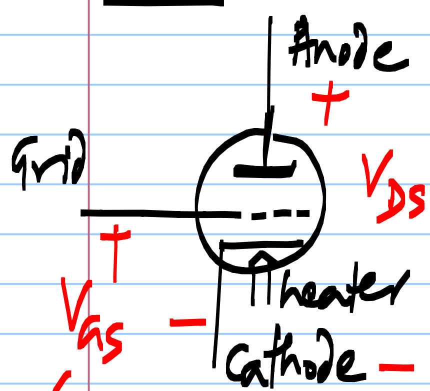
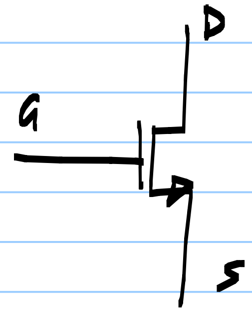


Figure 1 A 6AU6 pentode vacuum tube needs a quiescent plate current of approximately 5 mA.

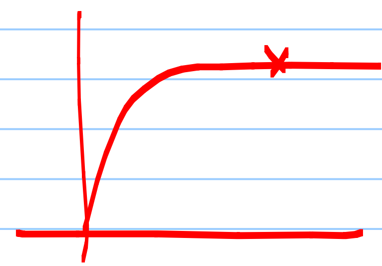
Triode (plate)





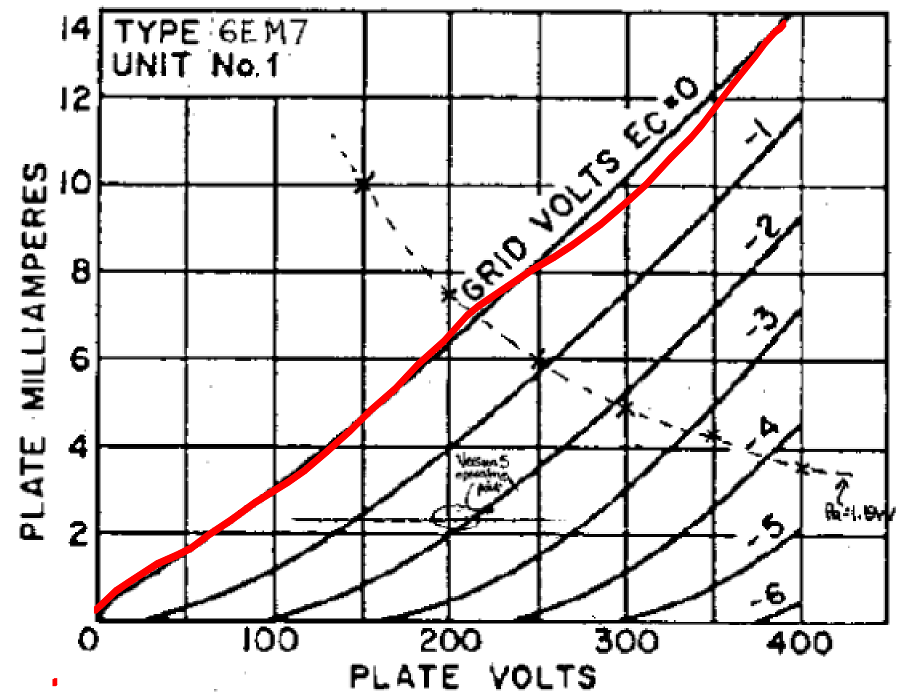
$V_{GS} < 0$

$V_{DS} \sim$ 100s of V

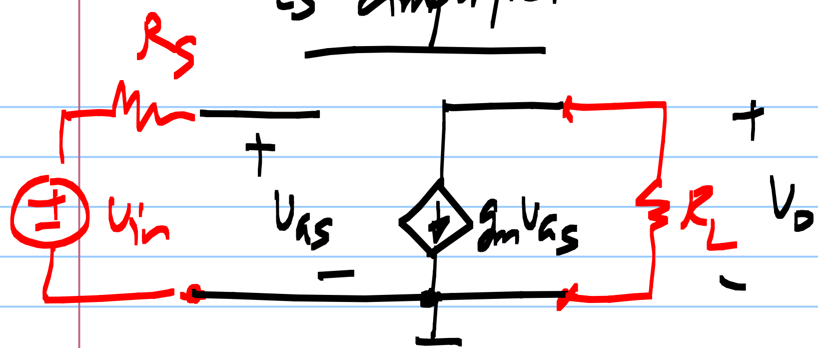


I_D V_G V_{DS}

Triode: I_{out} vs. V_{out}



CS amplifier



$$\frac{v_o}{v_{in}} = -g_m R_L$$

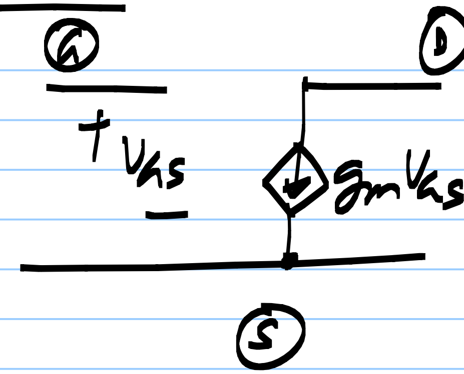
Controlled sources

VCVS

VCCS

CCCS

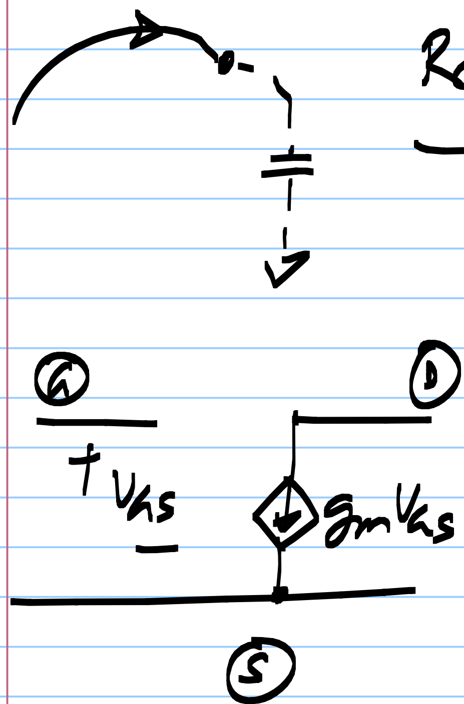
CCVS



−ve fb: Sense difference between desired & actual; drive the actual output in a way that reduces the difference.

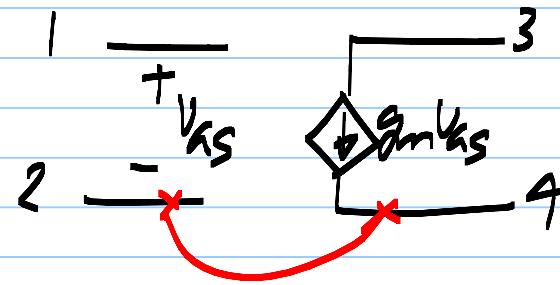
Increase node voltage: push a current into it

Reduce node voltage: pull a current out of it



"input" : G/S

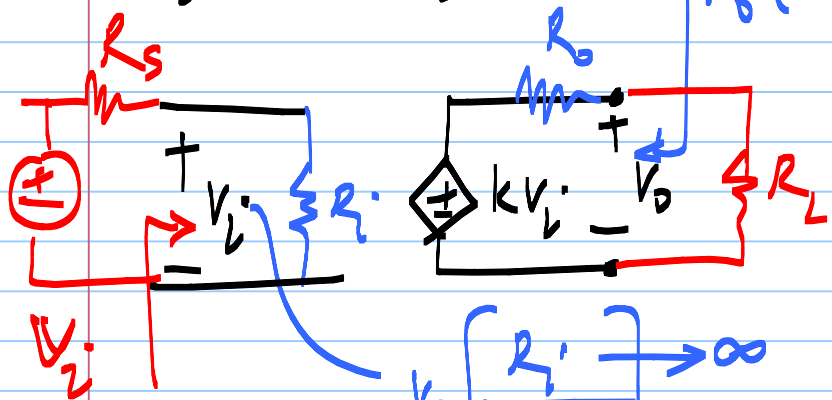
"output" : D/S



Voltage controlled voltage source

$v_o = k \cdot v_i$

R_o (output resistance)



$R_i = \infty$

$$v_i \underbrace{\left[\frac{R_i}{R_s + R_i}\right]}_{} \qquad R_i \to \infty, \quad \frac{R_i}{R_s+R_i} \to 1$$

$$kv_i \left[\frac{R_L}{R_o + R_L}\right] \to 1$$

$R_o \to 0$

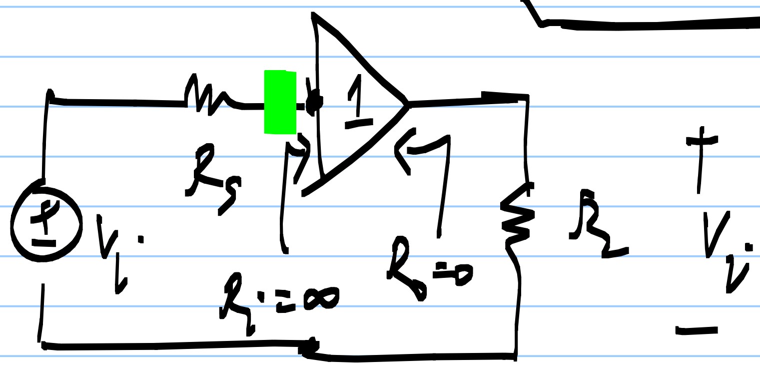
$R_i = \infty$; $R_o = 0$

R_i very large $\gg$ expected R_s

R_o very small $\ll$ expected R_L

Realizing a VCVS using an MOS transistor.

VCVS $k=1$ $\quad \underbrace{V_o = V_i \quad R_i \to \infty \; ; \; R_o \to 0}_{\text{Voltage buffer}}$

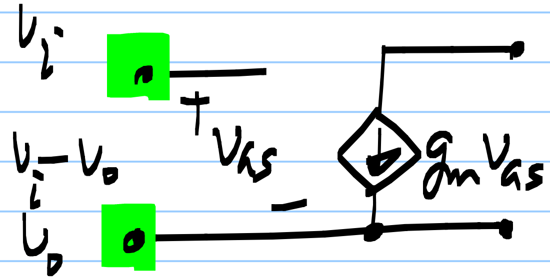


VCVS with K = 1

Voltage buffer using a MOS transistor

$v_o = v_i$

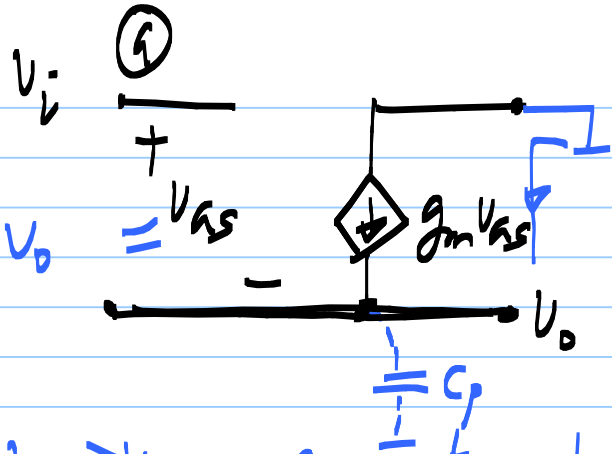
v_{GS}: $\left.\begin{array}{l} v_i - v_o \\ v_o - v_i \end{array}\right)$ $v_o = v_i$



$v_i > v_o$: v_o must be pushed up
current must be pushed into the o/p node

$v_i < v_o$: v_o must be pulled down
current must be pulled out of the o/p node

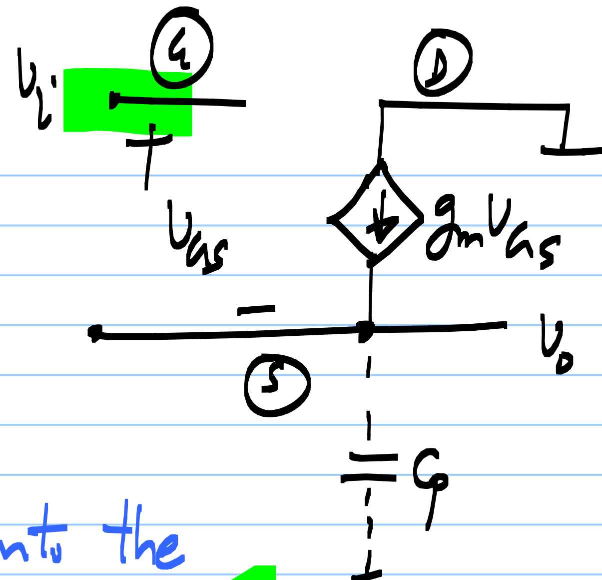
$v_{GS} > 0$: current is pushed into the source of the MOS transistor



$v_i - v_o = v_{GS}$

$v_i > v_o$: current pushed into the source node

v_o increases

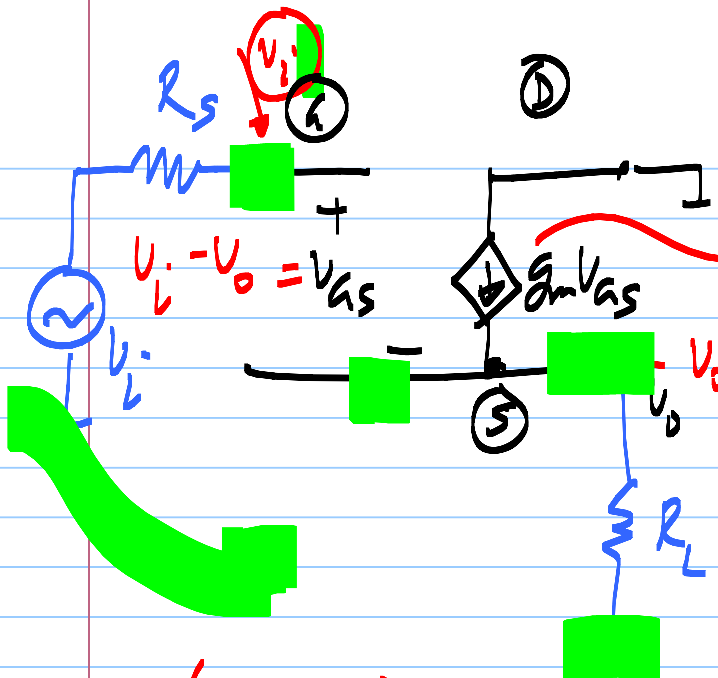


In steady state

$v_o = v_i$

$k = 1$

$R_i = \infty$



$$\boxed{v_o = v_i}$$

$$v_o = \frac{g_m R_L}{1 + g_m R_L} \cdot v_i \doteq \frac{g_m}{g_m + G_L} \cdot v_i$$

$R_i = \infty$

$R_o = 0$

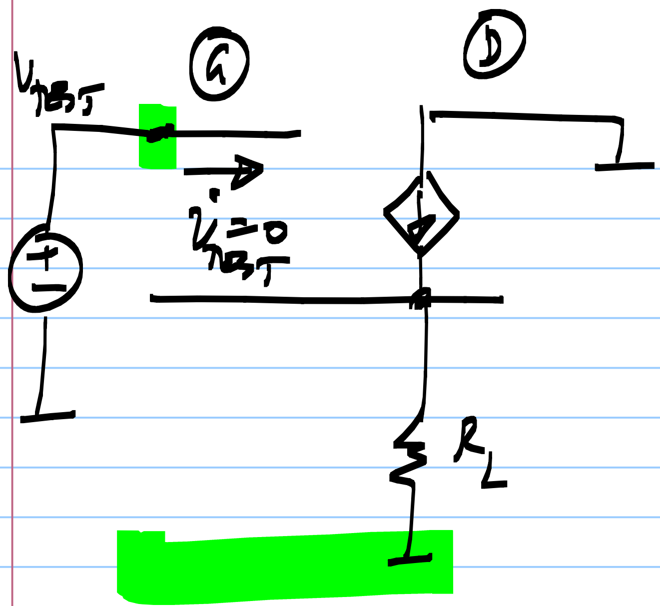
$\simeq 1$ if $g_m R_L \gg 1$

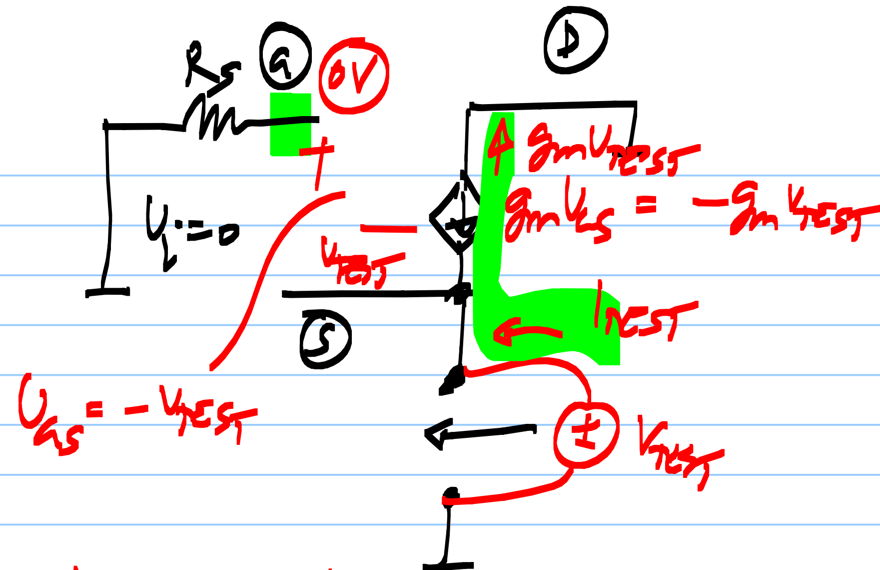
$g_m \gg G_L$

$g_m(v_i - v_o)$

load conductance $G_L = 1/R_L$

$$g_m(v_i - v_o) = v_o/R_L = v_o \cdot G_L$$





$R_{out} = 0$
(ideal)

$R_{out} = 1/g_m$

$$R_{in} = \frac{v_{TEST}}{i_{TEST}} = \infty$$

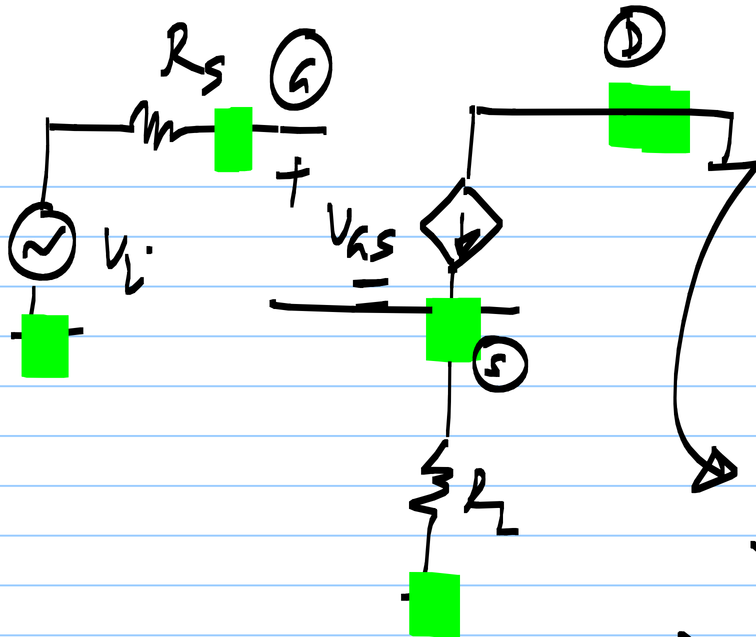
$$R_{out} = \frac{v_{TEST}}{I_{TEST}} = \frac{v_{TEST}}{g_m v_{TEST}} = \frac{1}{g_m}$$

$R_{out} \ll R_L$ in a VCVS

$\frac{1}{g_m} \ll R_L$ $\quad$ $\left.\begin{array}{l} g_m R_L \gg 1 \\ g_m \gg 1/R_L \end{array}\right]$ Same as the condition to get $v_o/v_i \simeq 1$

$$\frac{v_o}{v_i} = \frac{g_m R_L}{g_m R_L + 1} \simeq 1 \text{ if } g_m R_L \gg 1$$

$R_{in} = \infty$; $\quad R_{out} = 1/g_m \ll R_L$



Common drain amplifier

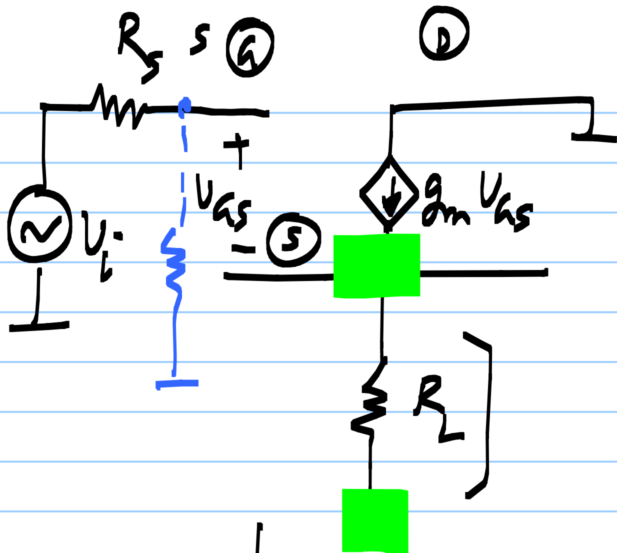
$$V_o = V(\text{source}) \simeq V_i = V(\text{gate})$$

Source voltage follows the gate voltage

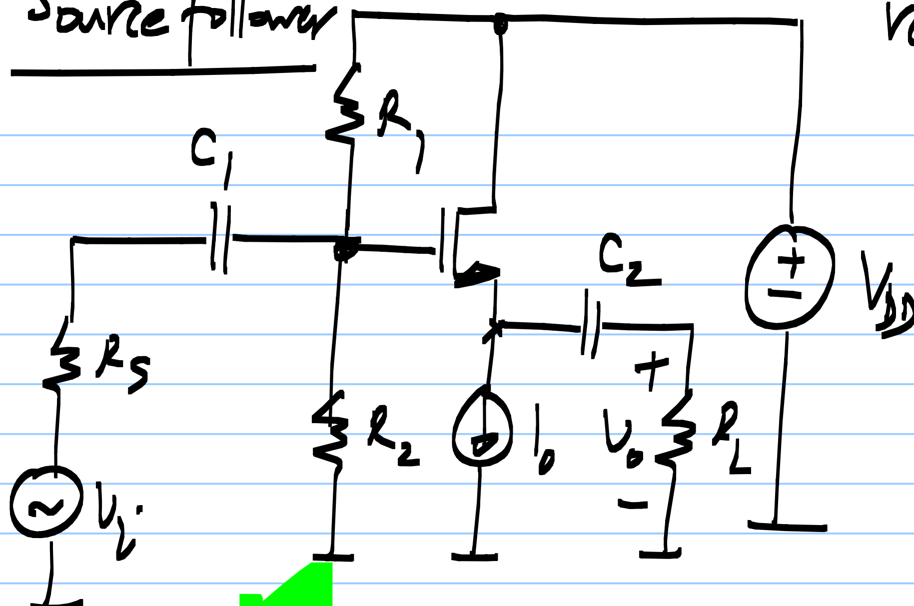
Source follower

Input between gate-drain

o/p between source-



Source follower



VCVS $\quad \frac{v_o}{v_i} = 1$

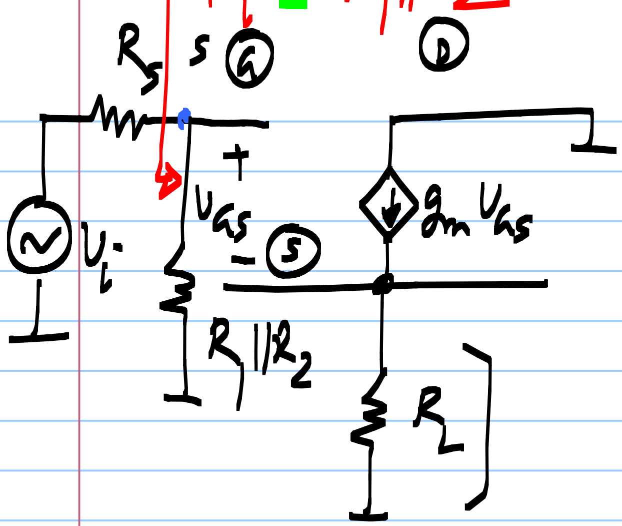
$g_m R_L \gg 1$

$\omega_{min} > 0$

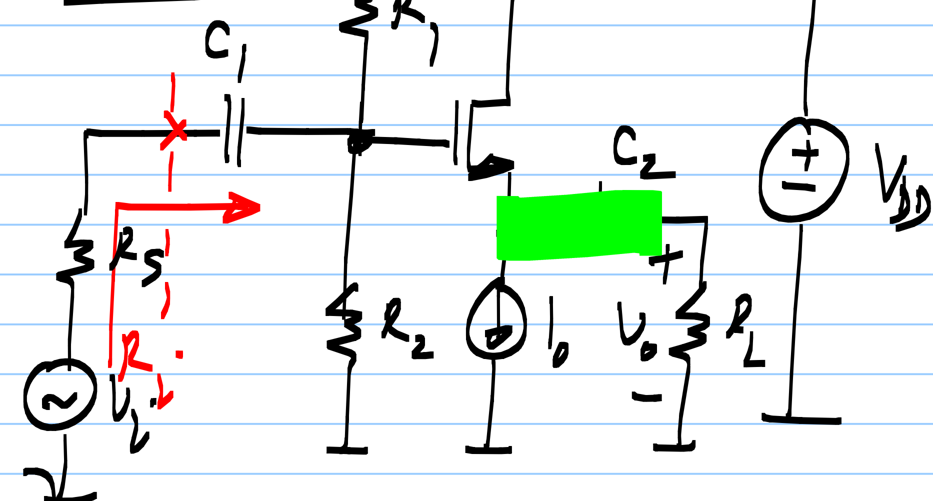
CS $\quad \frac{v_o}{v_i} = -g_m R_L = -1 \qquad g_m R_L \gg 1$

CD $\quad \frac{v_o}{v_i} = \frac{g_m R_L}{1 + g_m R_L} \simeq 1$

$R_i = R_1 \| R_2$

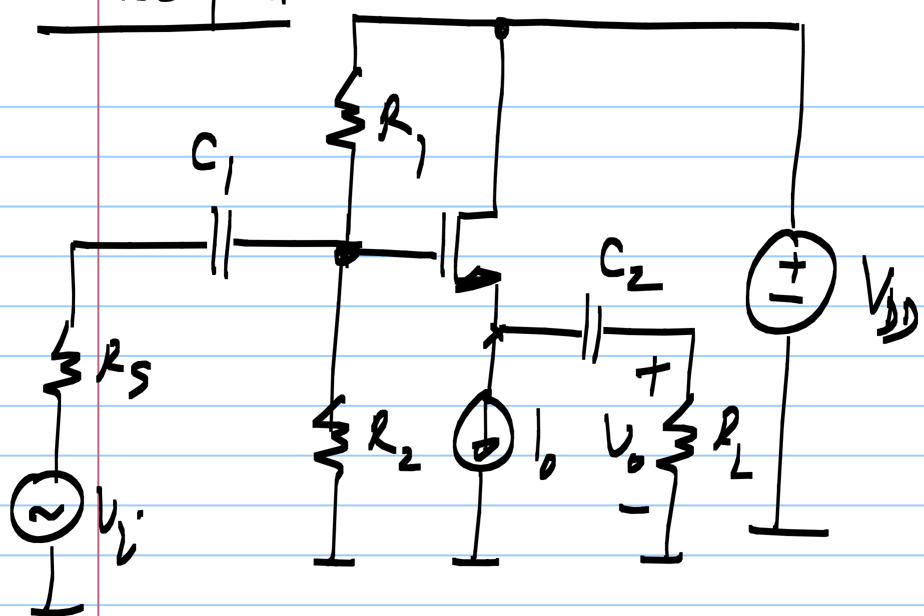


$C_1, C_2 \to \infty$

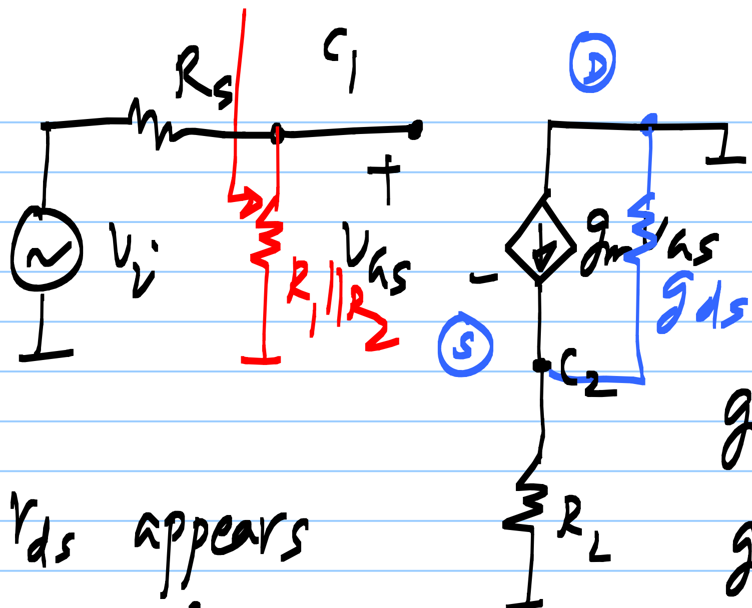


$$v_g = v_i \left[\frac{R_1 \| R_2}{R_s + (R_1 \| R_2)} \right] \simeq v_i \qquad R_1, R_2 \gg R_s$$

Source follower



* Effect of λ
* Find constraints on C_1 & C_2



$$\frac{v_o}{v_i} = \frac{g_m R_L}{1 + g_m R_L} \Rightarrow \frac{g_m (R_L \| r_{ds})}{1 + g_m (R_L \| r_{ds})}$$

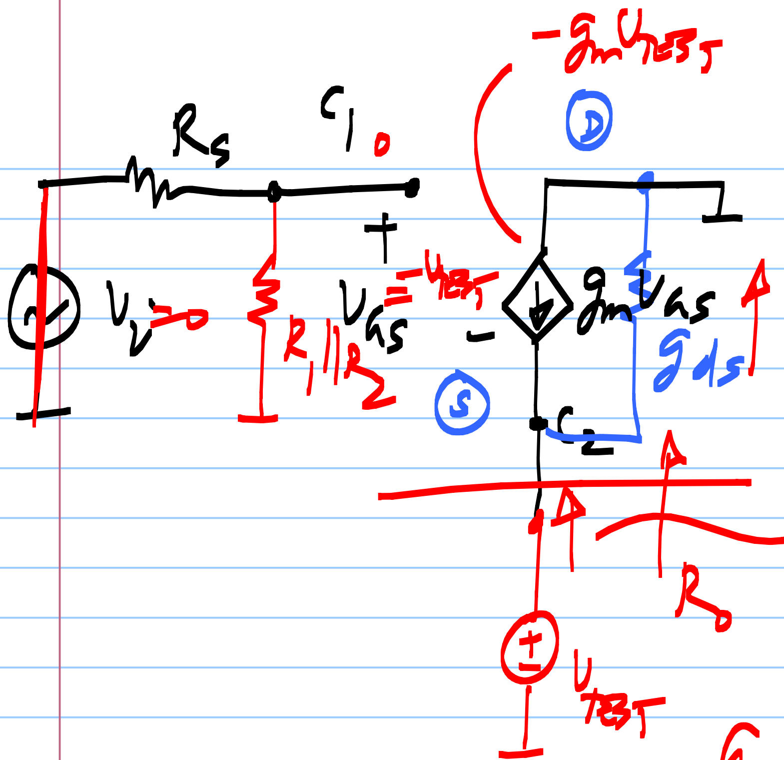
$$= \underbrace{\frac{g_m}{g_m + G_L + g_{ds}}}$$

$g_m \cdot R_L \| r_{ds} \gg 1$

$\underline{g_m \gg G_L + g_{ds}}$

r_{ds} appears across R_L

$R_L \longrightarrow R_L \| r_{ds}$



$v_{TEST}\, g_{ds}$

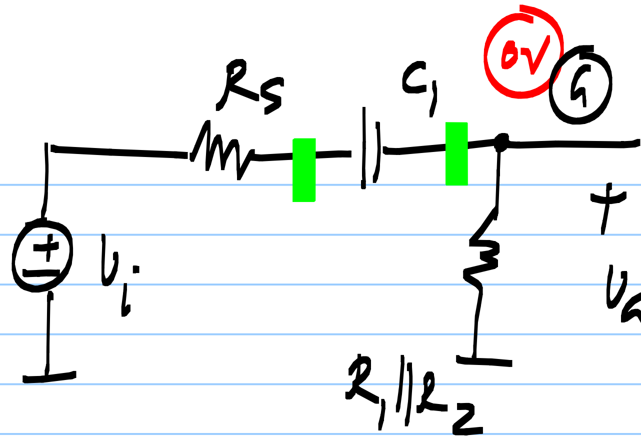
$(g_m + g_{ds})\, v_{TEST}$

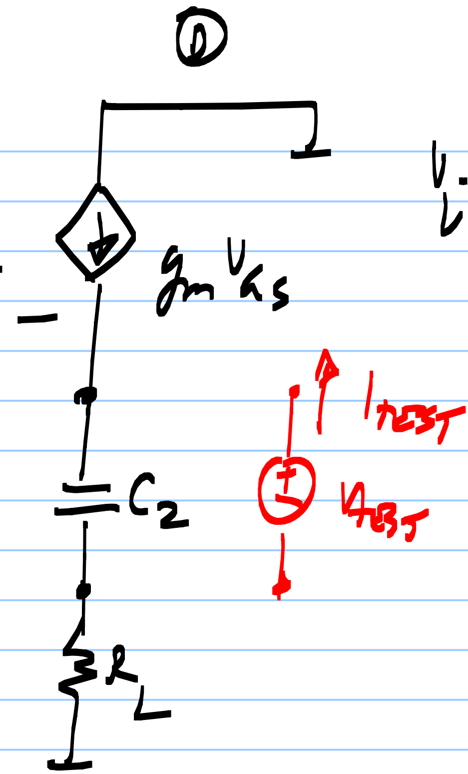
$$G_{out} = g_m + g_{ds} \quad ✓$$

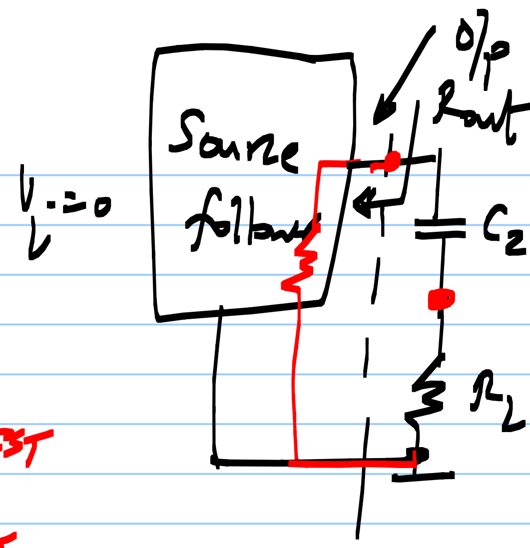
$$\underline{g_m \gg g_{ds}}$$

$$R_{out} = \frac{1}{g_m + g_{ds}}$$

$$G_{out} = \frac{g_m + g_{ds} \cdot \cancel{v_{TEST}}}{\cancel{v_{TEST}}}$$







Resistance across C_1:

$$R_S + R_1 \| R_2$$

$$C_1 \gg \frac{1}{\omega\left(R_S + R_1 \| R_2\right)}$$

Resistance across C_2 $= R_L + R_{out}$ $\longrightarrow$ $\frac{1}{g_m}$ ✓ ; $\underbrace{\frac{1}{g_m + g_{ds}}}$

$= R_L + \frac{1}{g_m}$

$$C_2 \gg \frac{1}{\omega\left(R_L + \frac{1}{g_m}\right)} \simeq \frac{1}{\omega R_L}$$

$g_m R_L \gg 1$ $\quad$ $R_L \gg \frac{1}{g_m}$

$$\frac{v_o}{v_i} = \frac{g_m R_L}{1 + g_m R_L} \rightarrow \frac{g_m (R_L \| r_{ds})}{1 + g_m (R_L \| r_{ds})}$$

$(g_m R_L \gg 1)$

$$R_i = R_1 \| R_2$$

$$R_{out} = \frac{1}{g_m} \rightarrow \frac{1}{g_m + g_{ds}}$$

$$C_1 \gg \frac{1}{\omega (R_s + R_1 \| R_2)}$$

$$C_2 \gg \frac{1}{\omega (R_L + 1/g_m)}$$