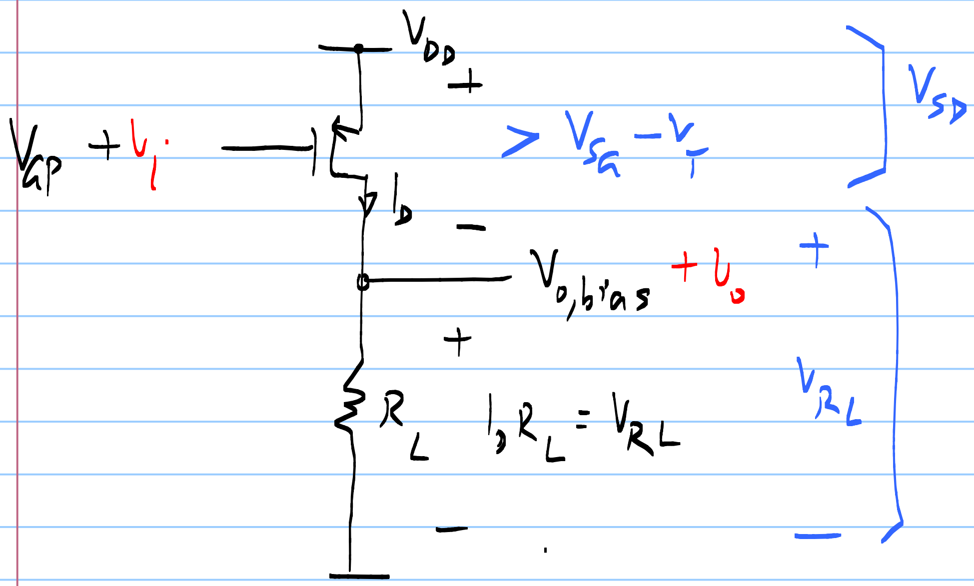
Note Title 20-06-2018

$V_{DD} = V_{SD} + V_{R_L} \geq \underbrace{V_{SG} - V_T}_{\geq 200mV} + V_{R_L}$

V_{R_L}

pMOS Common source amplifier



$$\text{Gain magnitude} = \sqrt{g_m R_L} = \frac{2 \cdot}{V_{SG} - V_T}$$

Increase g_m : Increasing I_D, W/L

Increase R_L :

$$g_m = \frac{2 I_D}{\underbrace{V_{SG} - V_T}_{\text{overdrive voltage}}}$$

Operating point

$V_{SG} = V_{DD} - V_{GP}$

$V_{o,bias} = I_D \cdot R_L$

$$I_D = \frac{\mu_p C_{ox}}{2} \frac{W}{L} \cdot (V_{SG} - V_T)^2$$

Signal:

$v_o = - g_m R_L \cdot v_i$

Gain magnitude : $\boxed{\dfrac{2 \cdot V_{RL}}{V_{SG} - V_T}}$ $\boxed{\dfrac{2 \cdot 1V}{200mV}}$ 10

$I_D = \dfrac{\mu_p C_{ox}}{2} \dfrac{W}{L} (V_{SG} - V_T)^2$

Decreasing $V_{SG} - V_T$: Square law model valid only if

$$\underbrace{V_{SG} - V_T}_{\sim 200mV \text{ or more}} \gg \frac{kT}{q} \sim 25mV \text{ @ } 300K$$

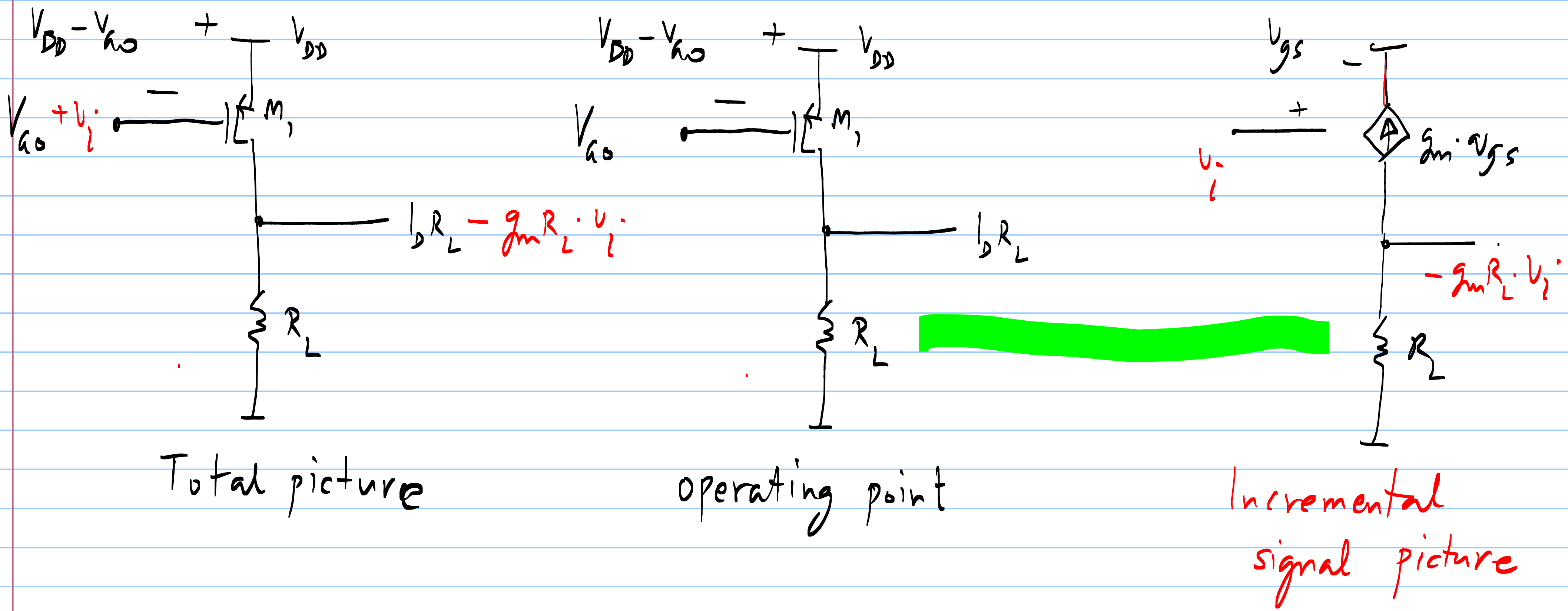
$V_{SG} - V_T \geq 200mV$, for operation in saturation region

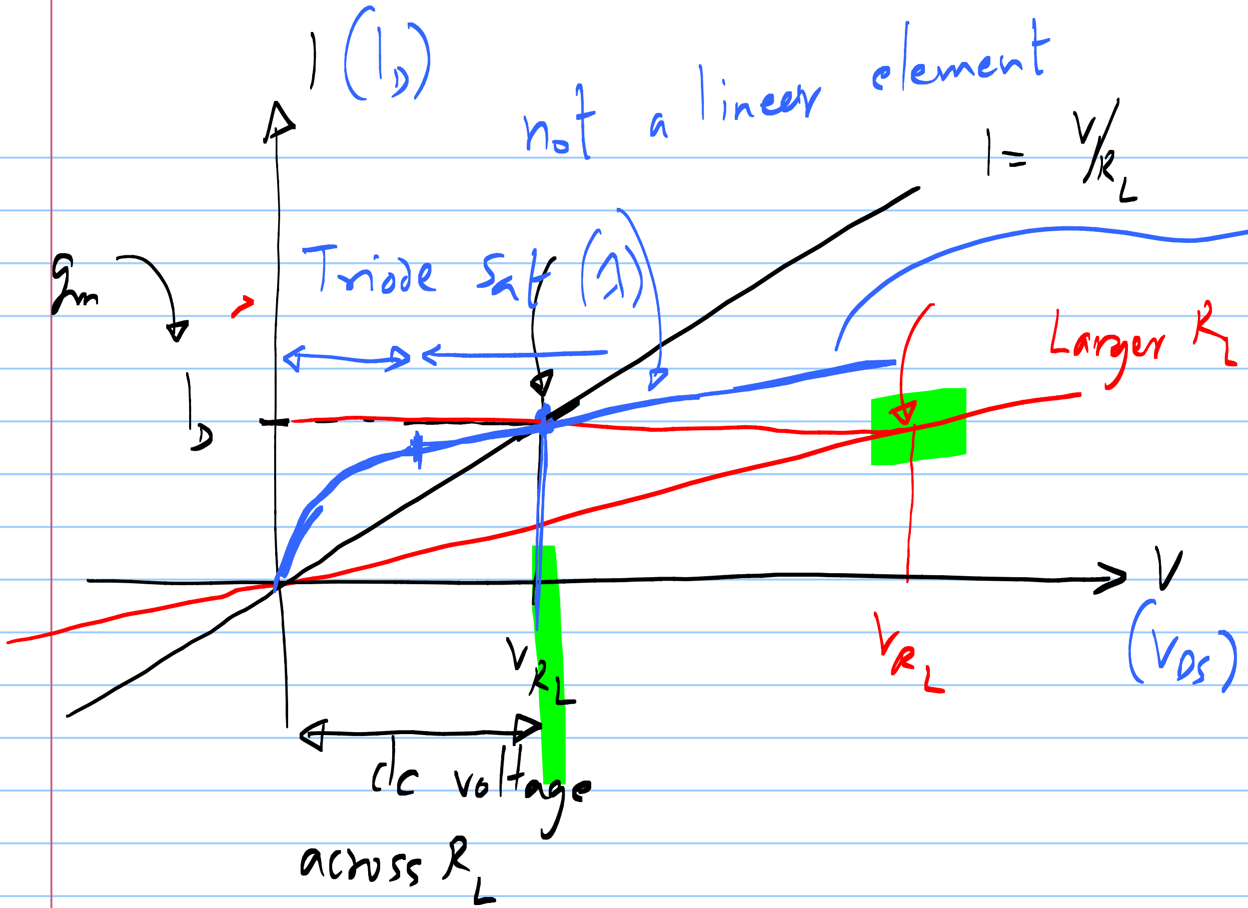
Increase V_{RL} : $\Rightarrow$ We have to increase V_{DD}

$V_{DD} > 10.2V$

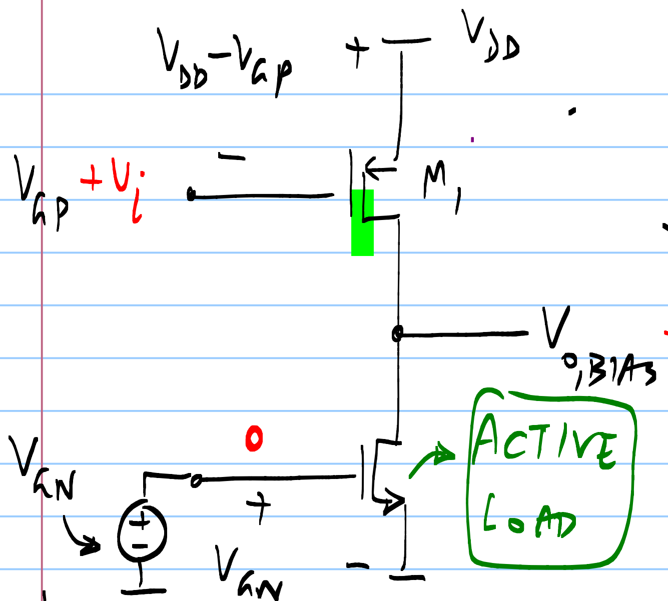
$I_{DD} = \boxed{\dfrac{2 \cdot 10V}{200mV}}$

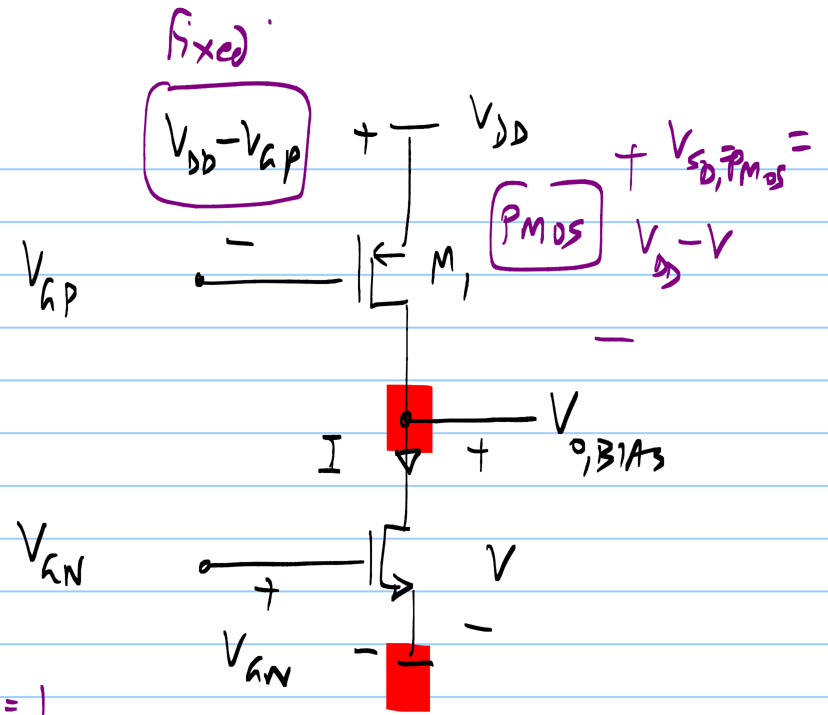
Common source amplifier with a large gain

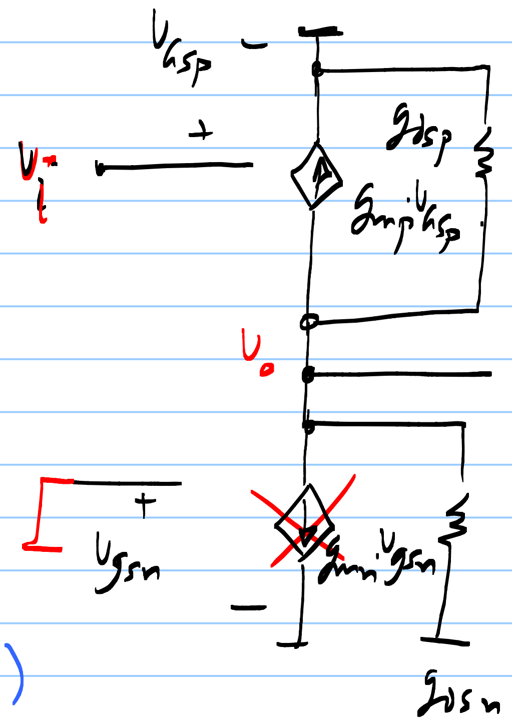


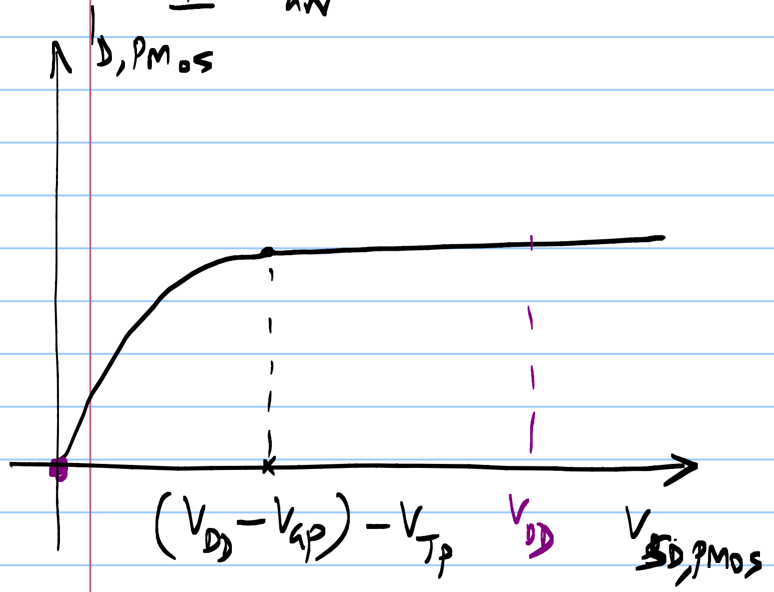


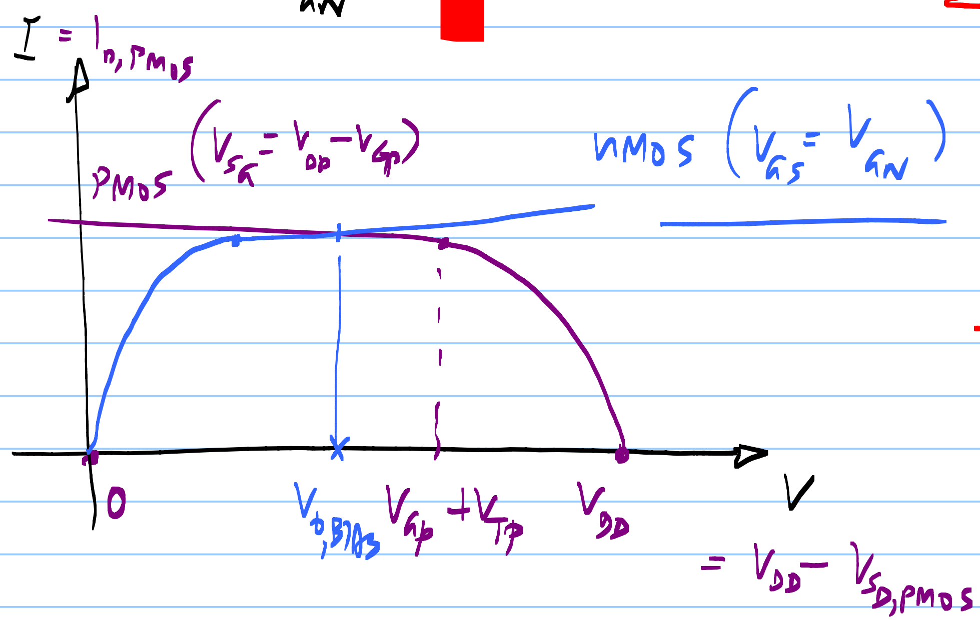
$I_D - V_{DS}$ characteristic of an nMOS transistor for a given V_{GS}





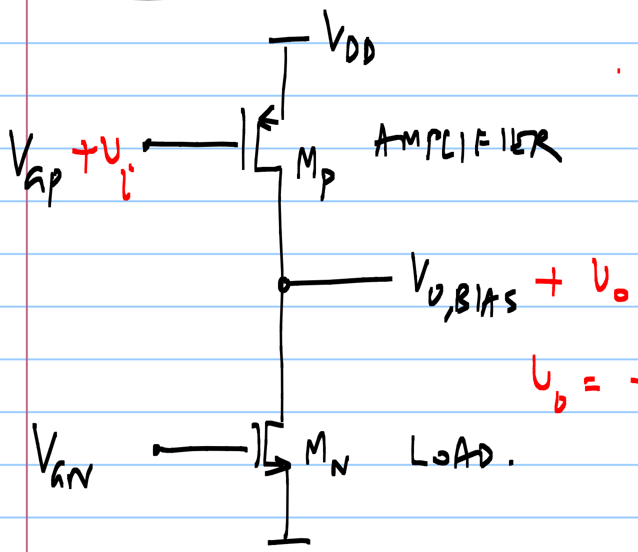






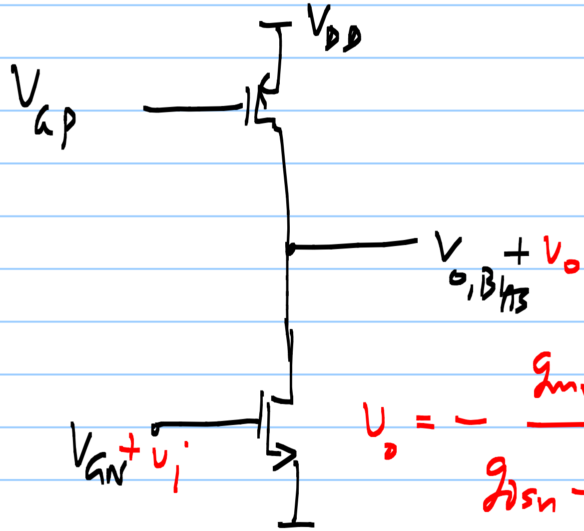
$$\frac{v_o}{v_i} = -\frac{g_{mp}}{g_{dsp} + g_{dsn}}$$

pMOS CS amplifier with nMOS active load

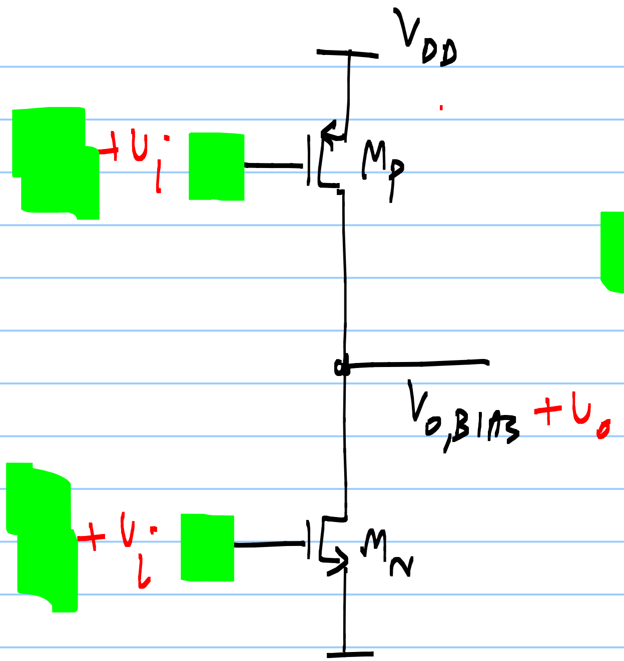


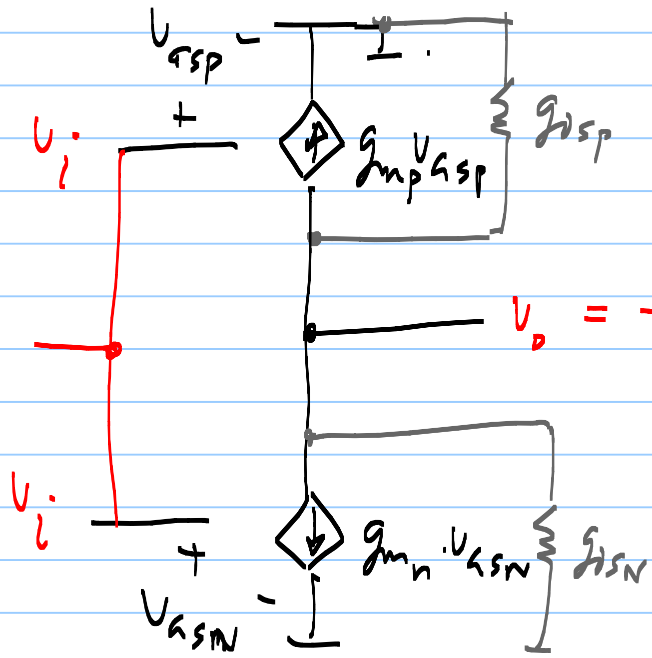
$$v_o = -\frac{g_{mp}}{g_{dsp} + g_{dsn}} \cdot v_i$$

nMOS CS amplifier with pMOS active load

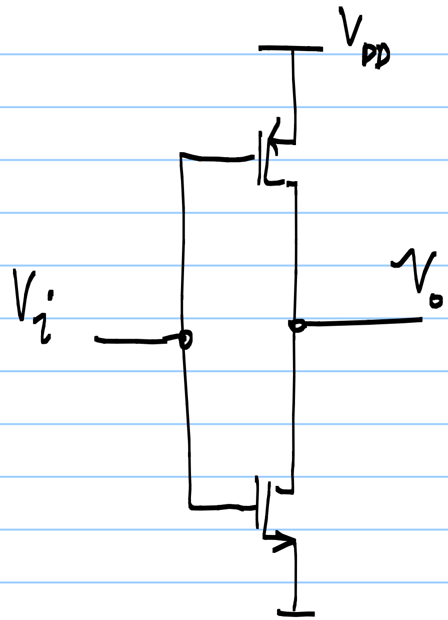


$$v_o = -\frac{g_{mn}}{g_{dsn} + g_{dsp}} \cdot v_i$$





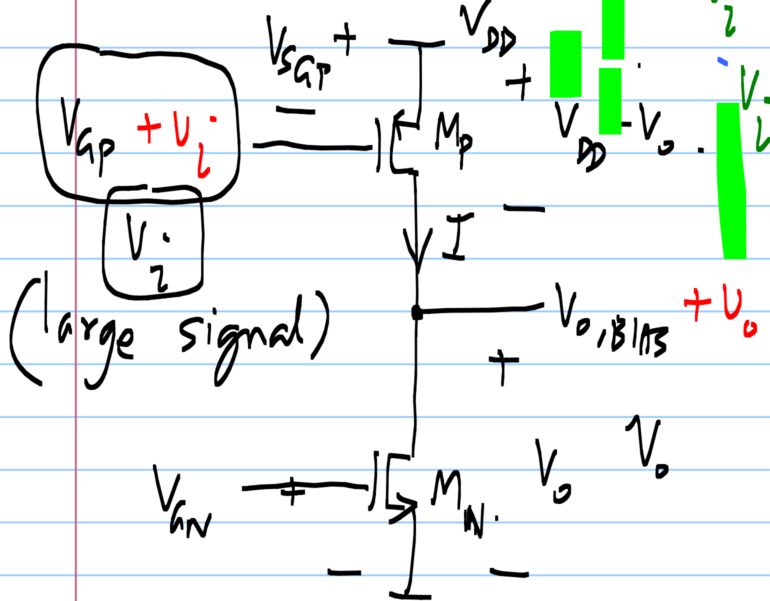
$$v_o = - \frac{g_{mN} + g_{mP}}{\underbrace{g_{dsN} + g_{dsP}}} \cdot v_i$$

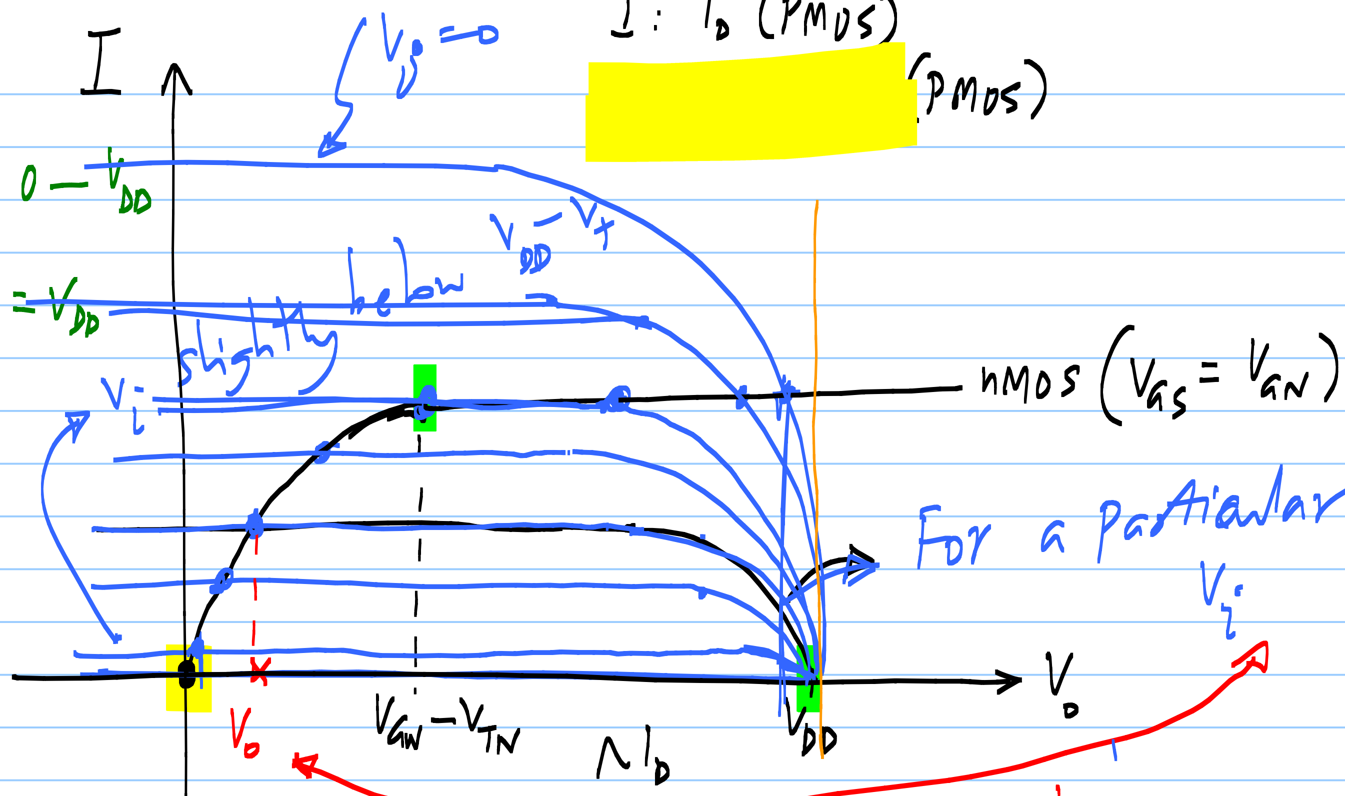


CMOS inverter

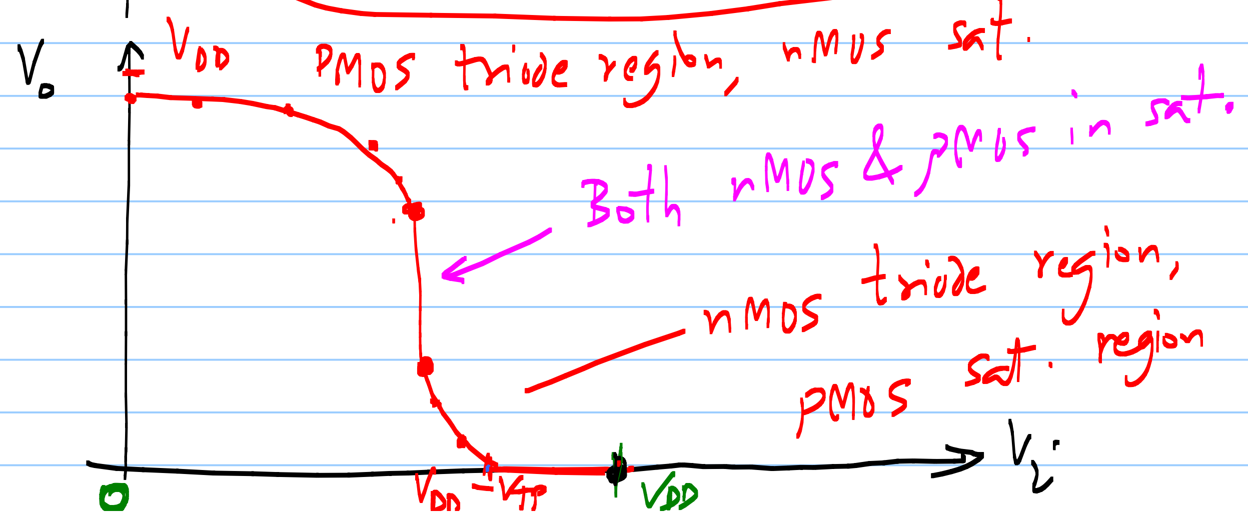
$V_{Gp} = V_{Gn}$

PMOS CS amplifier
w/ nMOS active load





V_o vs. V_i



PMOS:

$V_{SGP} = V_{DD} - V_i$

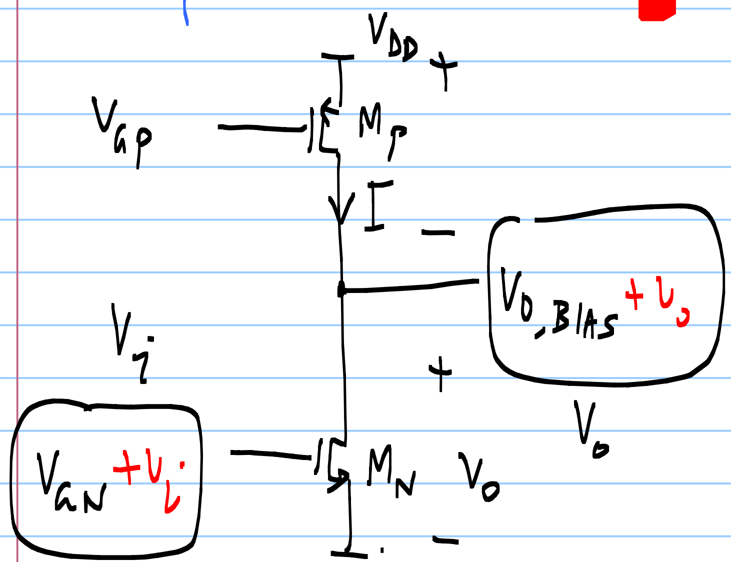
$V_{SDP} = V_{DD} - V_o$

nMOS:

$V_{GSN} = V_{GN}$

$V_{DSN} = V_o$

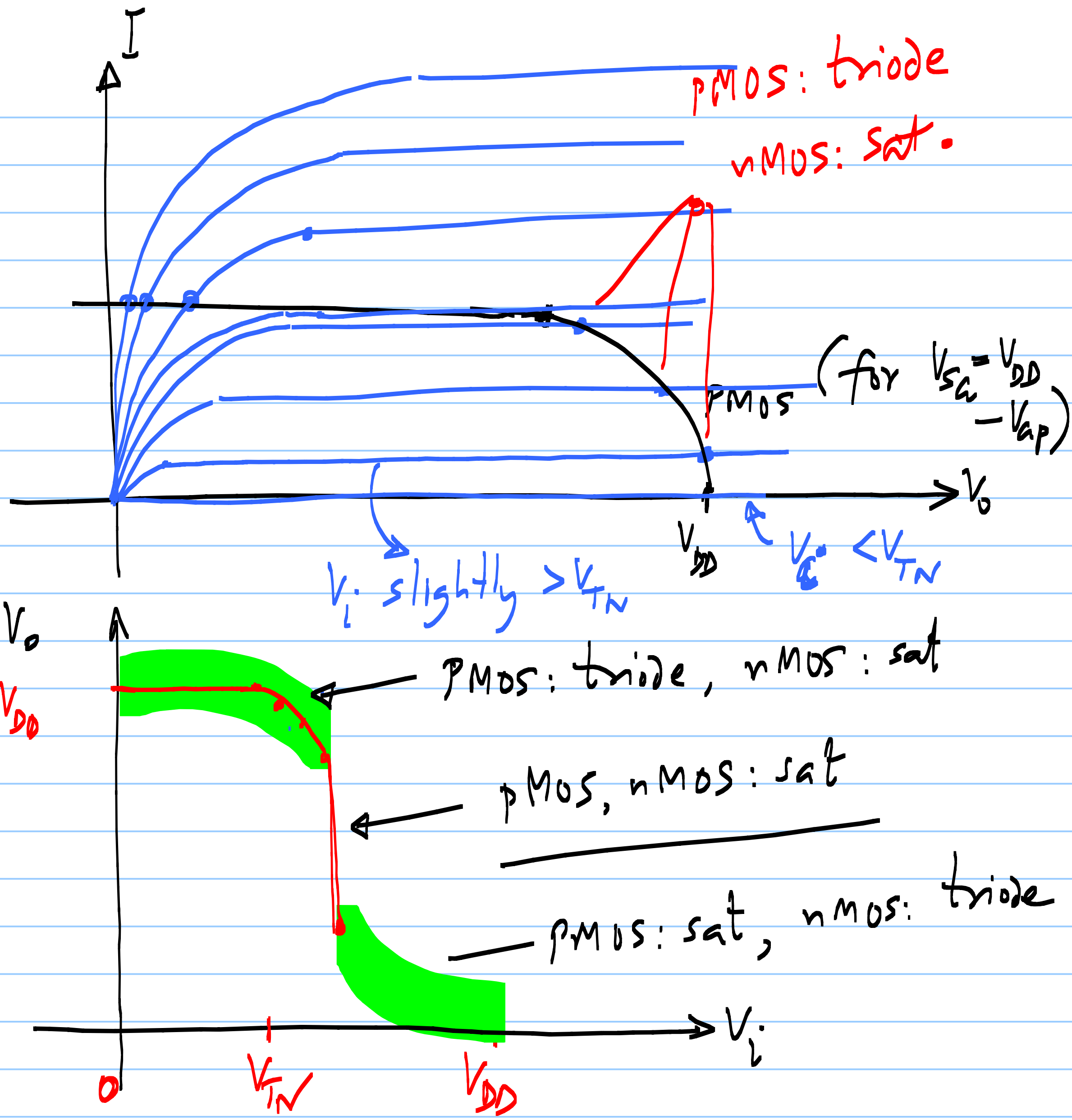
nMOS CS amplifier loaded by a pMOS active load



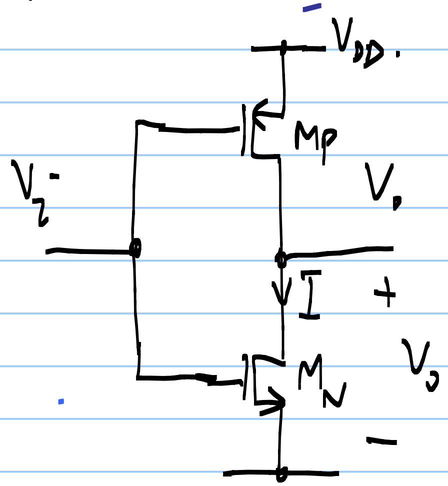
V_o vs. V_i:

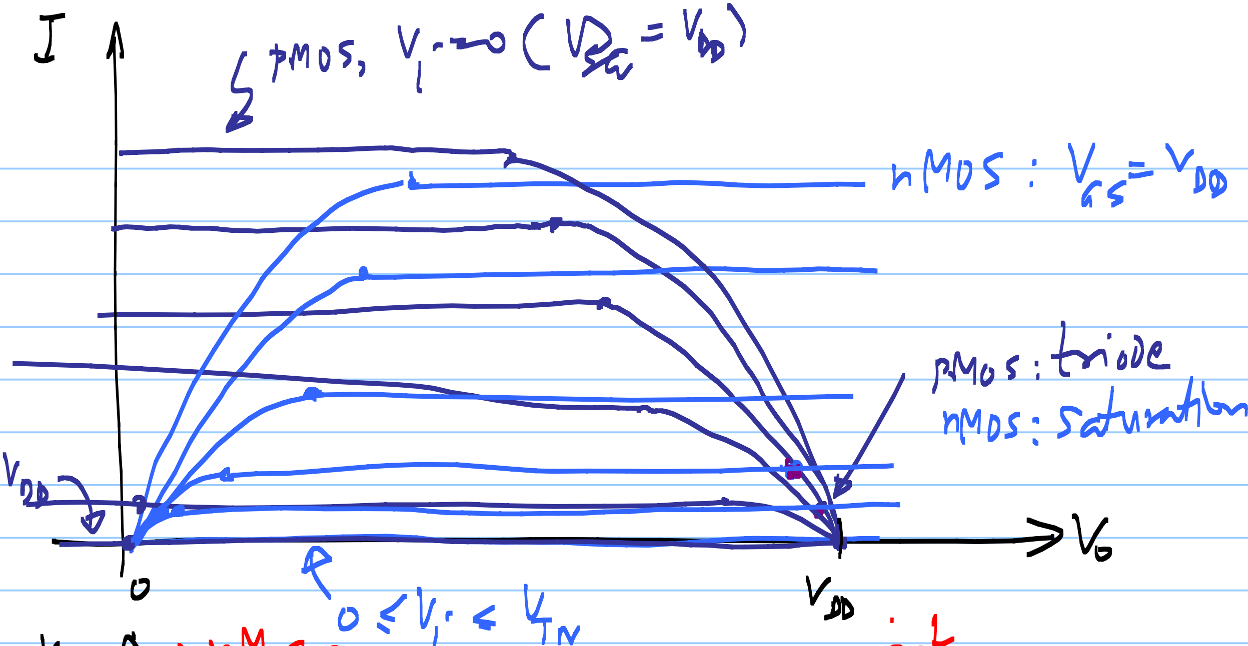
pMOS: $V_{SGp} = V_{DD} - V_{Gp}$; $V_{DD} - V_o$

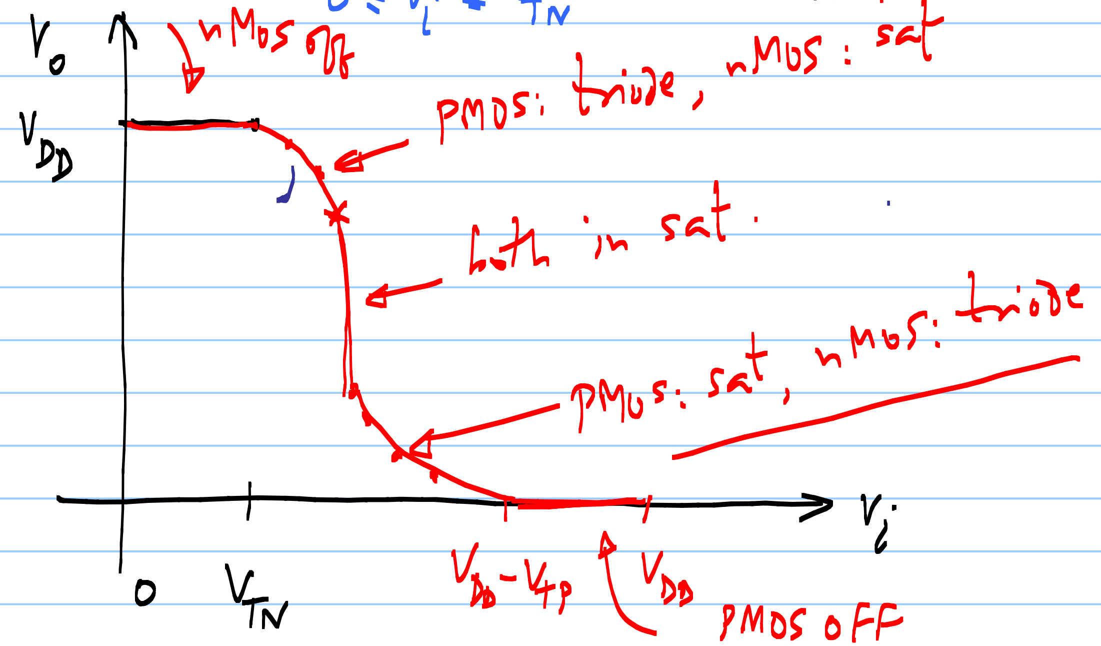
nMOS: $V_{GSN} = V_i$; $V_{DSN} = V_o$



CMOS inverter







pMOS: $V_{SG} = V_{DD} - V_i$

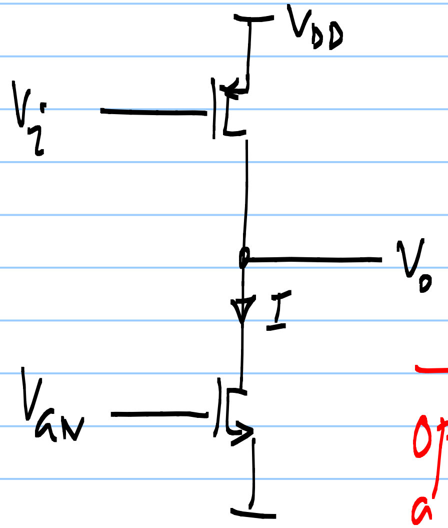
$V_{SD} = V_{DD} - V_o$

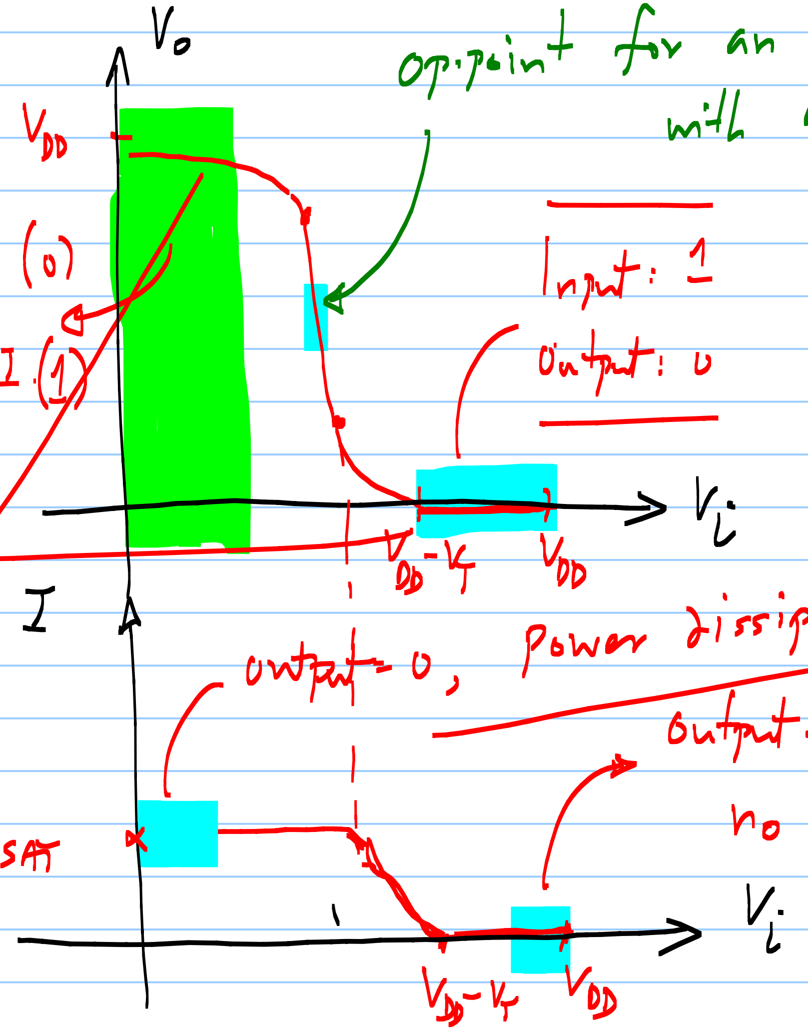
nMOS: $V_{GS} = V_i$

$V_{DS} = V_o$

CS amplifiers with active loads: Digital inverters

PMOS CS w/ nMOS Load





op. point for an analog amplifier with a high gain

Input: Lo (0)
Output: HI (1)

Operation as a digital inverter

Input: 1
Output: 0

Static power dissipation

output = 0, power dissipation > 0

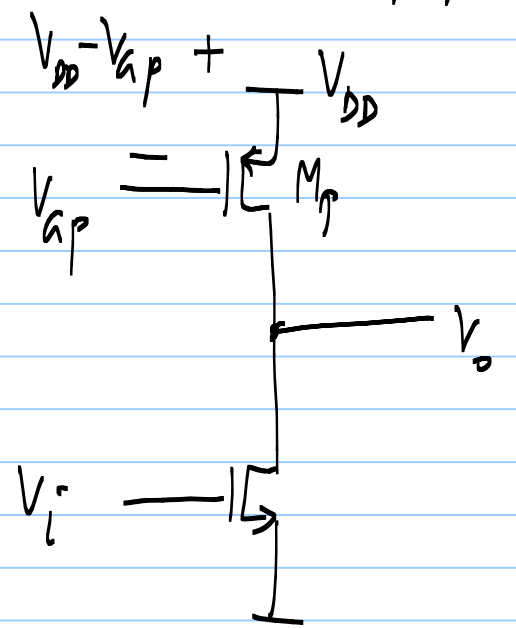
output = 1, I = 0,
no power dissipation

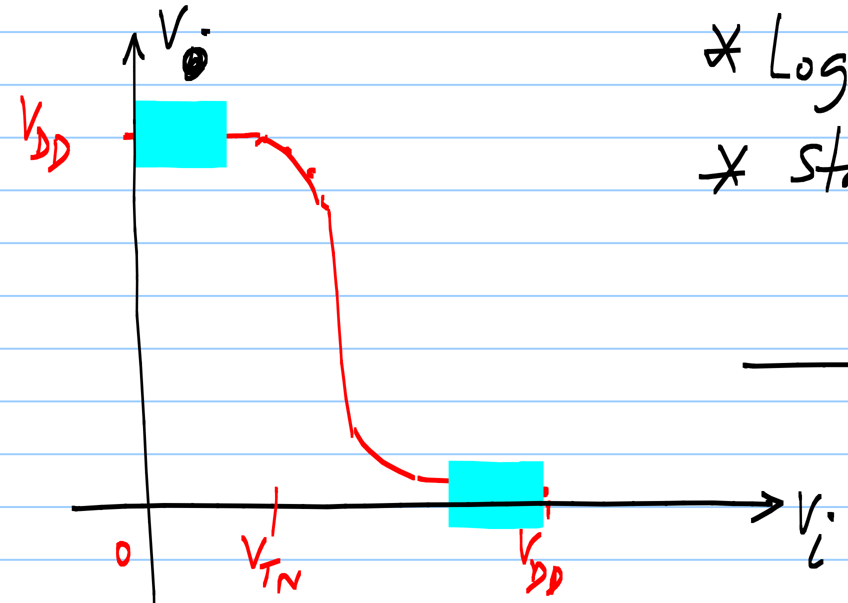
$$\frac{\mu_n C_{ox}}{2} \frac{W_N}{L_N} \left(V_{GN} - V_{TN}\right)^2 = I_{SAT}$$

faster than pMOS ($\mu_n > \mu_p$)

nMOS logic

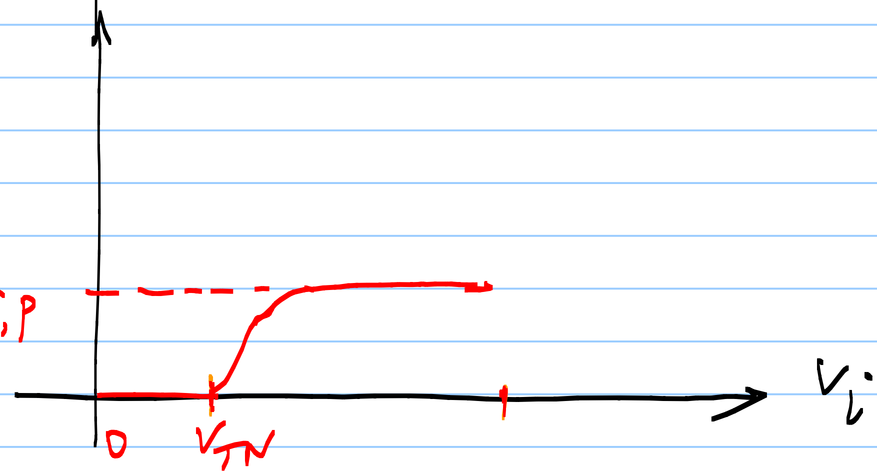
nMOS CS amplifier w/ pMOS load



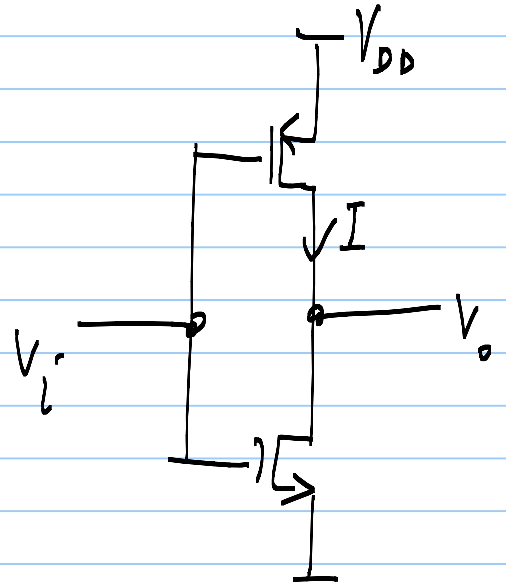


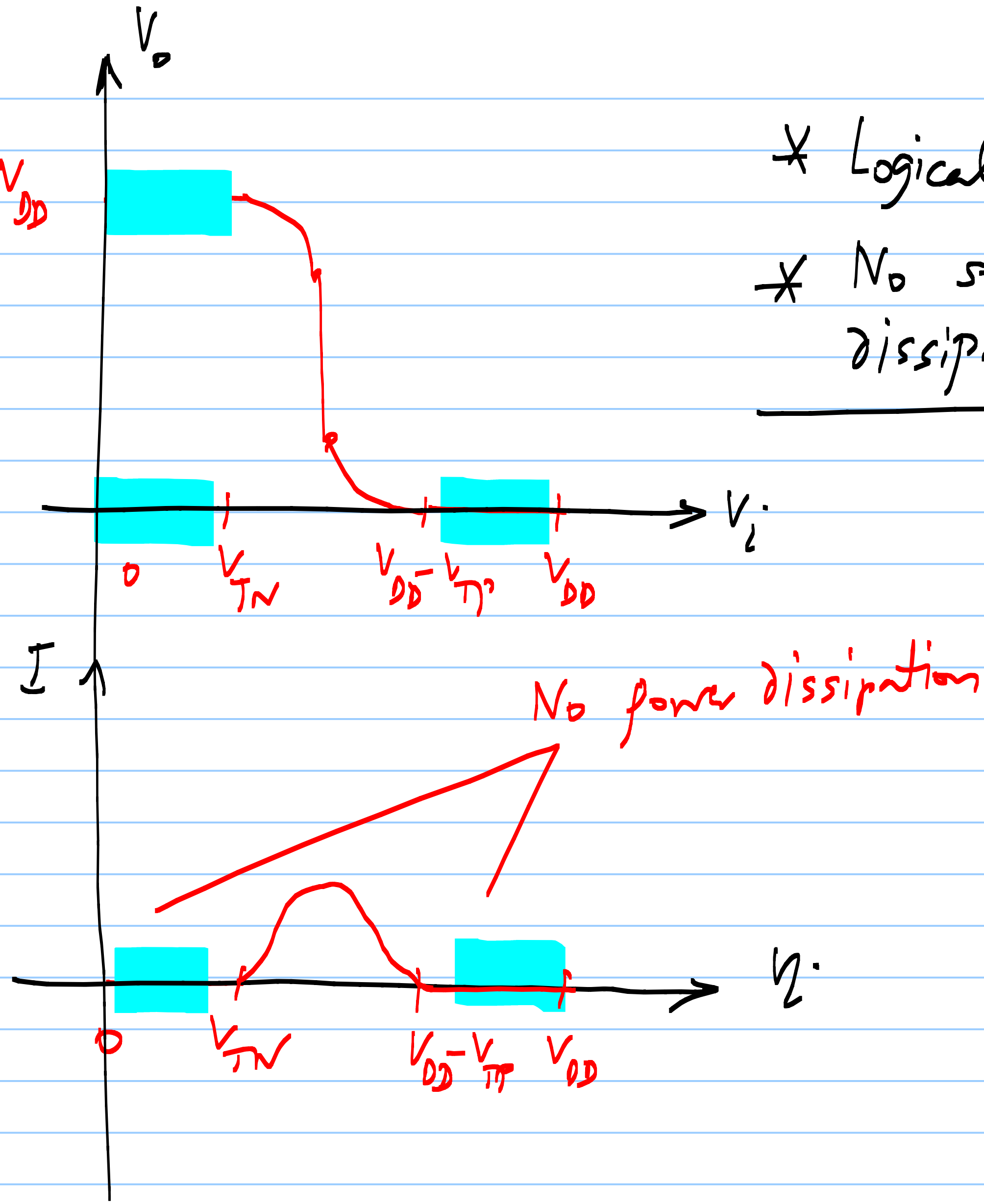
* Logical inverter
* Static power dissipation (output : LO (0))

$$\frac{\mu_p C_{ox}}{2} \frac{W_p}{L_p} \left(V_{DD} - V_{Gp} - V_{Tp}\right)^2 = I_{SAT,p}$$



CMOS inverter



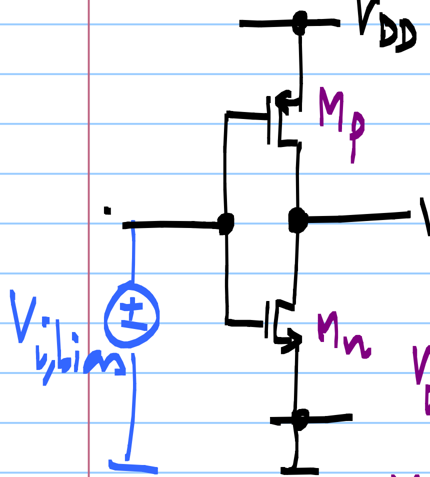


* Logical inverter
* No static power dissipation

Note Title 9/24/2018

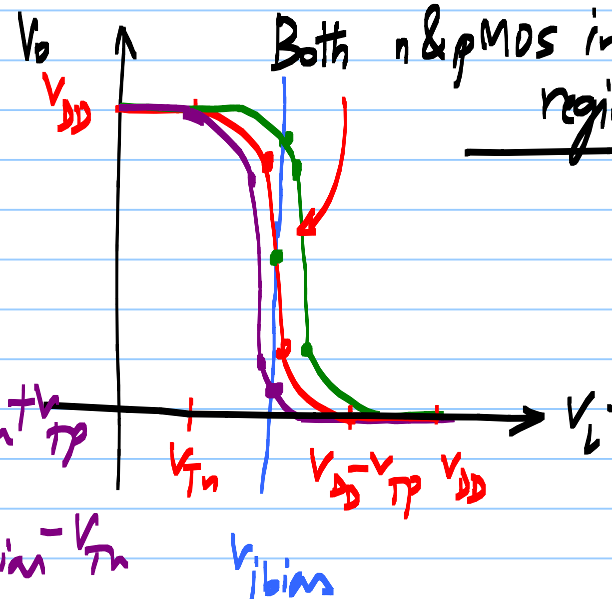
Biasing a CMOS inverter in the high gain region

$$\underbrace{\frac{g_{mn}+g_{mp}}{g_{dsn}+g_{dsp}}}$$

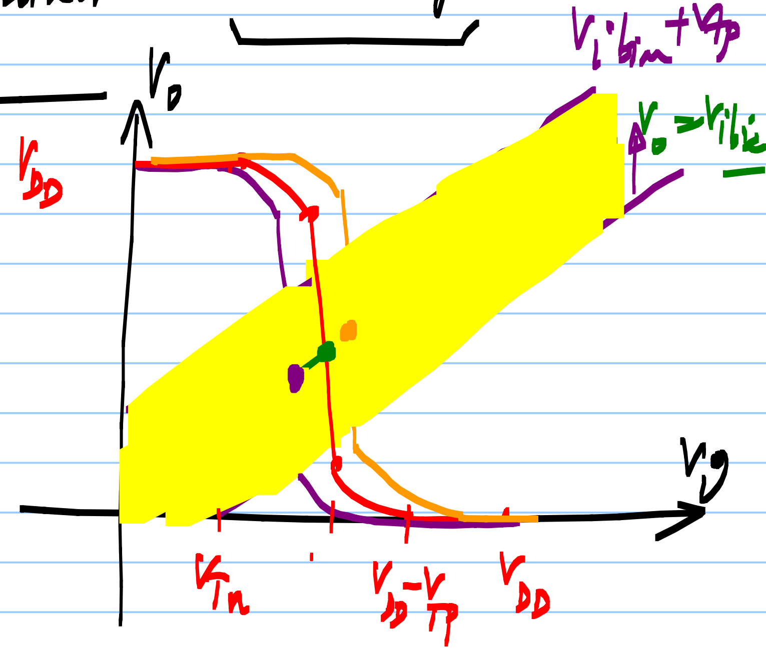


$V_o < V_{i,bias} + V_{Tp}$

$V_o > V_{i,bias} - V_{Tn}$

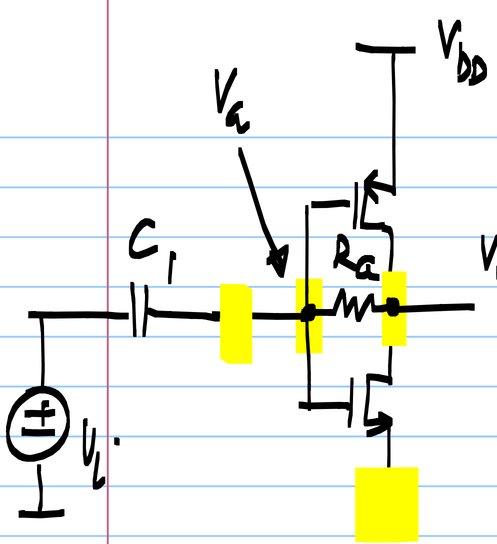


Both n&pMOS in saturation region



M_n saturation : $V_{i,bias} - V_o < V_{Tn}$ $\quad [V_{Tn} > 0]$

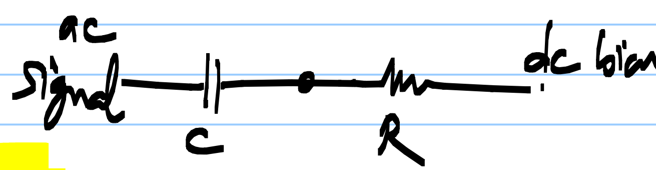
M_p saturation : $V_o - V_{i,bias} < V_{Tp}$ $\quad [V_{Tp} > 0]$



R_a must be large
C_1 must be large

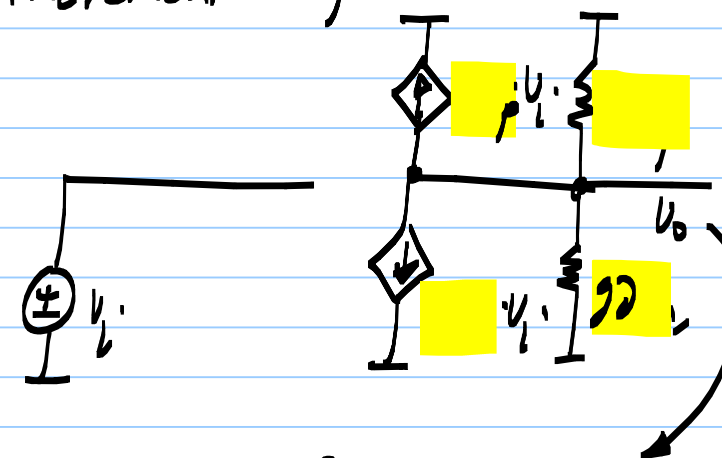
@ dc, $V_a = V_o$

@ ac, $v_a = v_i$



R_a is large enough to be treated as an open circuit

Incremental picture

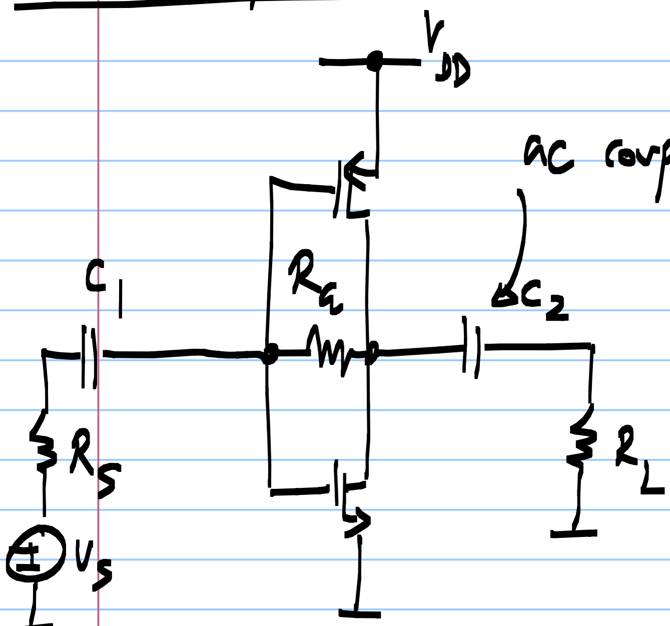


$$\frac{v_o}{v_i} = -\frac{g_{mn} + g_{mp}}{g_{dsn} + g_{dsp}}$$

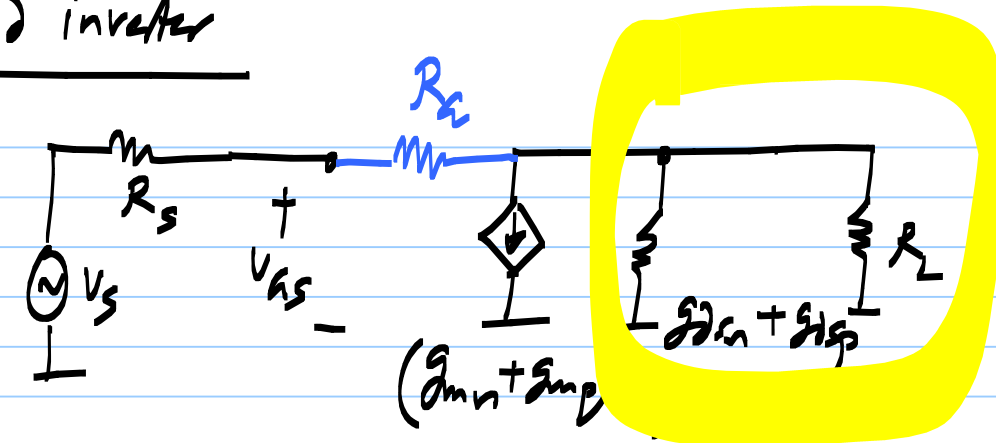
For dc bias : $V_{i,bias}$ =

Incremental signals, , the input voltage

CS amplifier using a self-biased inverter



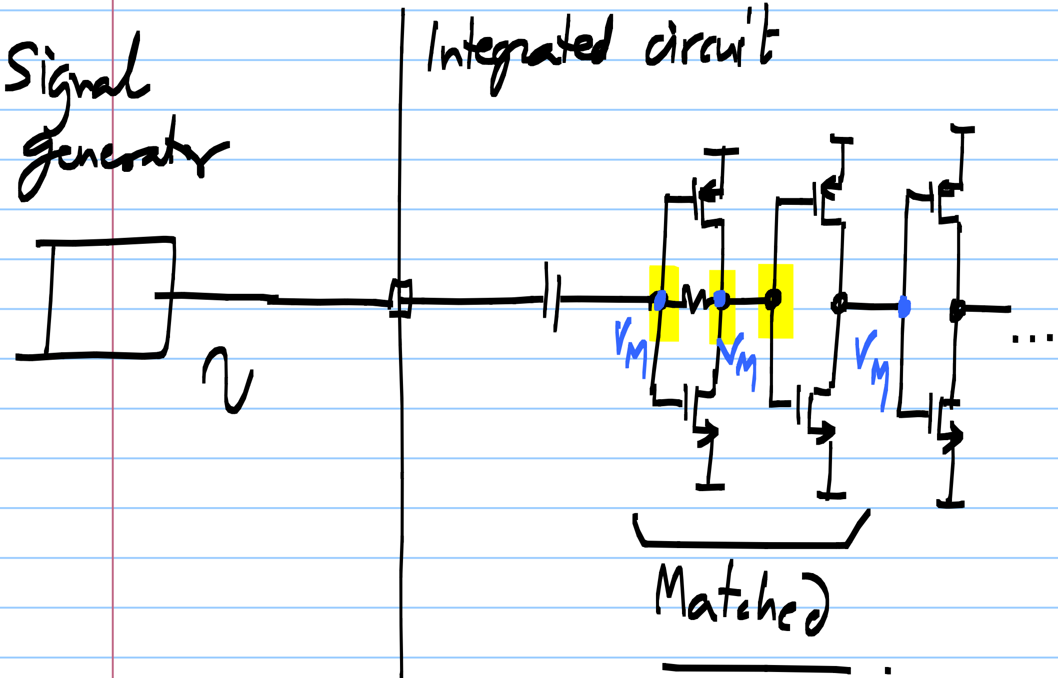
Self-biased inverter

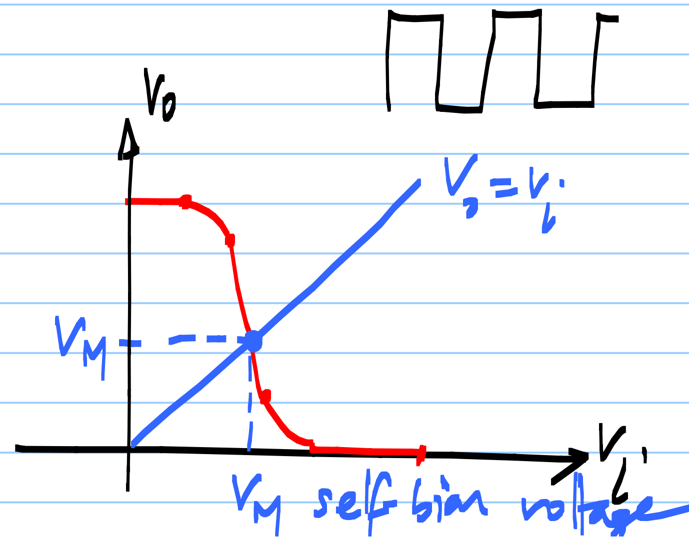


$$R_G \gg g_m R_L R_S \quad \text{OR} \quad R_L$$

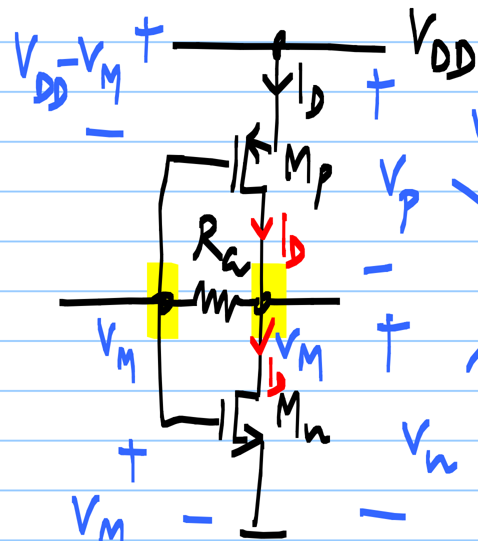
$$R_G \gg \frac{g_m R_S}{[g_{ds_n} + g_{ds_p} + G_L]} \; ; \quad R_G \gg \frac{1}{g_{ds_n} + g_{ds_p} + G_L}$$

Application of CS amplifier using a self-biased inverter

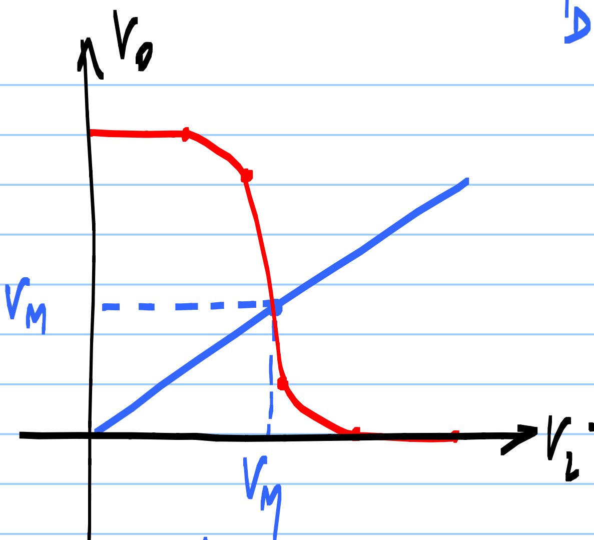




Self-biased inverter



nonlinear voltage divider



$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W_n}{L_n} (V_M - V_{Tn})^2$$

$$= \frac{\mu_p C_{ox}}{2} \cdot \frac{W_p}{L_p} (V_{DD} - V_M - V_{Tp})^2$$

$$V_M - V_{Tn} = \underbrace{\sqrt{\frac{\mu_p}{\mu_n} \cdot \frac{W_p/L_p}{W_n/L_n}}}_{\alpha} \cdot (V_{DD} - V_M - V_{Tp})$$

$$V_M = \frac{\alpha \cdot V_{DD} + V_{Tn} - \alpha V_{Tp}}{1+\alpha}$$

$$\alpha = 1$$

$$\left[\frac{V_{DD}}{2}\right]$$

$$I_D = \frac{\mu_n C_{ox}}{2} \cdot \frac{W_n}{L_n} \left(\frac{\alpha V_{DD} + V_{Tn} - \alpha V_{Tp}}{1+\alpha} - V_{Tn} \right)^2$$

$$= \frac{\mu_n C_{ox}}{2} \cdot \frac{W_n}{L_n} \left[\frac{\alpha \left(V_{DD} - V_{Tp} - V_{Tn}\right)}{1+\alpha} \right]^2$$

$$= \frac{\mu_n C_{ox}}{2} \cdot \frac{W_n}{L_n} \left(\frac{\alpha}{1+\alpha} \right)^2 \cdot \left(V_{DD} - V_{Tp} - V_{Tn} \right)^2$$

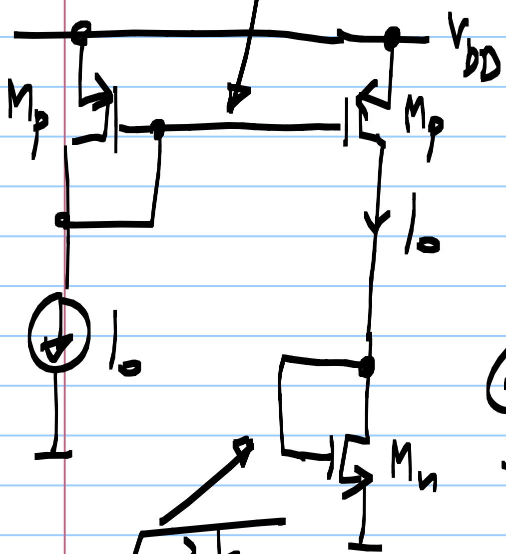
$$\alpha = \sqrt{\frac{\mu_p \cdot W_p / L_p}{}}$$

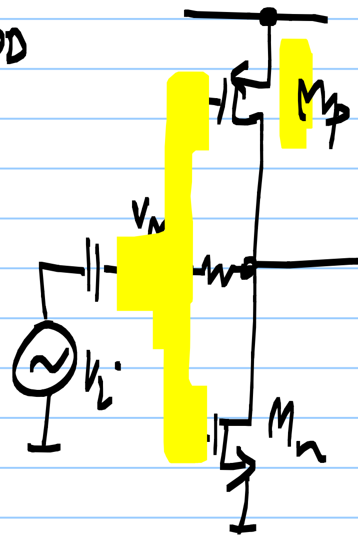
Current drawn from the supply is strongly dependent on V_{DD}

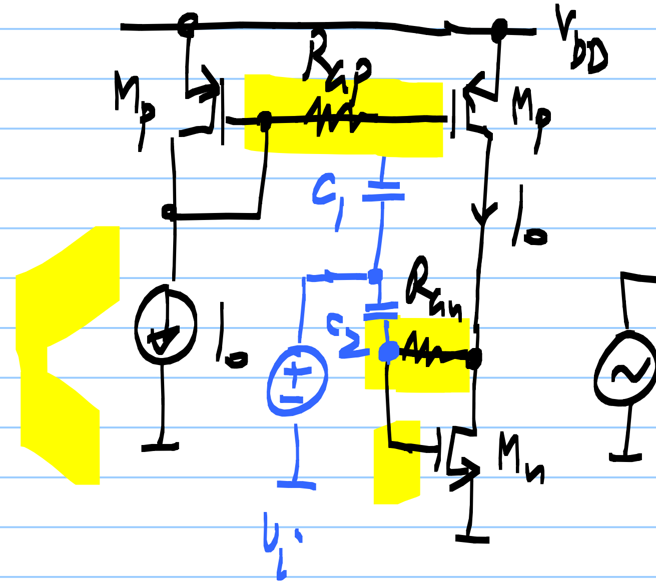
Calculate g_{mn}, g_{mp}

Increase with V_{DD}

$$V_{DD} - V_{Tp} - \sqrt{\frac{2I_0}{\mu_p C_{ox} W_p/L_p}}$$







$$V_{Tn} + \sqrt{\frac{2I_0}{\mu_n C_{ox} W_n/L_n}}$$

M_p, M_n : biased @ I_0