

Other Important Instructions

- ADC <reg>: Add register to accumulator with carry
- CMC: Complement carry
- DAA: Decimal adjust accumulator. Acc. content changed from 8-bit binary to two 4-bit BCD digits. If (D3-D0) > 9, add 6.
- DAD <reg_pair>: Add register pair to HL
- IN <port>: Get data from port
- LHLD <addr> : $L \leftarrow \text{Mem}[\text{addr}]$, $H \leftarrow \text{Mem}[\text{addr} + 1]$
- SHLD <addr>
- PCHL : $PC \leftarrow HL$
- SPHL : $SP \leftarrow HL$
- XCHG : Exchange HL with DE
- XTHL: Exchange HL with top of stack

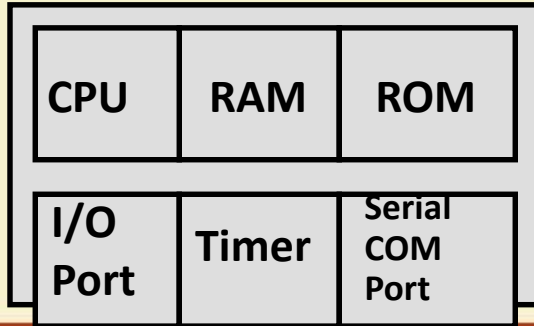
The 8051 Microcontroller

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Electronics and Electrical Communication Engineering

8051 Basic Component

- 4K bytes internal **ROM**
- 128 bytes internal **RAM**
- Four 8-bit **I/O ports** (P0 - P3).
- Two 16-bit **timers**/counters
- One **serial** interface

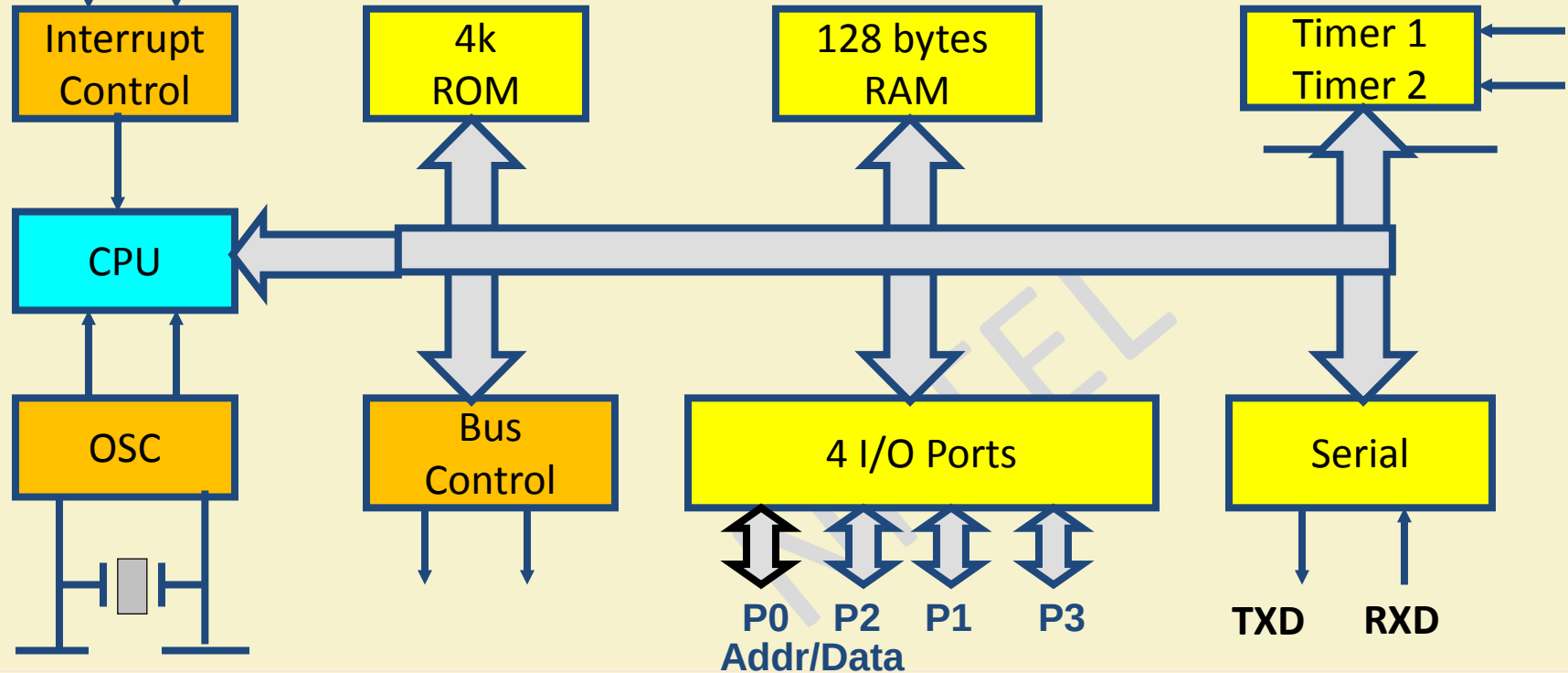


← A single chip
Microcontroller



Block Diagram

External Interrupts

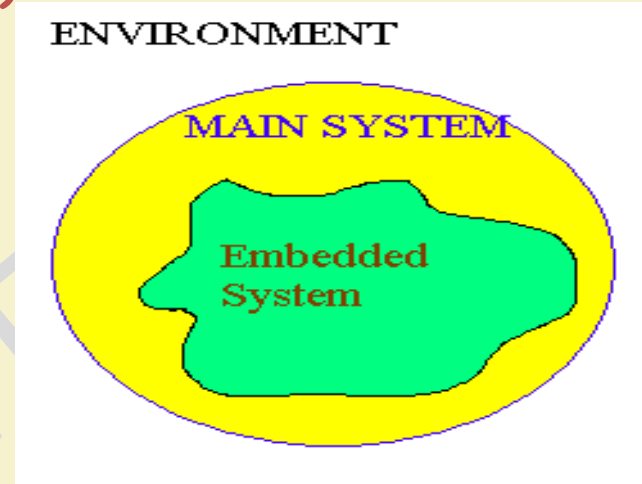


Other 8051 featurrs

- Only 1 On chip oscillator (external crystal)
- 6 interrupt sources (2 external , 3 internal, Reset)
- 64K external code (program) memory(only read)PSEN
- 64K external data memory(can be read and write) by RD,WR
- Code memory is selectable by EA (internal or external)
- We may have External memory as data and code

Embedded System (8051 Application)

- What is Embedded System?
 - An embedded system is closely integrated with the main system
 - It may not interact directly with the environment
 - For example – A microcomputer in a car ignition control
 - ❖ An embedded product uses a microprocessor or microcontroller to **do one task** only
 - ❖ There is only one application software that is typically **burnt into ROM**



Examples of Embedded Systems

- Keyboard
- Printer
- video game player
- MP3 music players
- Embedded memories to keep configuration information
- Mobile phone units
- Domestic (home) appliances
- Data switches
- Automotive controls

Three criteria in Choosing a Microcontroller

- meeting the computing needs of the task efficiently and cost effectively
 - speed, the amount of ROM and RAM, the number of I/O ports and timers, size, packaging, power consumption
 - easy to upgrade
 - cost per unit
- availability of software development tools
 - assemblers, debuggers, C compilers, emulator, simulator, technical support
- wide availability and reliable sources of the microcontrollers

Comparison of the 8051 Family Members

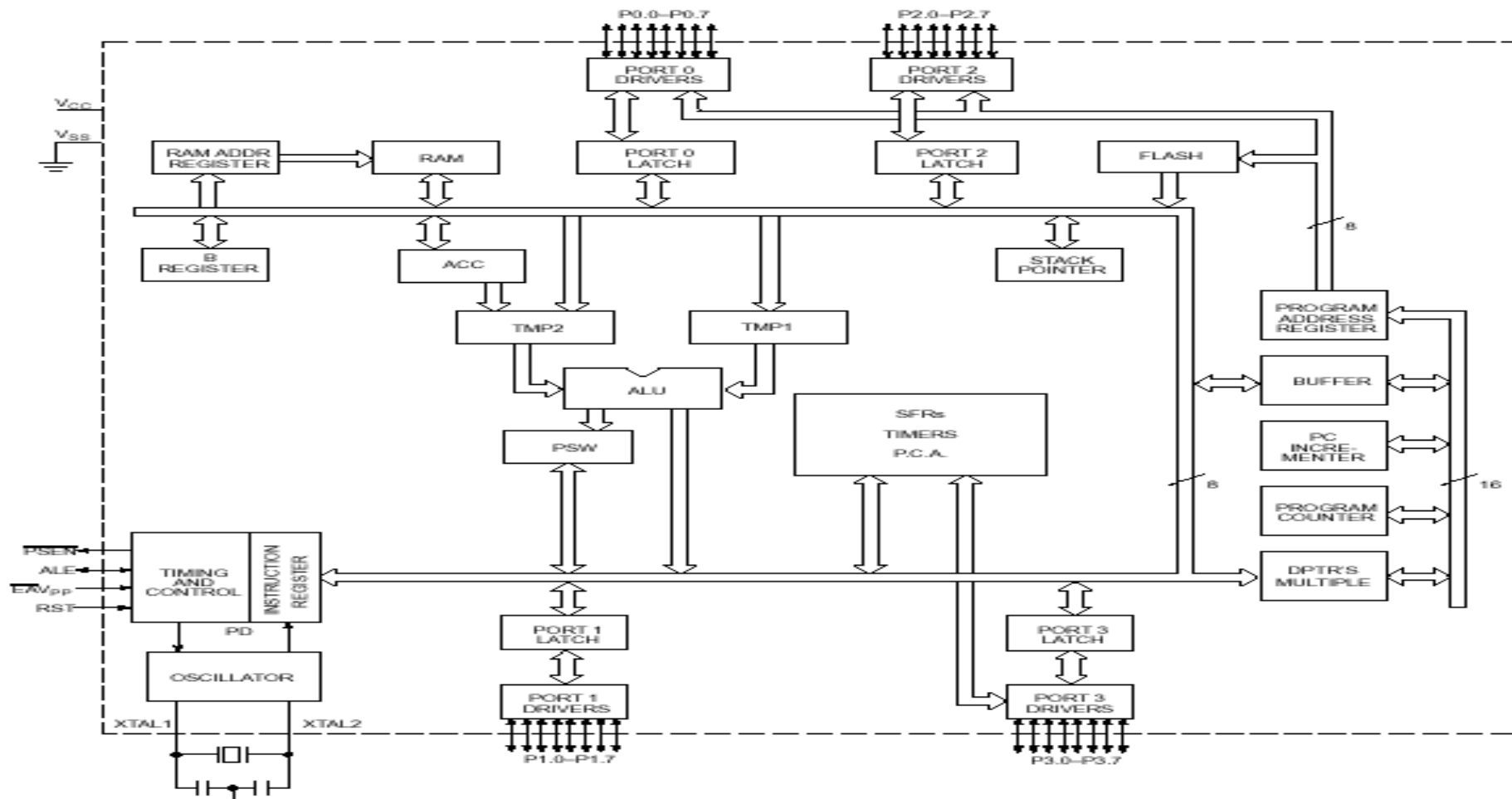
- ROM type
 - 8031 no ROM
 - 80xx mask ROM
 - 87xx EPROM
 - 89xx Flash EEPROM
- 89xx
 - 8951
 - 8952
 - 8953
 - 8955
 - 898252
 - 891051
 - 892051
- Example (AT89C51,AT89LV51,AT89S51)
 - AT= ATMEL(Manufacture)
 - C = CMOS technology
 - LV= Low Power(3.0v)

Comparison of the 8051 Family Members

89XX	ROM	RAM	Timer	Int Source	IO pin	Other
8951	4k	128	2	6	32	-
8952	8k	256	3	8	32	-
8953	12k	256	3	9	32	WD
8955	20k	256	3	8	32	WD
898252	8k	256	3	9	32	ISP
891051	1k	64	1	3	16	AC
892051	2k	128	2	6	16	AC

WD: Watch Dog Timer
AC: Analog Comparator
ISP: In System Programmable

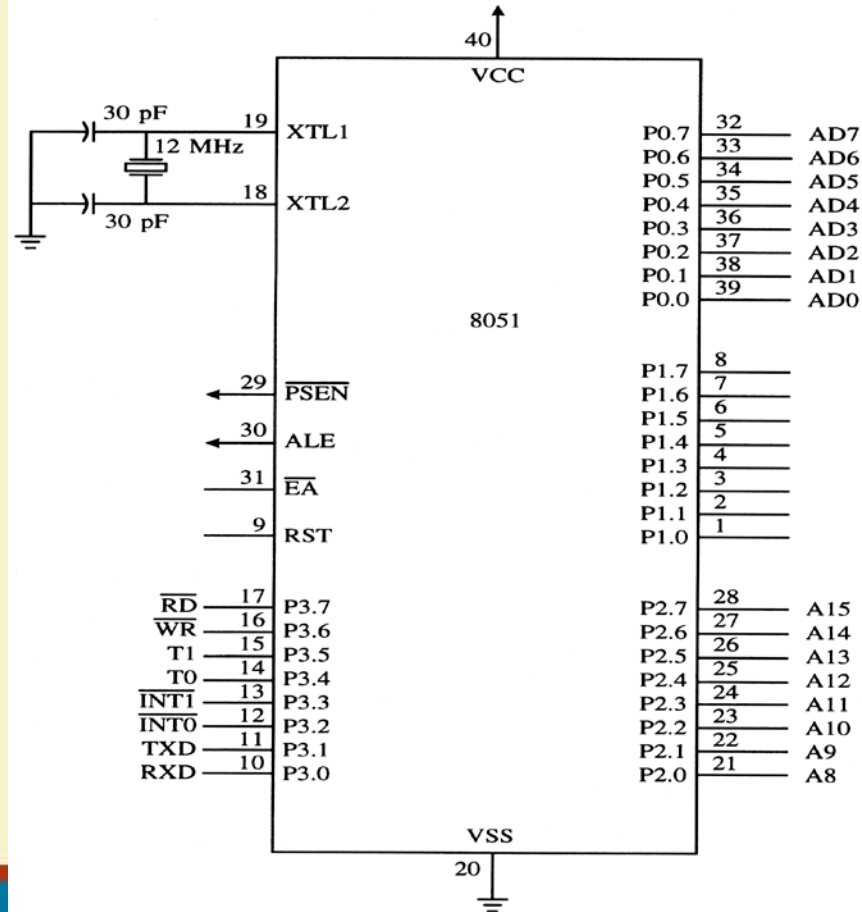
8051 Internal Block Diagram



8051

Schematic

Pin out

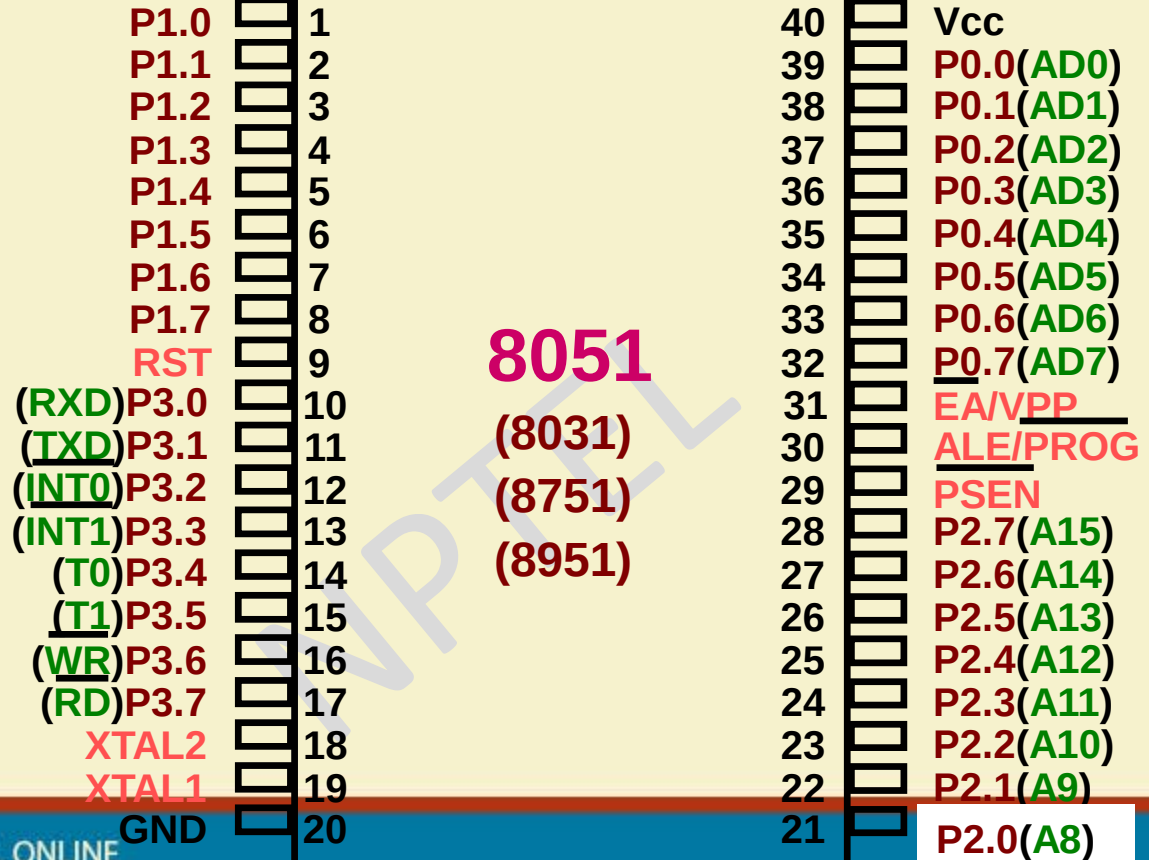


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8051 Foot Print



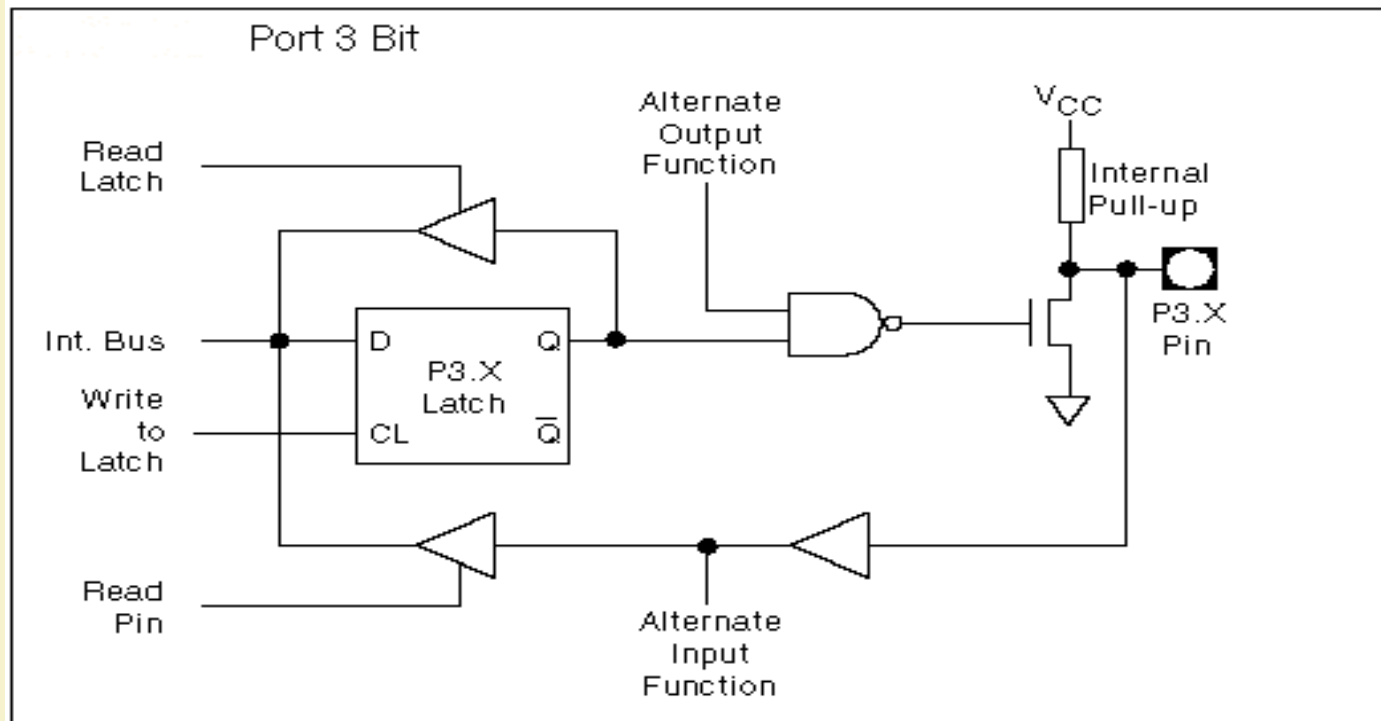
IMPORTANT PINS (IO Ports)

- One of the most useful features of the 8051 is that it contains four I/O ports (P0 - P3)
- Port 0 (pins 32-39) : P0 (P0.0~P0.7)
 - 8-bit R/W - General Purpose I/O
 - Or acts as a multiplexed low byte address and data bus for external memory design
- Port 1 (pins 1-8) : P1 (P1.0~P1.7)
 - Only 8-bit R/W - General Purpose I/O
- Port 2 (pins 21-28) : P2 (P2.0~P2.7)
 - 8-bit R/W - General Purpose I/O
 - Or high byte of the address bus for external memory design
- Port 3 (pins 10-17) : P3 (P3.0~P3.7)
 - General Purpose I/O
 - if not using any of the internal peripherals (timers) or external interrupts.
- Each port can be used as input or output (bi-direction)

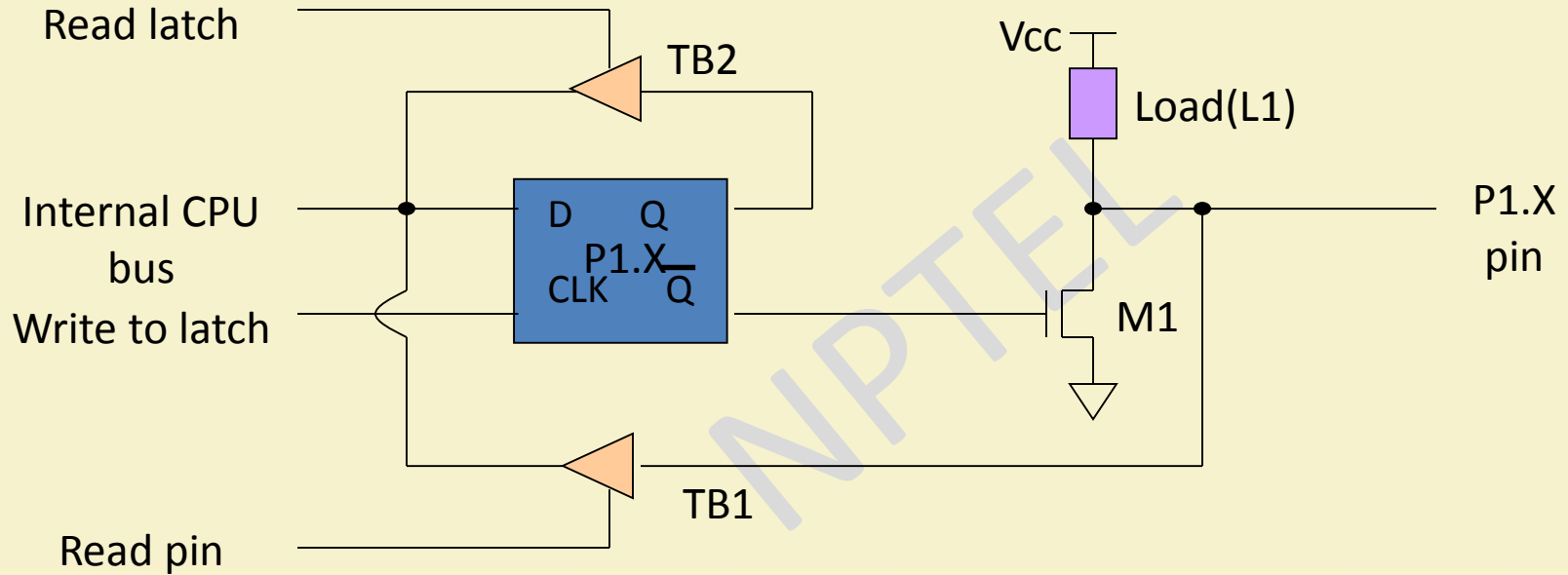
Port 3 Alternate Functions

Port Pin	Alternate Function
P3.0	RXD (serial input port)
P3.1	TXD (serial output port)
P3.2	$\overline{\text{INT0}}$ (external interrupt 0)
P3.3	$\overline{\text{INT1}}$ (external interrupt 1)
P3.4	T0 (Timer 0 external input)
P3.5	T1 (Timer 1 external input)
P3.6	$\overline{\text{WR}}$ (external data memory write strobe)
P3.7	$\overline{\text{RD}}$ (external data memory read strobe)

8051 Port 3 Bit Latches and I/O Buffers



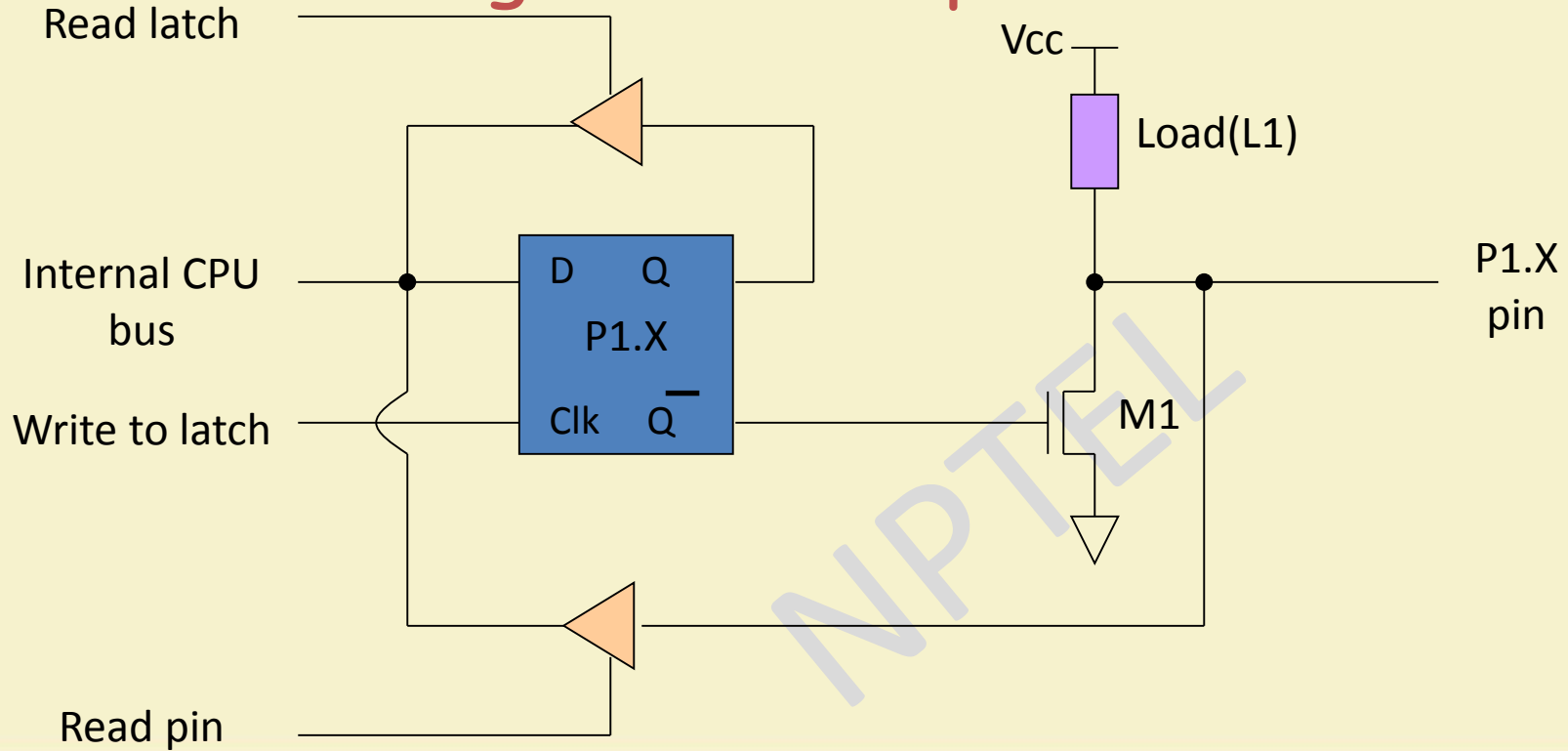
Hardware Structure of I/O Pin



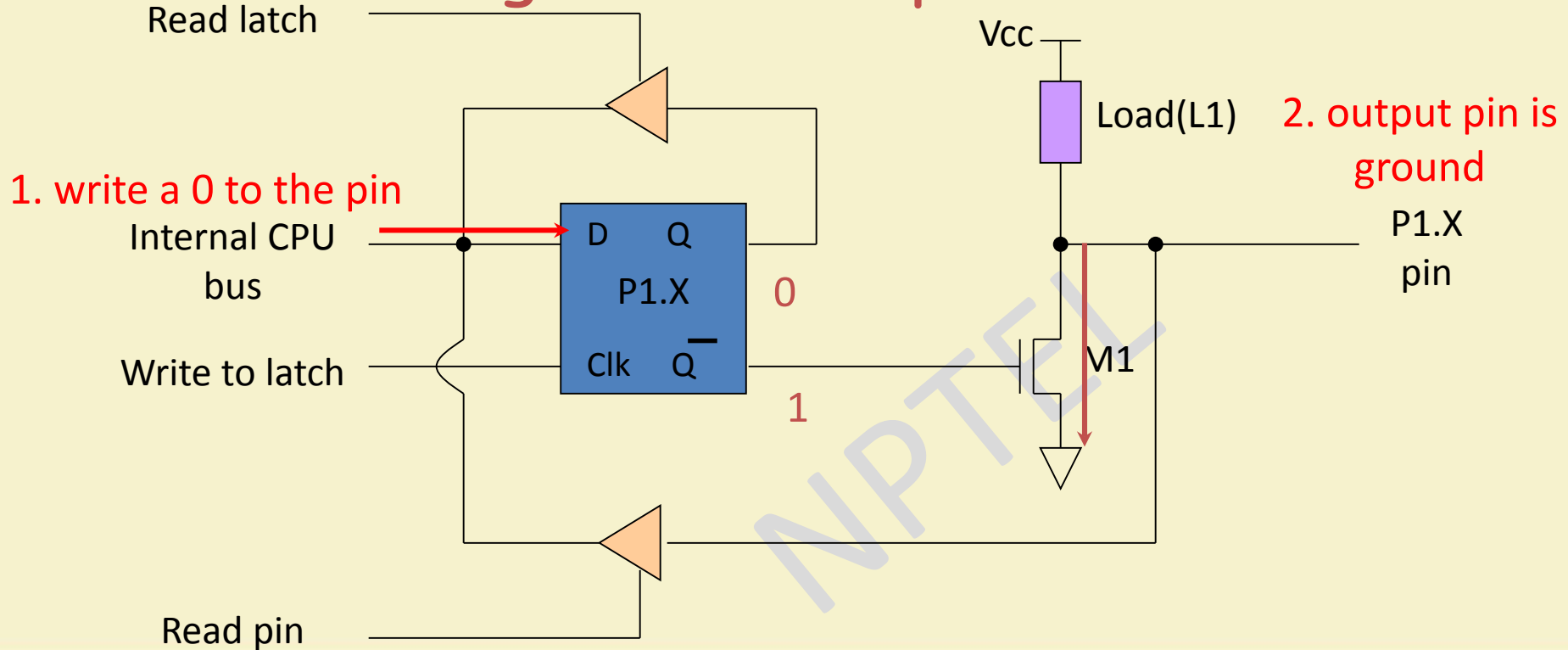
Hardware Structure of I/O Pin

- Each pin of I/O ports
 - Internally connected to CPU bus
 - A **D latch** store the value of this pin
 - Write to latch = 1 : write data into the D latch
 - 2 **Tri-state** buffer :
 - TB1: controlled by “Read pin”
 - Read pin = 1 : really read the data present at the pin
 - TB2: controlled by “Read latch”
 - Read latch = 1 : read value from internal latch
 - A **transistor** M1 gate
 - Gate=0: open
 - Gate=1: close

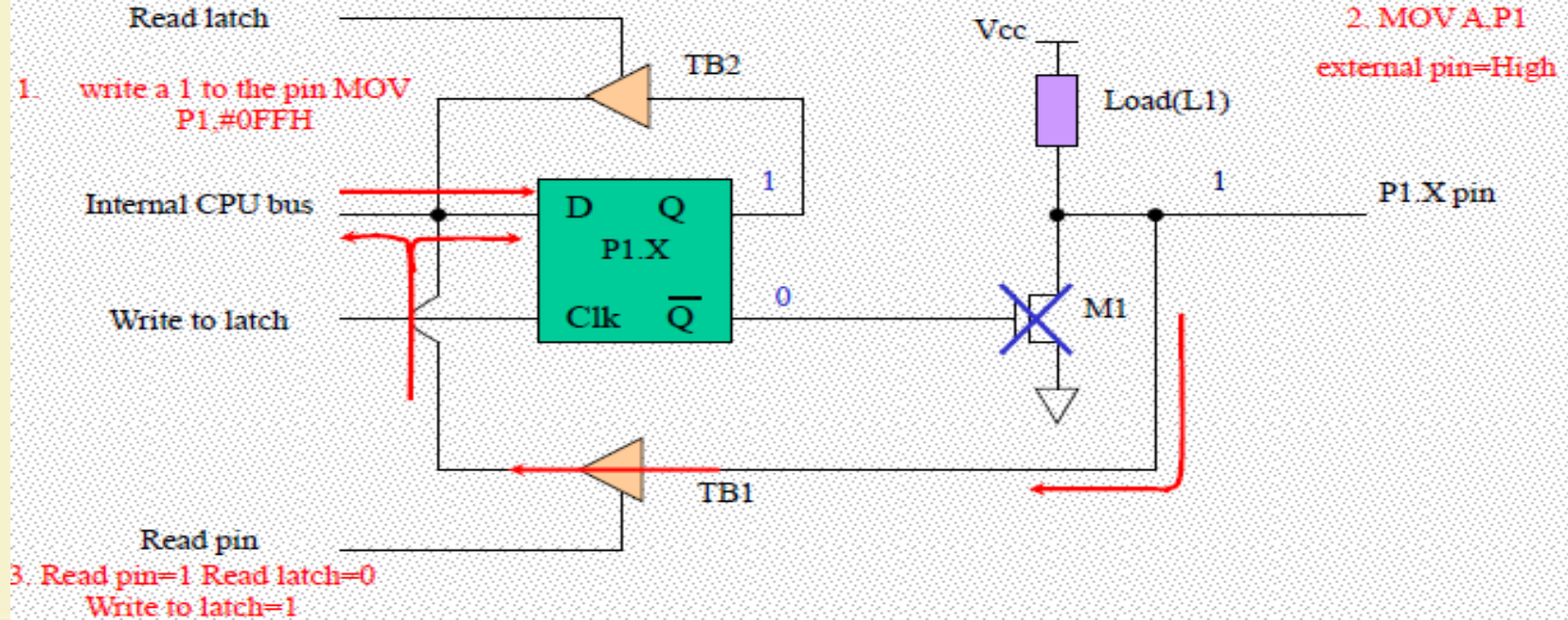
Writing "1" to Output Pin P1.X



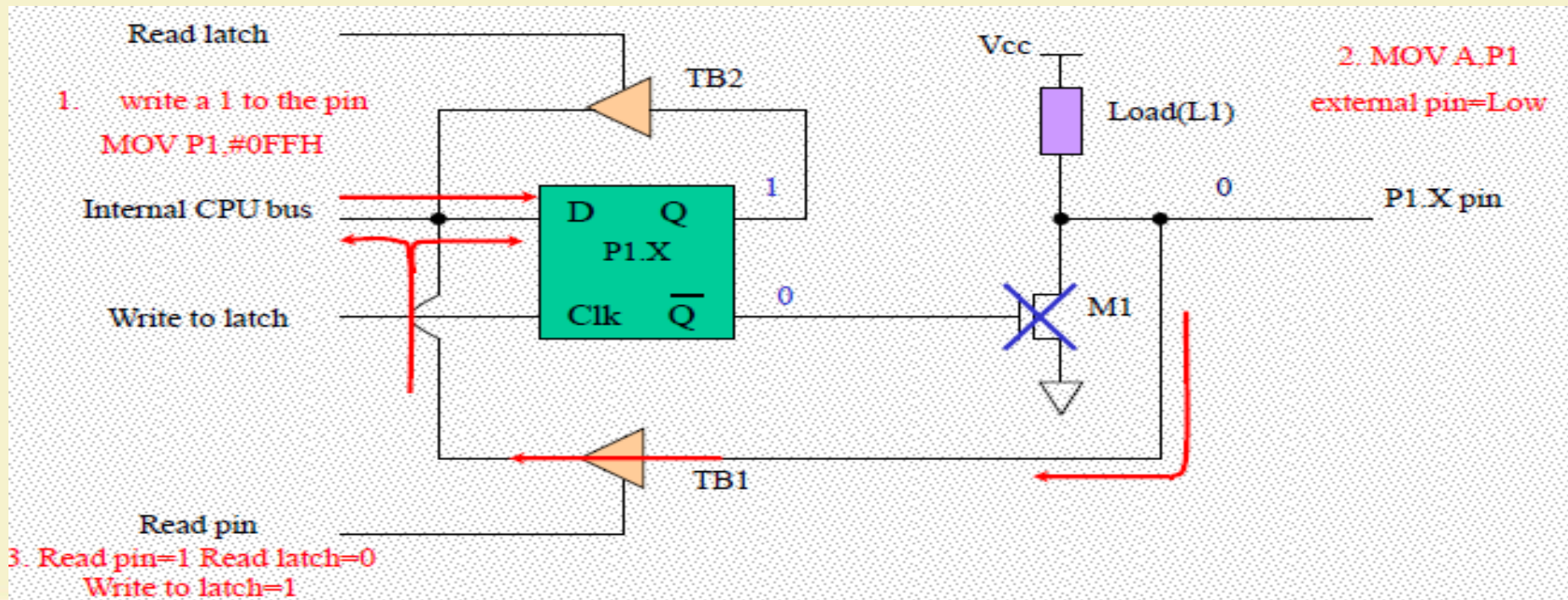
Writing "0" to Output Pin P1.X



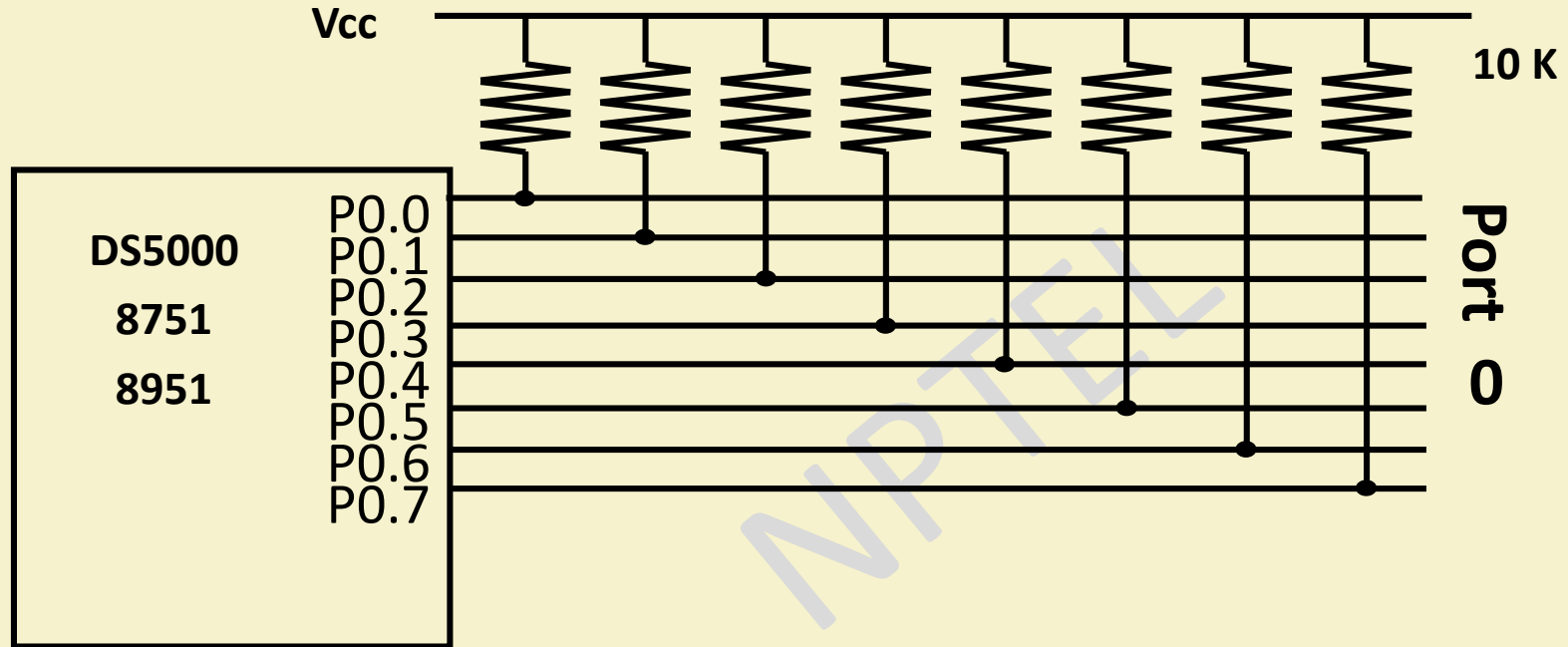
Reading "High" at Input Pin



Reading "Low" at Input Pin



Port 0 with Pull-Up Resistors



IMPORTANT PINS

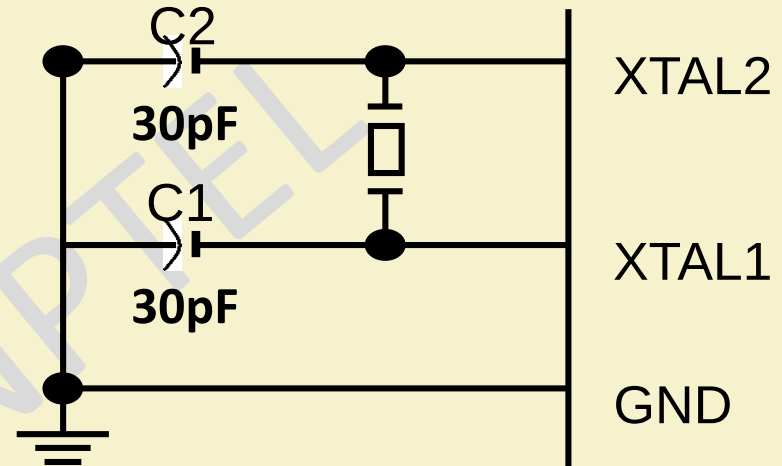
- **PSEN** (out): **P**rogram **S**tore **E**nable, the read signal for external program memory (active low).
- **ALE** (out): **A**ddress **L**atch **E**nable, to latch address outputs at Port0 and Port2
- **EA** (in): **E**xternal **A**ccess Enable, active low to access external program memory locations 0 to 4K
- **RXD, TXD**: UART pins for serial I/O on Port 3
- **XTAL1 & XTAL2**: Crystal inputs for internal oscillator.

Pins of 8051

- Vcc (pin 40) :
 - Vcc provides supply voltage to the chip.
 - The voltage source is +5V.
- GND (pin 20) : ground
- XTAL1 and XTAL2 (pins 19,18) :
 - These 2 pins provide external clock.
 - Way 1 : using a quartz crystal oscillator
 - Way 2 : using a TTL oscillator
 - Example 4-1 shows the relationship between XTAL and the machine cycle.

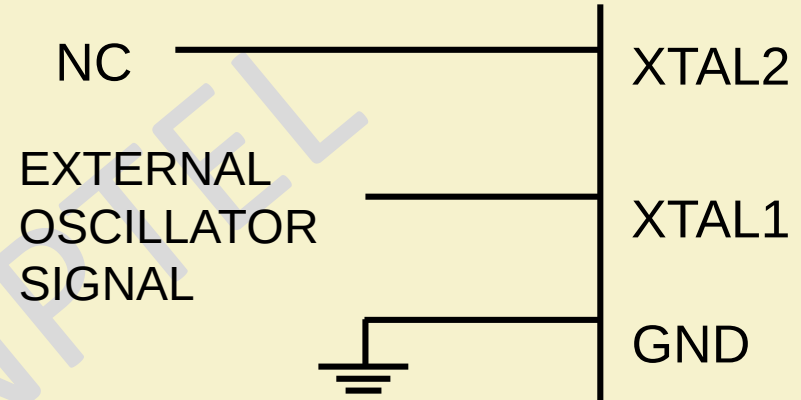
XTAL Connection to 8051

- Using a quartz crystal oscillator
- We can observe the frequency on the XTAL2 pin.



XTAL Connection to an External Clock Source

- Using a TTL oscillator
- XTAL2 is unconnected.



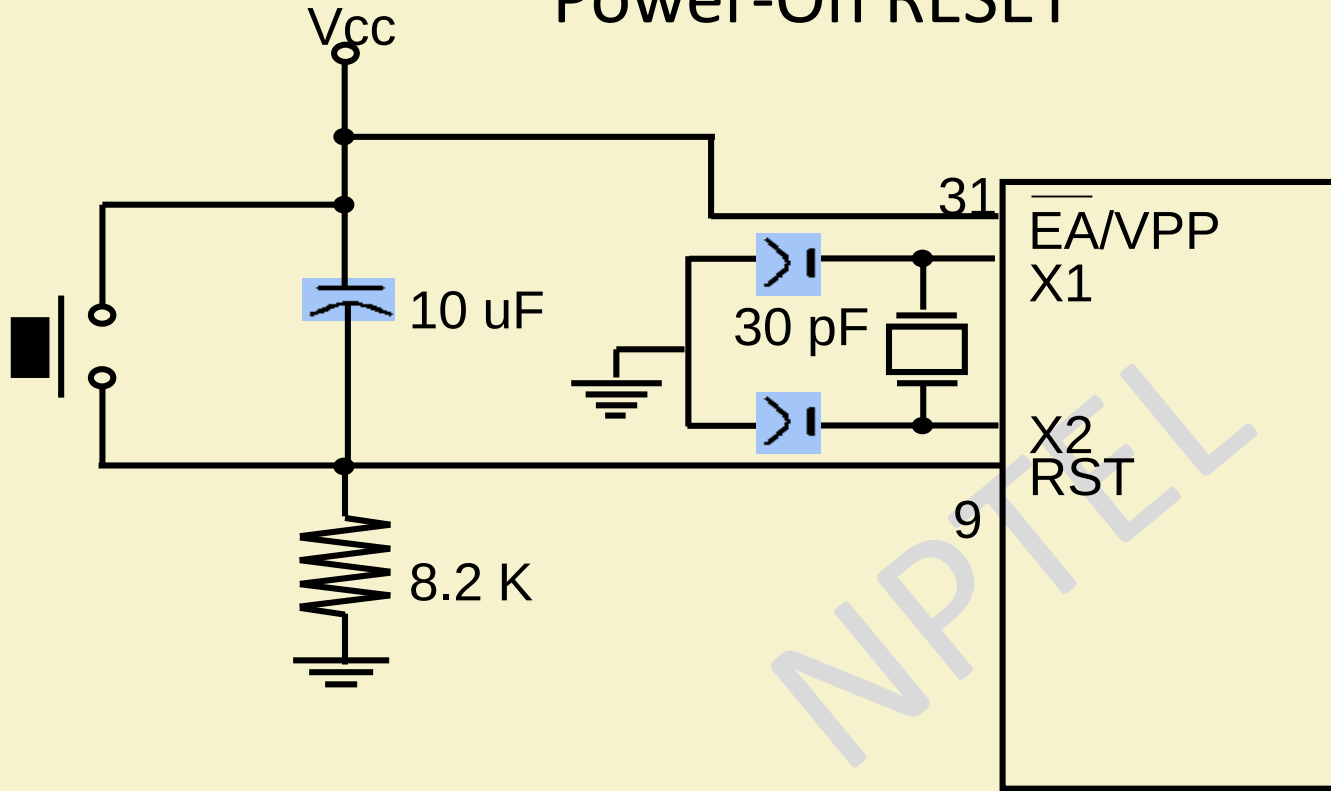
Machine cycle

- Find the machine cycle for
- (a) XTAL = 11.0592 MHz
- (b) XTAL = 16 MHz.
- **Solution:**
- (a) $11.0592 \text{ MHz} / 12 = 921.6 \text{ kHz}$;
- machine cycle = $1 / 921.6 \text{ kHz} = 1.085 \mu\text{s}$
- (b) $16 \text{ MHz} / 12 = 1.333 \text{ MHz}$;
- machine cycle = $1 / 1.333 \text{ MHz} = 0.75 \mu\text{s}$

Pins of 8051

- RST (pin 9) : reset
 - input pin and active high (normally low) .
 - The high pulse must be high at least 2 machine cycles.
 - power-on reset.
 - Upon applying a high pulse to RST, the microcontroller will reset and all values in registers will be lost.
 - Reset values of some 8051 registers
 - power-on reset circuit

Power-On RESET



RESET Value of Some 8051 Registers:

Register	Reset Value
PC	0000
ACC	0000
B	0000
PSW	0000
SP	0007
DPTR	0000
RAM are all zero	

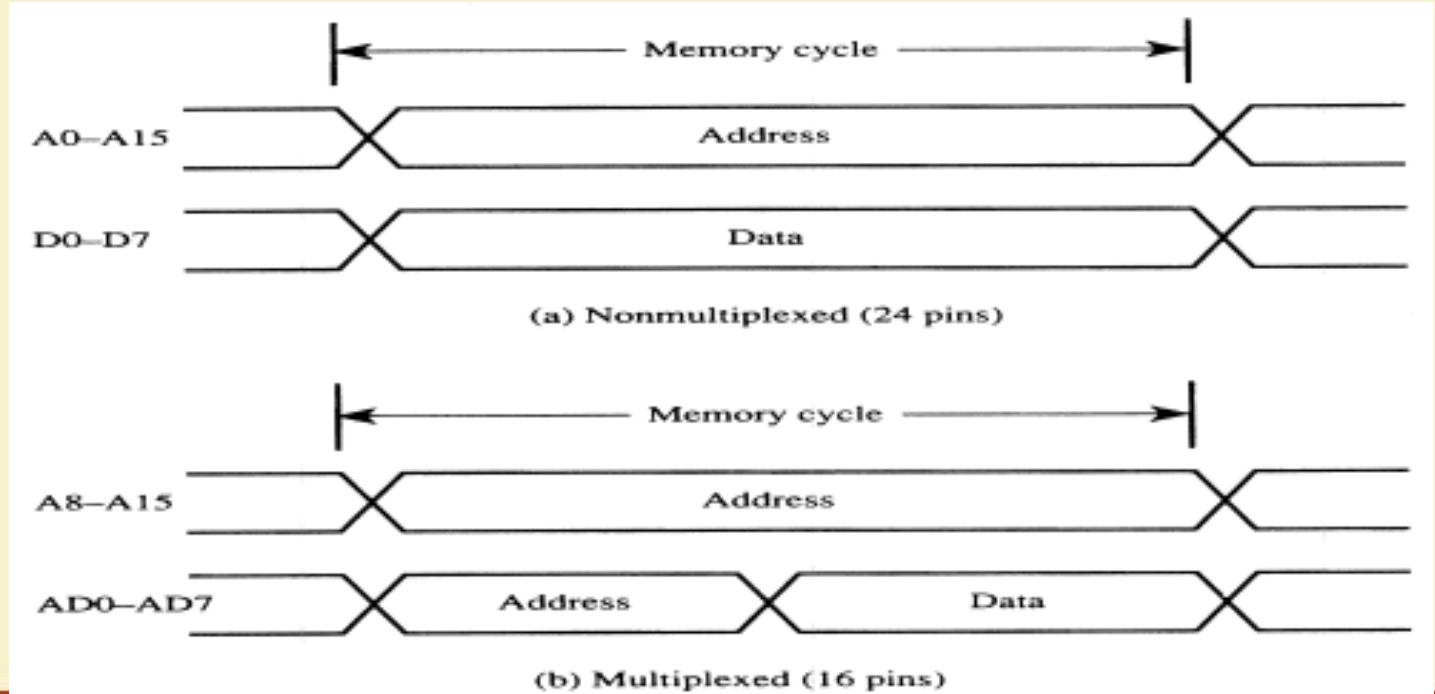
Pins of 8051

- /EA (pin 31) : external access
 - There is no on-chip ROM in 8031 and 8032 .
 - The /EA pin is connected to GND to indicate the code is stored externally.
 - /PSEN & ALE are used for external ROM.
 - For 8051, /EA pin is connected to Vcc.
 - “/” means active low.
- /PSEN (pin 29) : program store enable
 - This is an output pin and is connected to the OE pin of the ROM.

Pins of 8051

- ALE (pin 30) : address latch enable
 - It is an output pin and is active high.
 - 8051 port 0 provides both address and data.
 - The ALE pin is used for de-multiplexing the address and data by connecting to the G pin of the 74LS373 latch.

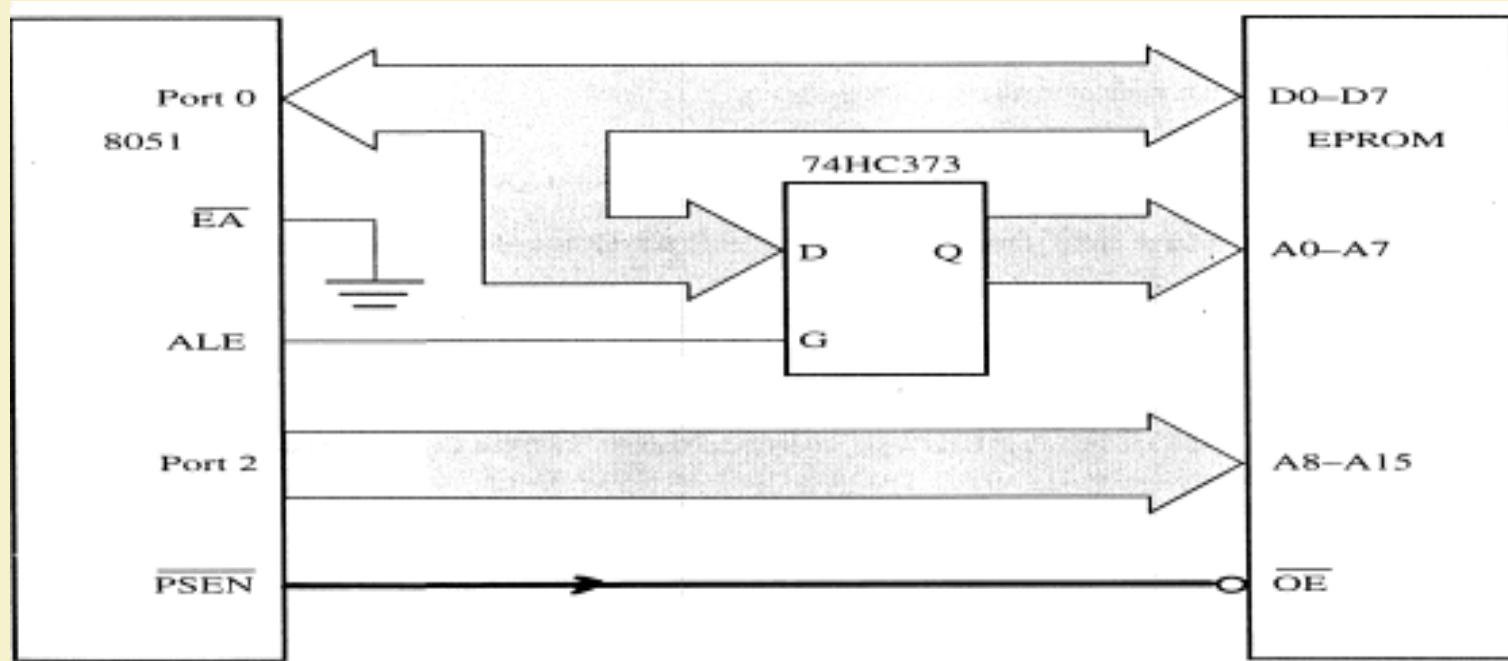
Address Multiplexing for External Memory



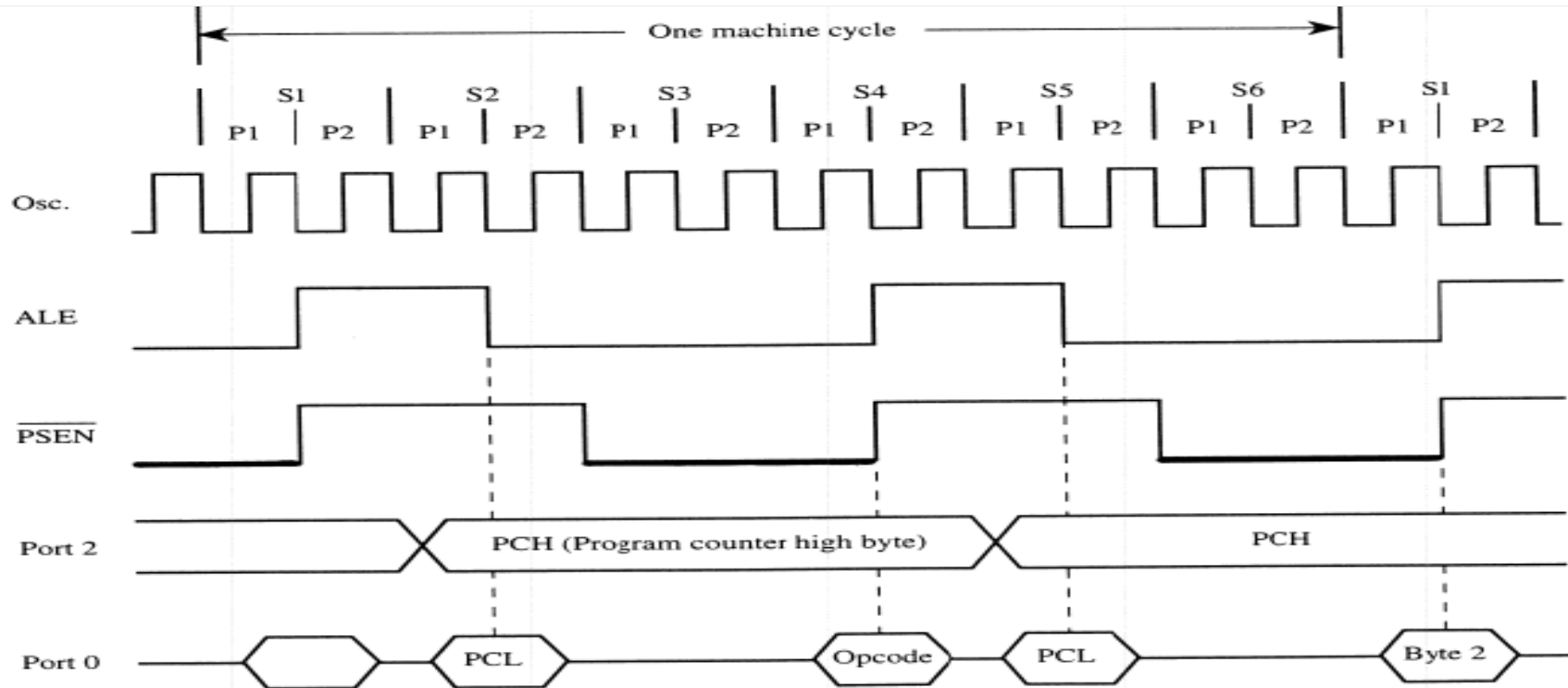
Multiplexing
the address
(low-byte)
and data
bus

Address Multiplexing for External Memory

Accessing
external
code
memory

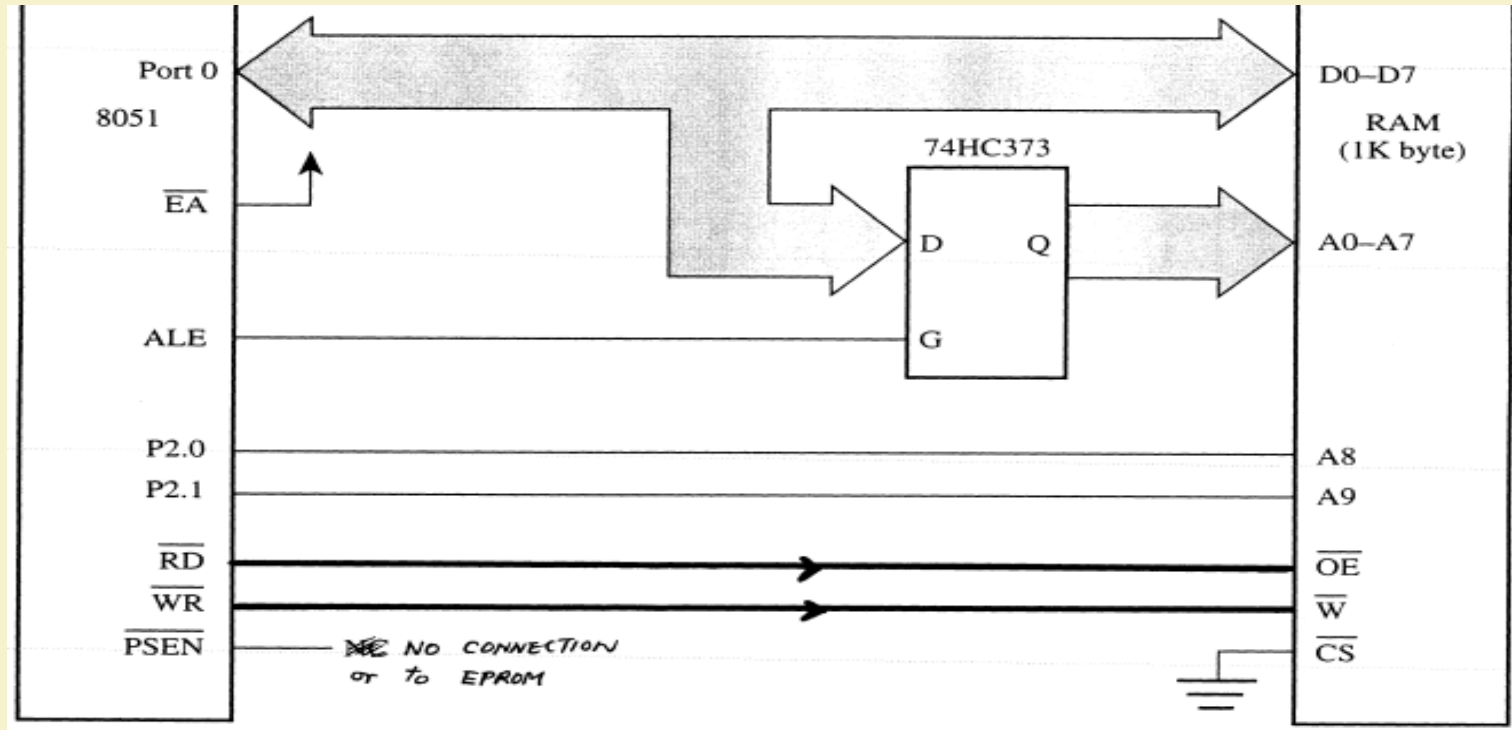


Read Timing for External Code Memory

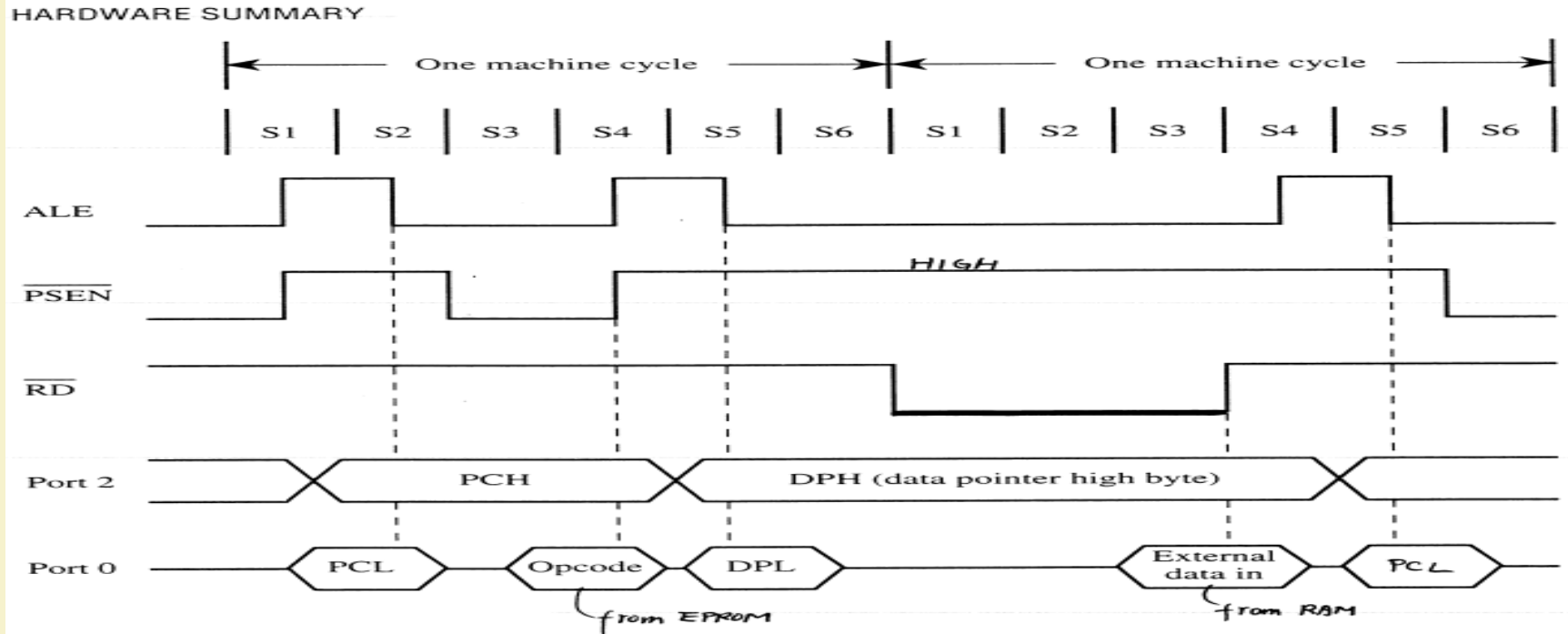


Accessing 1K External Data Memory

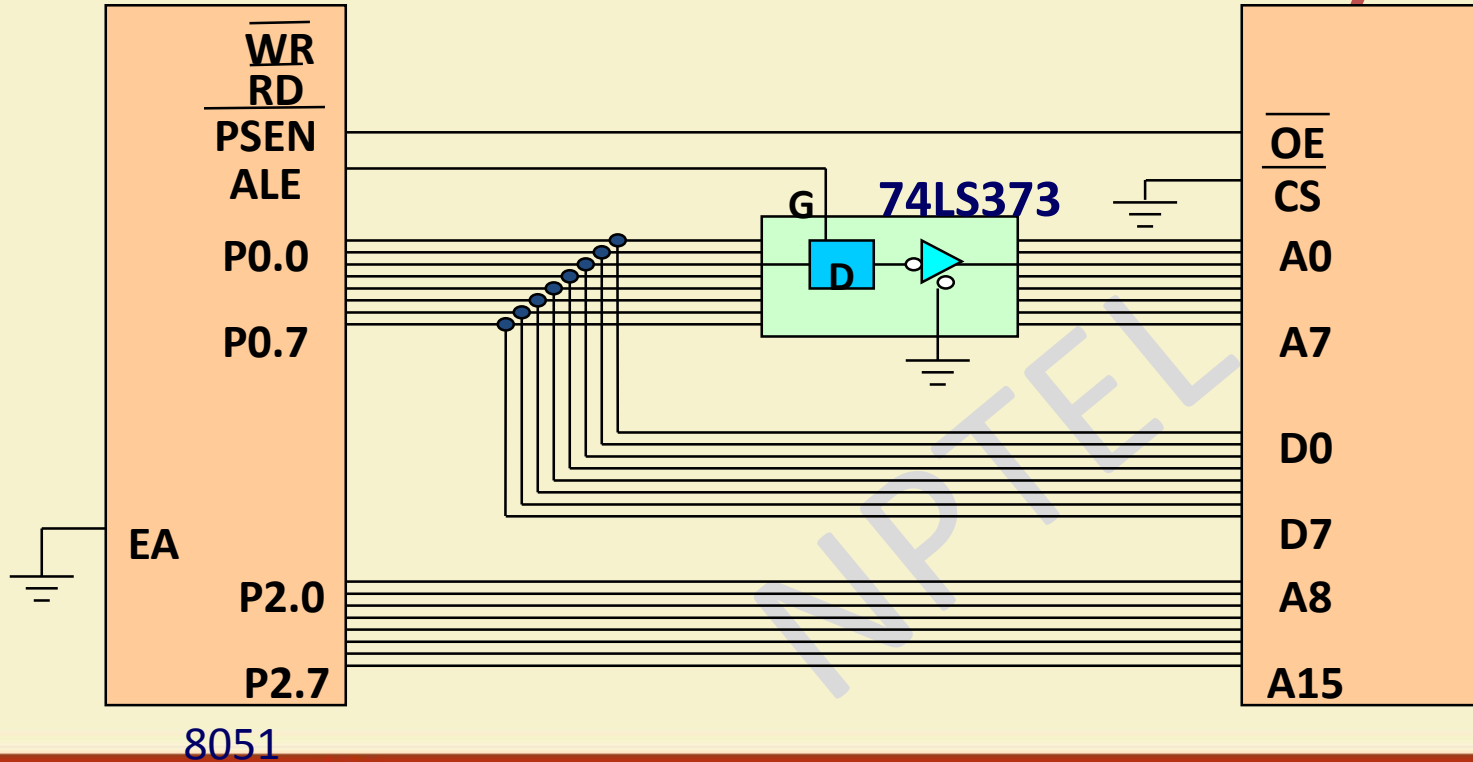
Interface
to 1K
RAM



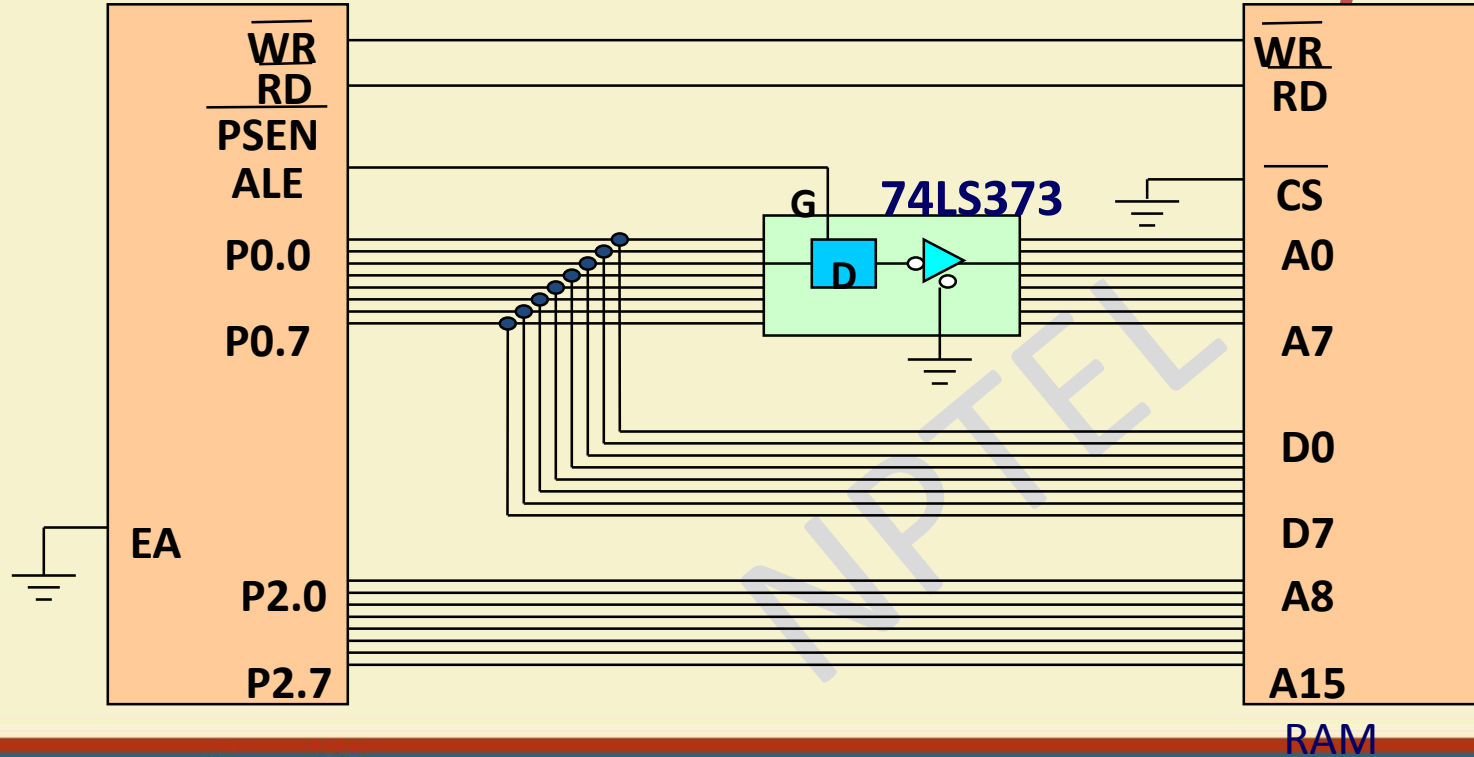
Timing for MOVX instruction



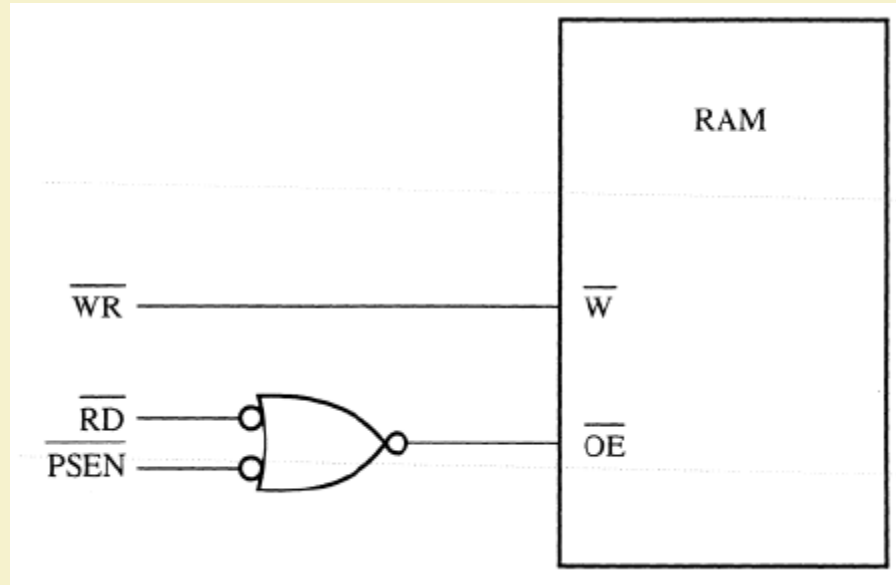
External code memory



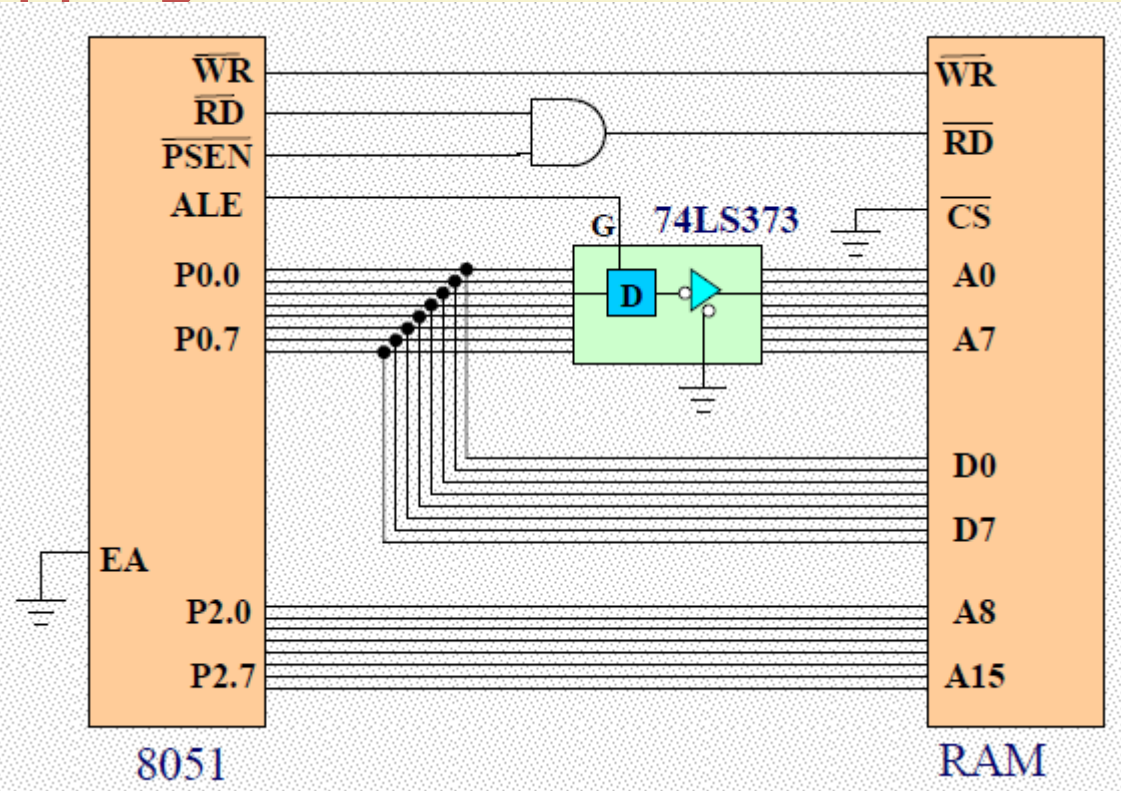
External data memory



Overlapping External Code and Data Spaces



Overlapping External Code and Data Spaces



Overlapping External Code and Data Spaces

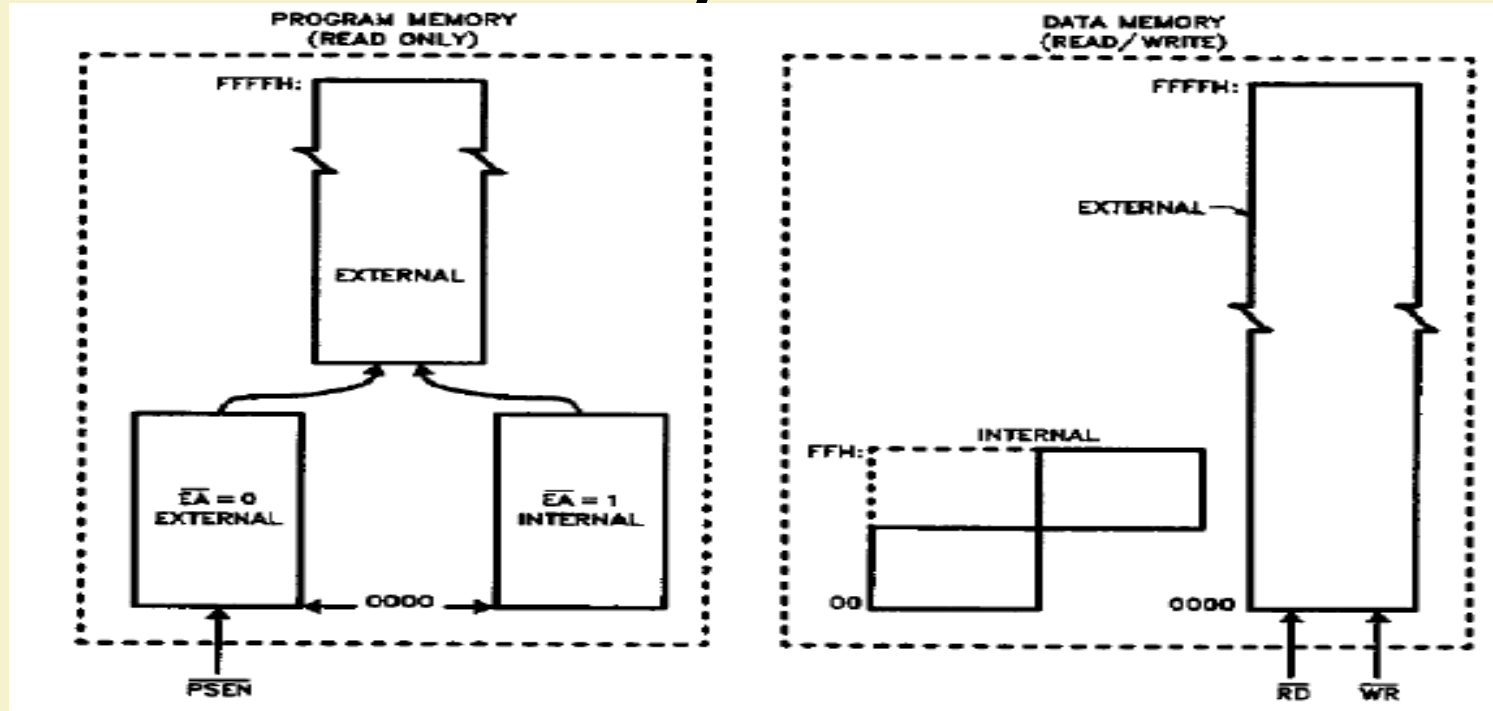
- Allows the RAM to be

- ❖ written as data memory, and
- ❖ read as data memory as well as **code memory**.

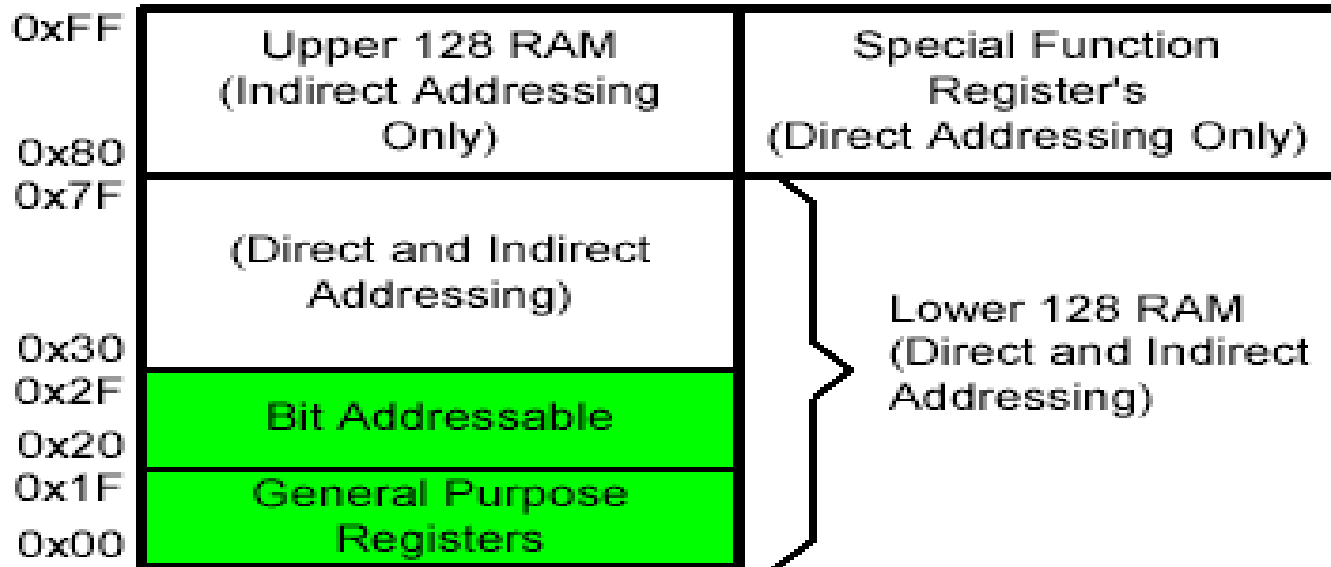
- This allows a program to be

- ❖ downloaded from outside into the RAM as data, and
- ❖ executed from RAM as code.

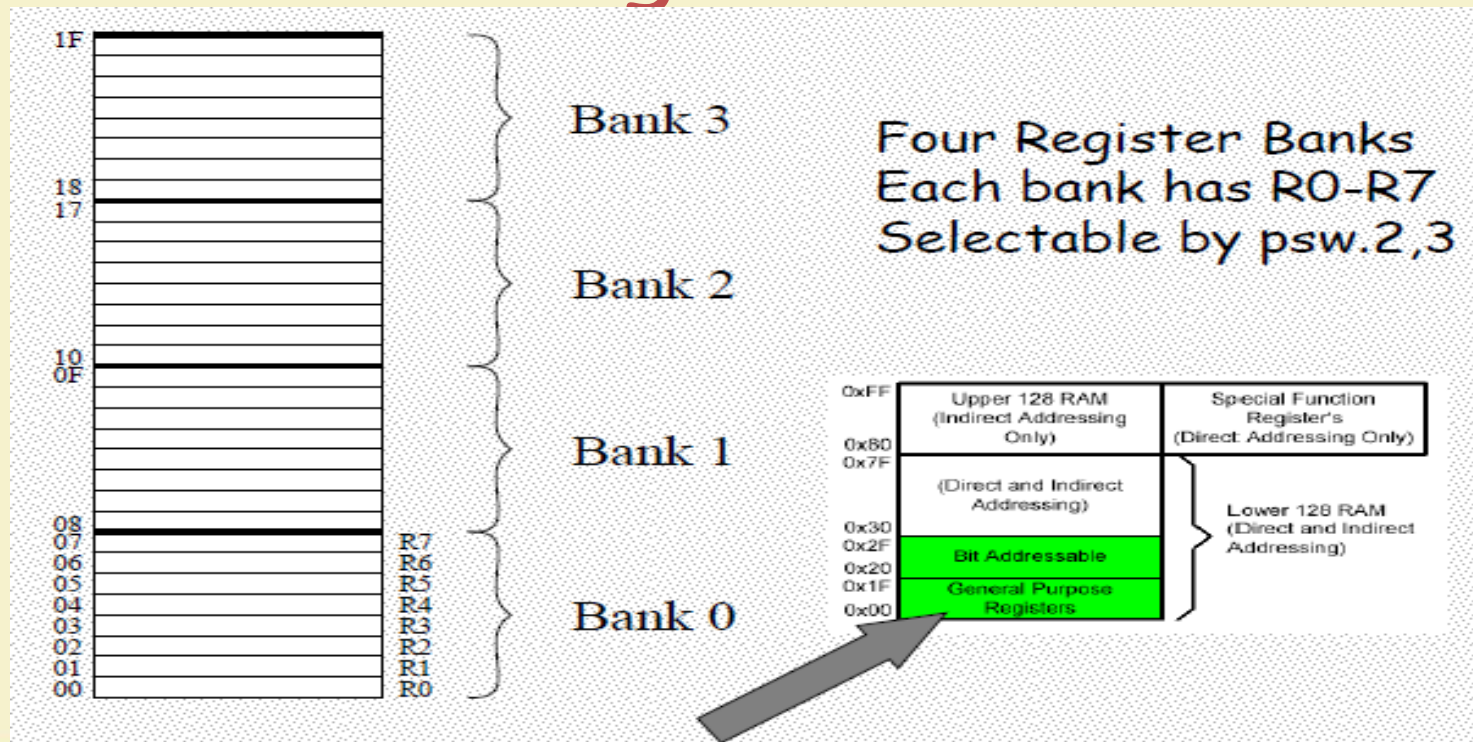
Memory Structure



On-Chip Memory Internal RAM



Registers



Bit Addressable Memory

2F	7F							78
2E								
2D								
2C								
2B								
2A								
29								
28								
27								
26								
25								
24						1A		
23								10
22	0F							08
21	07	06	05	04	03	02	01	00
20								

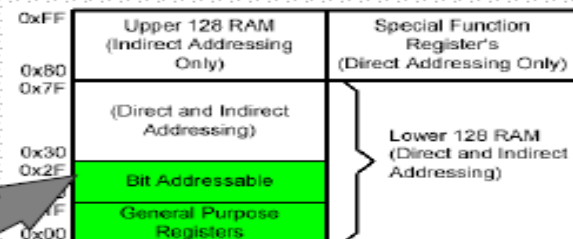
20h – 2Fh (16 locations X
8-bits = 128 bits)

Bit addressing:

mov C, 1Ah

or

mov C, 23h.2

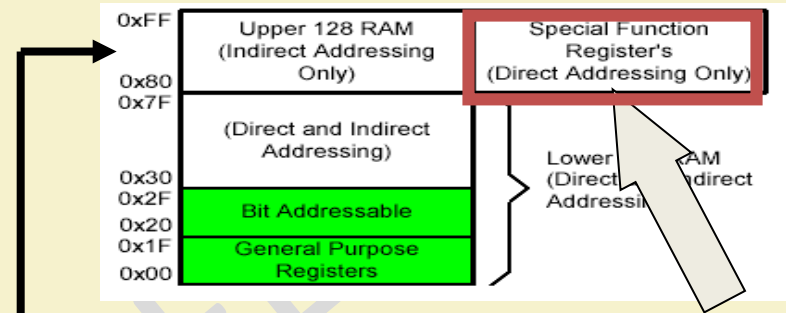


Special Function Registers

❑ DATA registers

❑ CONTROL registers

- ❖ Timers
- ❖ Serial ports
- ❖ Interrupt system
- ❖ Analog to Digital converter
- ❖ Digital to Analog converter
- ❖ Etc.



Addresses 80h - FFh

Direct Addressing used to access SPRs

Bit Addressable RAM

Summary
of the 8051
on-chip
data
memory
(RAM)

RAM

Byte address	Bit address							
27	3F	3E	3D	3C	3B	3A	39	38
26	37	36	35	34	33	32	31	30
25	2F	2E	2D	2C	2B	2A	29	28
24	27	26	25	24	23	22	21	20
23	1F	1E	1D	1C	1B	1A	19	18
22	17	16	15	14	13	12	11	10
21	0F	0E	0D	0C	0B	0A	09	08
20	07	06	05	04	03	02	01	00
1F	Bank 3							
18								
17	Bank 2							
10								
0F	Bank 1							
08								
07	Default register bank for R0-R7							
00								

Bit-addressable locations

Byte address	Bit address															
7F	General purpose RAM															
30																
2F									7F	7E	7D	7C	7B	7A	79	78
2E									77	76	75	74	73	72	71	70
2D									6F	6E	6D	6C	6B	6A	69	68
2C									67	66	65	64	63	62	61	60
2B									5F	5E	5D	5C	5B	5A	59	58
2A									57	56	55	54	53	52	51	50
29									4F	4E	4D	4C	4B	4A	49	48
28									47	46	45	44	43	42	41	40

Bit-addressable locations



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Bit Addressable RAM

Summary
of the 8051
on-chip
data
memory

(Special
Function
Registers)

Byte address	Bit address		Byte address	Bit address	
98	9F 9E 9D 9C 9B 9A 99 98	SCON	FF		
			F0	F7 F6 F5 F4 F3 F2 F1 F0	B
90	97 96 95 94 93 92 91 90	P1			
			E0	E7 E6 E5 E4 E3 E2 E1 E0	ACC
8D	not bit addressable	TH1			
8C	not bit addressable	TH0	D0	D7 D6 D5 D4 D3 D2 – D0	PSW
8B	not bit addressable	TL1			
8A	not bit addressable	TL0	B8	– – – BC BB BA B9 B8	IP
89	not bit addressable	TMOD			
88	8F 8E 8D 8C 8B 8A 89 88	TCON	B0	B7 B6 B5 B4 B3 B2 B1 B0	P3
87	not bit addressable	PCON			
			A8	AF – – AC AB AA A9 A8	IE
83	not bit addressable	DPH			
82	not bit addressable	DPL	A0	A7 A6 A5 A4 A3 A2 A1 A0	P2
81	not bit addressable	SP			
80	87 86 85 84 83 82 81 80	P0	99	not bit addressable	SBUF

SFR Memory Map

SFR MEMORY MAP

8 Bytes

F8								FF
F0	B							F7
E8								E7
E0	ACC							DF
D8								D7
D0	PSW							CF
C8	T2CON		RCAP2L	RCAP2H	TL2	TH2		C7
C0								B7
B8	IP							BF
B0	P3							AF
A8	IE							A7
A0	P2							9F
98	SCON	SBUF						97
90	P1							8F
88	TCON	TMOD	TL0	TL1	TH0	TH1		87
80	P0	SP	DPL	DPH			PCON	

↑
Bit
Addressable

Figure 5

Register Banks

- ❑ Active bank selected by PSW [RS1,RS0] bit
- ❑ Permits fast “context switching” in interrupt service routines (ISR).

PSW: PROGRAM STATUS WORD. BIT ADDRESSABLE.

CY	AC	F0	RS1	RS0	OV	—	P
----	----	----	-----	-----	----	---	---

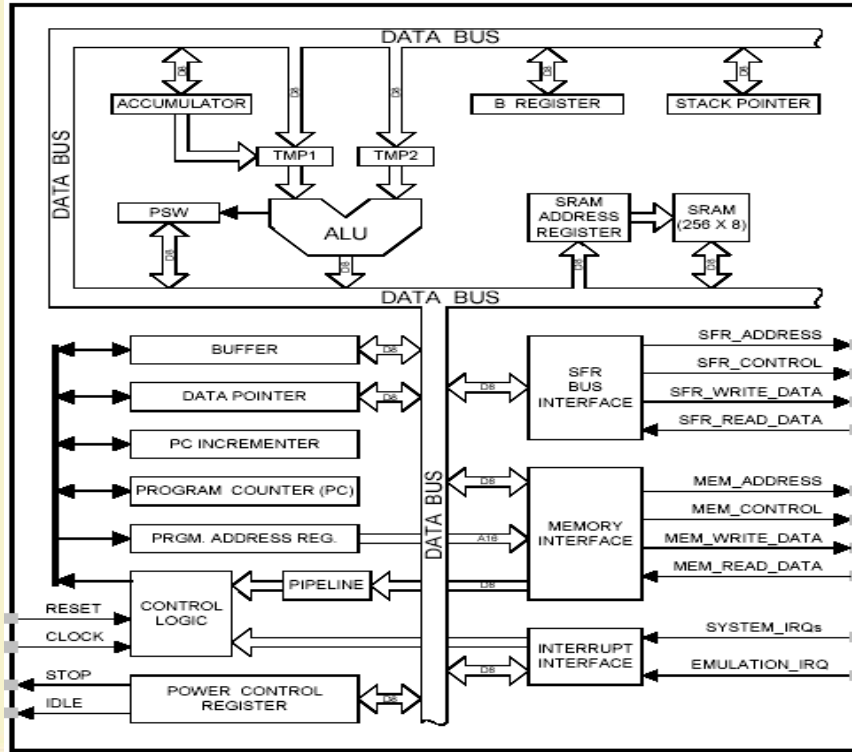
CY	PSW.7	Carry Flag.
AC	PSW.6	Auxiliary Carry Flag.
F0	PSW.5	Flag 0 available to the user for general purpose.
RS1	PSW.4	Register Bank selector bit 1 (SEE NOTE 1).
RS0	PSW.3	Register Bank selector bit 0 (SEE NOTE 1).
OV	PSW.2	Overflow Flag.
—	PSW.1	User definable flag.
P	PSW.0	Parity flag. Set/cleared by hardware each instruction cycle to indicate an odd/even number of '1' bits in the accumulator.

NOTE:

1. The value presented by RS0 and RS1 selects the corresponding register bank.

RS1	RS0	Register Bank	Address
0	0	0	00H-07H
0	1	1	08H-0FH
1	0	2	10H-17H
1	1	3	18H-1FH

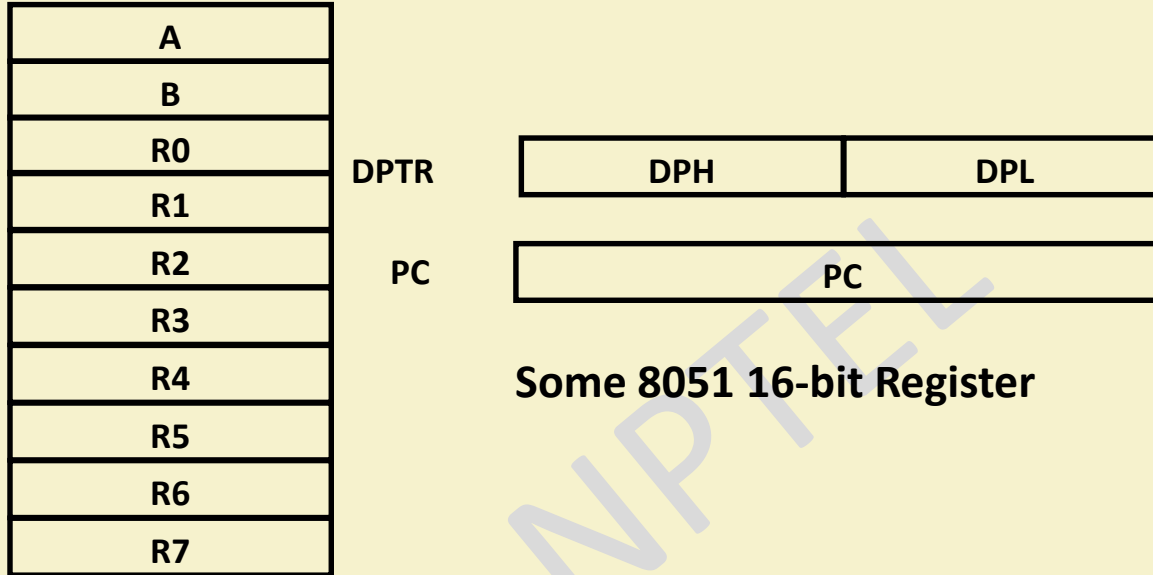
8051 CPU Registers



- A (Accumulator)
- B
- PSW (Program Status Word)
- SP (Stack Pointer)
- PC (Program Counter)
- DPTR (Data Pointer)

Used in assembler instructions

Registers



Some 8051 16-bit Register

Some 8-bit Registers of the 8051

The 8051 Assembly Language



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Overview

- Data transfer instructions
- Addressing modes
- Data processing (arithmetic and logic)
- Program flow instructions

Data Transfer Instructions

- MOV dest, source dest ← source
- Stack instructions
 PUSH byte ;increment stack pointer,
 ;move byte on stack
 POP byte ;move from stack to byte,
 ;decrement stack pointer
- Exchange instructions
 XCH a, byte ;exchange accumulator and byte
 XCHD a, byte ;exchange low nibbles of
 ;accumulator and byte



Addressing Modes

Immediate Mode – specify data by its **value**

```
mov A, #0           ;put 0 in the accumulator  
                    ;A = 00000000  
  
mov R4, #11h        ;put 11hex in the R4 register  
                    ;R4 = 00010001  
  
mov B, #11          ;put 11 decimal in b register  
                    ;B = 00001011  
  
mov DPTR, #7521h    ;put 7521 hex in DPTR  
                    ;DPTR = 0111010100100001
```

Addressing Modes

Immediate Mode – continue

```
MOV DPTR, #7521h  
MOV DPL, #21H  
MOV DPH, #75
```

```
COUNT EQU 30  
~  
~  
mov R4, #COUNT
```

```
MOV DPTR, #MYDATA  
~  
~  
ORG 200H  
MYDATA: DB "INDIA"
```