

Module 2

Embedded Processors and Memory

Lesson

11

Embedded Processors - II

Signals of a Typical Microcontroller

In this lesson the student will learn the following

- The Overview of Signals of Intel MCS 96 family of Microcontrollers
- Introduction
- Typical Signals of a Microcontroller

Pre-requisite

- Digital Electronics

11.1 Introduction

Microcontrollers are required to operate in the real world without much of interface circuitry. The input-output signals of such a processor are both analog and digital. The digital data transmission can be both parallel and serial. The voltage levels also could be different.

The architecture of a basic microcontroller is shown in Fig. 11.1. It illustrates the various modules inside a microcontroller. Common processors will have Digital Input/Output, Timer and Serial Input/Output lines. Some of the microcontrollers also support multi-channel Analog to Digital Converter (ADC) as well as Digital to Analog Converter (DAC) units. Thus analog signal input and output pins are also present in typical microcontroller units. For external memory and I/O chips the address as well as data lines are also supported.

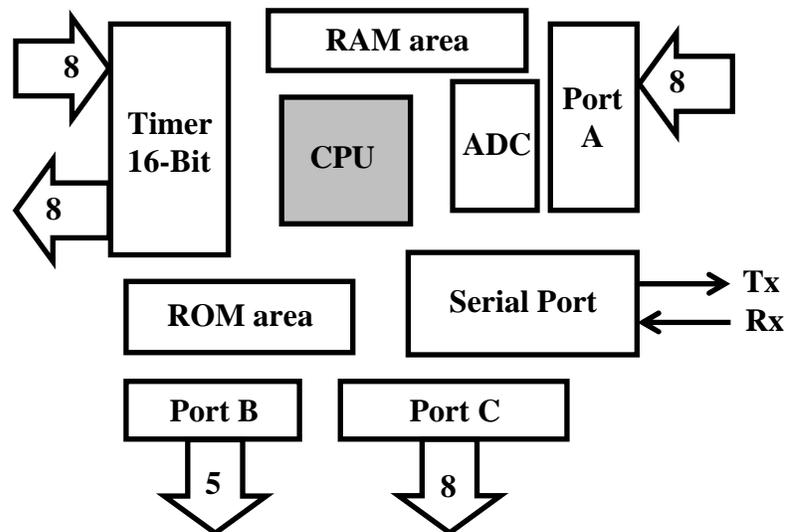


Fig. 11.1 A basic Microcontroller and its signals

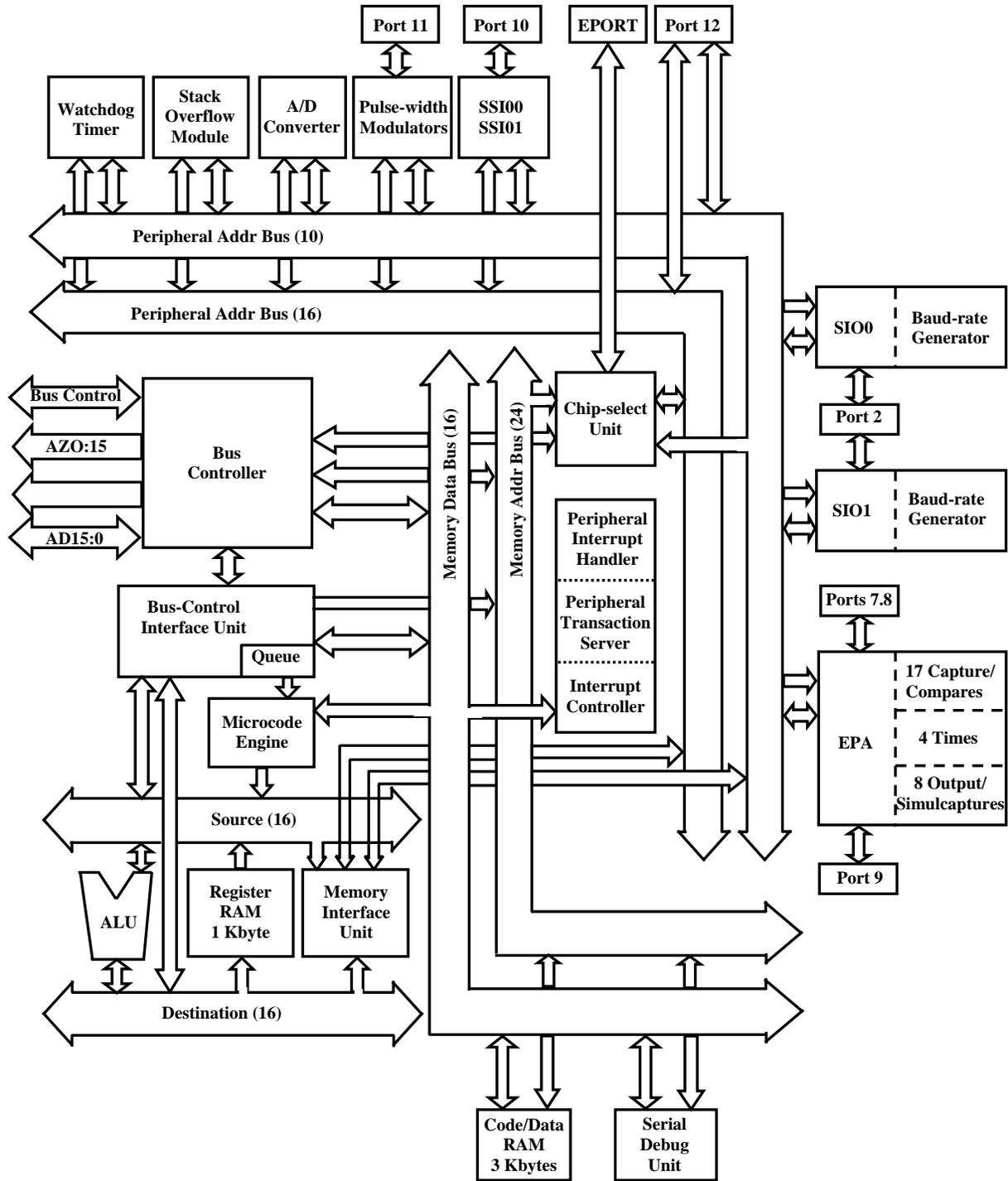


Fig. 11.2 The architecture of an MCS96 processor

11.2 The Signals of Intel Mcs 96

The various units of an MCS96 processor are shown in Fig. 11.2. The signals of such a processor can be divided into the following groups

- Address/Data Lines
- Bus Control Signals
- Signals related to Interrupt
- Signals related to Timers/Event Manager
- Digital Input/Output Ports
- Analog Input/Output Ports

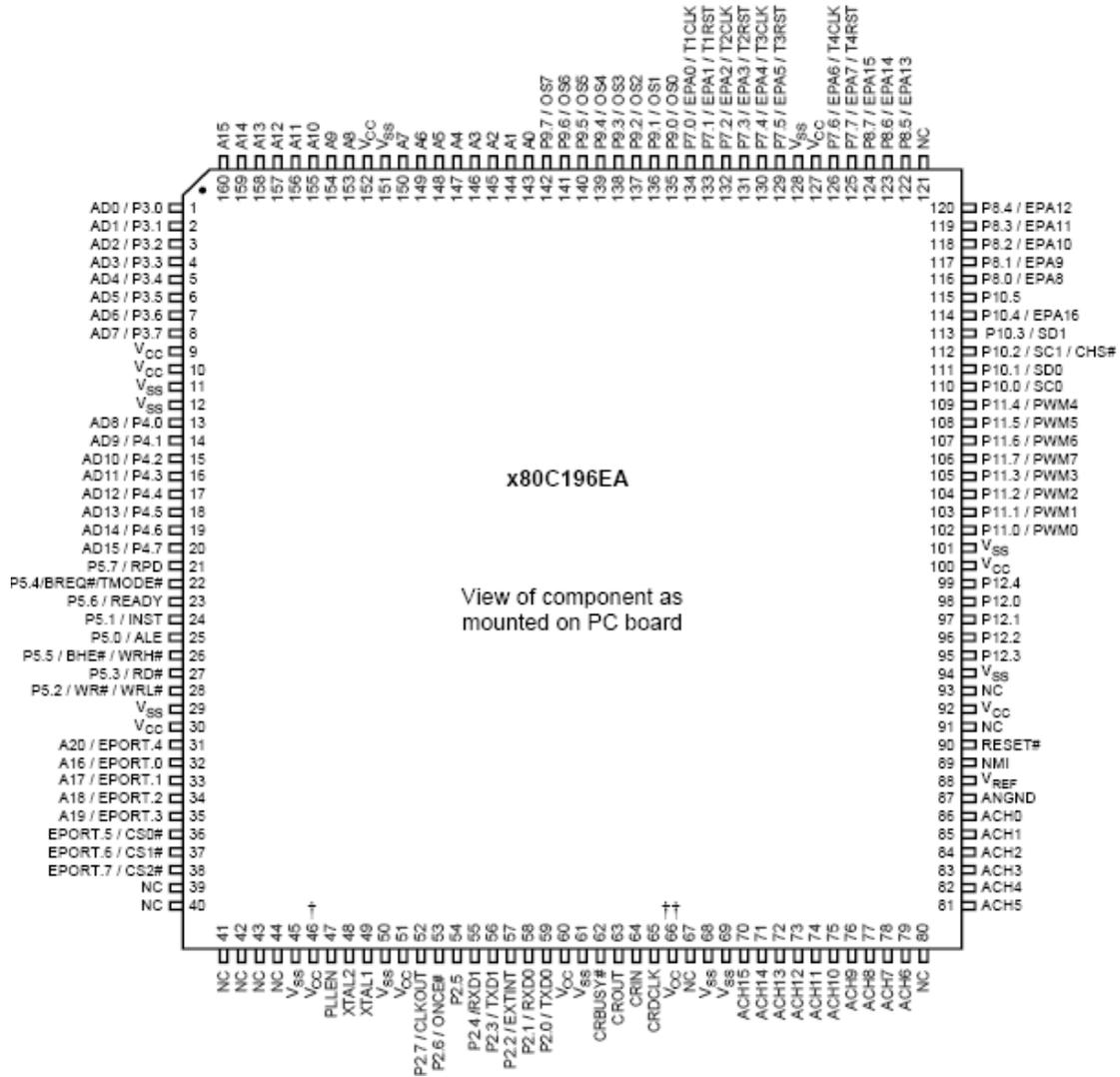


Fig. 11.3 Signals of MCS96

Address and Data Pins

A15:0 System Address Bus. These are output pins and provide address bits 0–15 during the entire external memory cycle.

A20:16 Address Pins 16–20. These are output pins used during external memory cycle. These are multiplexed with EPOR.4:0. This is a part of the 8-bit extended addressing port. It is used to

support extended addressing. The EPORT is an 8-bit port which can operate either as a general-purpose I/O signal (I/O mode) or as a special-function signal (special-function mode).

AD15:0 Address/Data Lines These lines serve as input as well as output pins. The function of these pins depends on the bus width and mode. When a bus access is not occurring, these pins revert to their I/O port function. AD15:0 drive address bits 0–15 during the first half of the bus cycle and drive or receive data during the second half of the bus cycle.

Bus Control and Status Signals

ALE Address Latch Enable: This is an output signal and is active-high output. It is asserted only during external memory cycles. ALE signals the start of an external bus cycle and indicates that valid address information is available on the system address/data bus (A20:16 and AD15:0 for a multiplexed bus; A20:0 for a demultiplexed bus). An external latch can use this signal to demultiplex address bits 0–15 from the address/data bus in multiplexed mode.

BHE: Byte High Enable- During 16-bit bus cycles, this active-low output signal is asserted for word and high-byte reads and writes to external memory. BHE# indicates that valid data is being transferred over the upper half of the system data bus.

WRH Write High. This is an output signal During 16-bit data transfers from the cpu to external devices, this active-low output signal is asserted for high-byte writes and word writes to external memory.

BREQ: Bus Request .This is an output signal. This active-low output signal is asserted during a hold cycle when the bus controller has a pending external memory cycle.

CS2:0 Chip-select Lines 0–2: Output Signal. The active-low output is asserted during an external memory cycle when the address to be accessed is in the range as programmed.

HOLD: Input Signal: Hold Request An external device uses this active-low input signal to request control of the bus.

HLDA: Output Signal: Bus Hold Acknowledge This active-low output indicates that the CPU has released the bus as the result of an external device asserting HOLD.

INST Output signal: When high, INST indicates that an instruction is being fetched from external memory. The signal remains high during the entire bus cycle of an external instruction fetch.

RD: Read Signal: Output: It is asserted only during external memory reads.

READY: Ready Input: This active-high input can be used to insert wait states in addition to those programmed in the chip configuration.

WR: Write: Output Signal: This active-low output indicates that an external write is occurring. This signal is asserted only during external memory writes.

WRH Write High: Output Signal: During 16-bit bus cycles, this active-low output signal is asserted for high-byte writes and word writes to external memory.

WRL Write Low: Output Signal: During 16-bit bus cycles, this active-low output signal is asserted for low-byte writes and word writes to external memory.

Processor Control Signals

CLKOUT: Clock Out: It is the output of the internal clock generator. This signal can be programmed to have different frequencies and can be used by the external devices for synchronization etc.

EA: External Access: Input Signal: This input determines whether memory accesses to the upper 7 Kbytes of ROM (FF2400–FF3FFFH) are directed to internal or external memory. These accesses are directed to internal memory if EA# is held high and to external memory if EA# is held low. For an access to any other memory location, the value of EA# is irrelevant.

EXTINT: External Interrupt Input: In normal operating mode, a rising edge on EXTINT sets the EXTINT interrupt pending bit. EXTINT is sampled during phase 2 (CLKOUT high). The minimum high time is one state time. If the EXTINT interrupt is enabled, the CPU executes the interrupt service routine.

NMI: Nonmaskable Interrupt Input: In normal operating mode, a rising edge on NMI generates a nonmaskable interrupt. NMI has the highest priority of all prioritized interrupts.

ONCE: Input: On-circuit emulation (ONCE) mode electrically isolates the microcontroller from the system. By invoking the ONCE mode, you can test the printed circuit board while the microcontroller is soldered onto the board.

PLEN: Input Signal: Phase-locked Loop Enable This active-high input pin enables the on-chip clock multiplier. The PLEN pin must be held low along with the ONCE# pin to enter on-circuit emulation (ONCE) mode.

RESET: I/O Reset: A level-sensitive reset input to, and an open-drain system reset output from, the microcontroller. Either a falling edge on or an internal reset turns on a pull-down transistor connected to the RESET for 16 state times. In the power down and idle modes, asserting RESET causes the microcontroller to reset and return to normal operating mode.

RPD: Return-From-Power-Down Input Signal: Return from Power down Timing pin for the return-from-power down circuit.

TMODE: Test-Mode Entry Input: If this pin is held low during reset, the microcontroller will enter a test mode. The value of several other pins defines the actual test mode.

XTAL1 I Input Crystal/Resonator or External Clock Input: Input to the on-chip oscillator and the internal clock generators. The internal clock generators provide the peripheral clocks, CPU clock, and CLKOUT signal. When using an external clock source instead of the on-chip oscillator, connect the clock input to XTAL1.

XTAL2: Output: Inverted Output for the Crystal/Resonator Output of the on-chip oscillator inverter. Leave XTAL2 floating when the design uses an external clock source instead of the on-chip oscillator.

Parallel Digital Input/Output Ports

P2.7:0 I/O Port 2: This is a standard, 8-bit, bidirectional port that shares package pins with individually selectable special-function signals. P2.6 is multiplexed with the ONCE function.

P3.7:0 I/O Port 3: This is a memory-mapped, 8-bit, bidirectional port with programmable open drain or complementary output modes.

P4.7:0 I/O Port 4 This is a memory-mapped, 8-bit, bidirectional port with programmable open drain or complementary output modes.

P5.7:0 I/O Port 5 This is a memory-mapped, 8-bit, bidirectional port.

P7.7:0 I/O Port 7 This is a standard, 8-bit, bidirectional port that shares package pins with individually selectable special-function signals.

P8.7:0 I/O Port 8: This is a standard, 8-bit, bidirectional port.

P9.7:0 I/O Port 9: This is a standard, 8-bit, bidirectional port.

P10.5:0 I/O Port 10: This is a standard, 6-bit, bidirectional port that is multiplexed with individually selectable special-function signals.

P11.7:0 I/O Port 11: This is a standard, 8-bit, bidirectional port that is multiplexed with individually selectable special-function signals.

P12.4:0 I/O Port 12: This is a memory-mapped, 5-bit, bidirectional port. P12.2:0 select the TROM

Most of the above ports are shared with other important signals discussed here. For instance Port 3 pins P3.7:0 share package pins with AD7:0. That means by writing a specific word to the configuration register the pins can change their function.

Serial Digital Input/Output Ports

TXD1:0 Output Signal: Transmit Serial Data 0 and 1. It can be programmed in different modes by writing specific words to the internal configuration registers.

RXD1:0 Input: Receive Serial Data 0 and 1 in different preprogrammed modes.

Analog Inputs

ACH15:0: Input Analog Channels: These signals are analog inputs to the A/D converter. The ANGND and VREF pins are also used for the standard A/D converter to function.

Other important signals of a typical microcontroller include

- Power Supply and Ground pins at multiple points
- Signals from the internal programmable Timer
- Debug Pins

The reader is requested to follow the link www.intel.com/design/mcs96/manuals/272804.htm or www.intel.com/design/mcs96/manuals/27280403.pdf for more details.

Some Specifications of the Processor

Frequency of Operation: 40 MHz

2 Mbytes of linear address space

1 Kbyte of register RAM

3 Kbytes of code RAM

8 Kbytes of ROM

2 peripheral interrupt handlers (PIH)

6 peripheral interrupts

83 I/O port pins

2 full-duplex serial ports with baud-rate generators

Synchronous serial unit

8 pulse-width modulator (PWM) outputs with 8-bit resolution

16-bit watchdog timer

Sixteen 10-bit A/D channels

Programmable clock output signal

11.3 Conclusions

This chapter discussed the important signals of a typical microcontroller. The detailed electrical and timing specifications are available in the respective manuals.

11.4 Questions

1. Which ports of the 80C196EA can generate PWM pulses? What is the voltage level of such pulses?

Ans:

Port Pin	PWM Signal	PWM Signal Type	Description
P6.6	PWM0	O	Pulse-width modulator 0 output with high-drive capability.
P6.7	PWM1	O	Pulse-width modulator 1 output with high-drive capability.

2. Why the power supply is given to multiple points on a chip?

Ans:

The multiple power supply points ensure the following

- The voltages at devices (transistors and cells) are better than a set target under a specified set of varying load conditions in the design. This is to ensure correct operation of circuits at the expected level of performance.
- the current supplied by a pad, pin, or voltage regulator is within a specified limit under any of the specified loading conditions. This is required: a) for not exceeding the design capacity of regulators and pads; and b) to distribute currents more uniformly among the pads, so that the $L \frac{di}{dt}$ voltage variations due to parasitic inductance in the package's substrate, ball-grid array, and bond wires are minimized.