Module
2

Embedded Processors and Memory

Lesson 9

General Purpose Processors - II

Signals

In this lesson the student will learn the following
> Signals of a General Purpose Processor
>> Multiplexing
>> Address Signals
>> Data Signals
>> Control
>>> Bus Arbitration Signals
>>> Status Signal Indicators
>> Sleep State Indicators
>> Interrupts

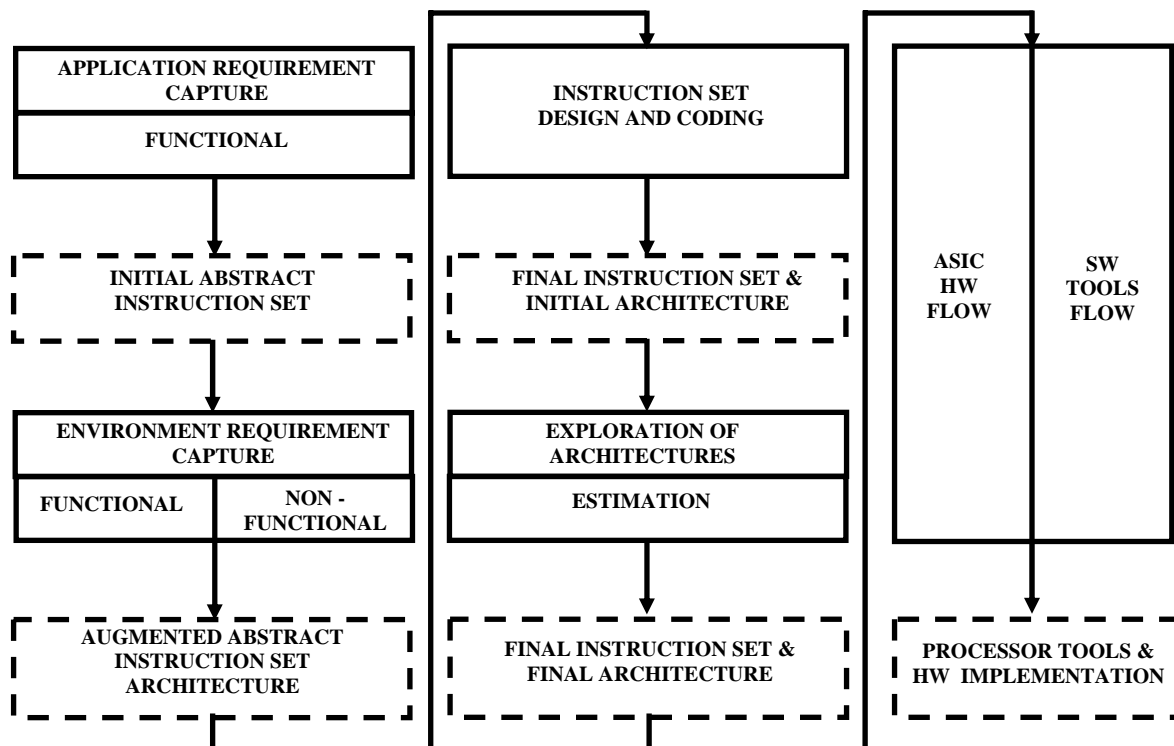# Pre-requisite

Digital Electronics

9.1   Introduction

The input/output signals of a processor chip are the matter discussion in this chapter. We shall take up the same VIA C3 processor as discussed in the last chapter.

In the design flow of a processor the internal architecture is determined and simulated for optimal performance.

**Fig. 9.1 The overall design flow for a typical processor**

The basic architecture decides the signals. Broadly the signals can be classified as:
1. Address Signals
2. Data Signals
3. Control Signals
4. Power Supply Signals

Some of these signals are *multiplexed in time* for making the VLSI design easier and efficient without affecting the over all performance.

Multiplexed in Time (known as Time Division Multiplexing)

A digital data transmission method that takes signals from multiple sources, divides them into pieces which are then placed periodically into time slots,(clock cycles here) transmits them down a single path and reassembles the time slots back into multiple signals on the remote end of the transmission
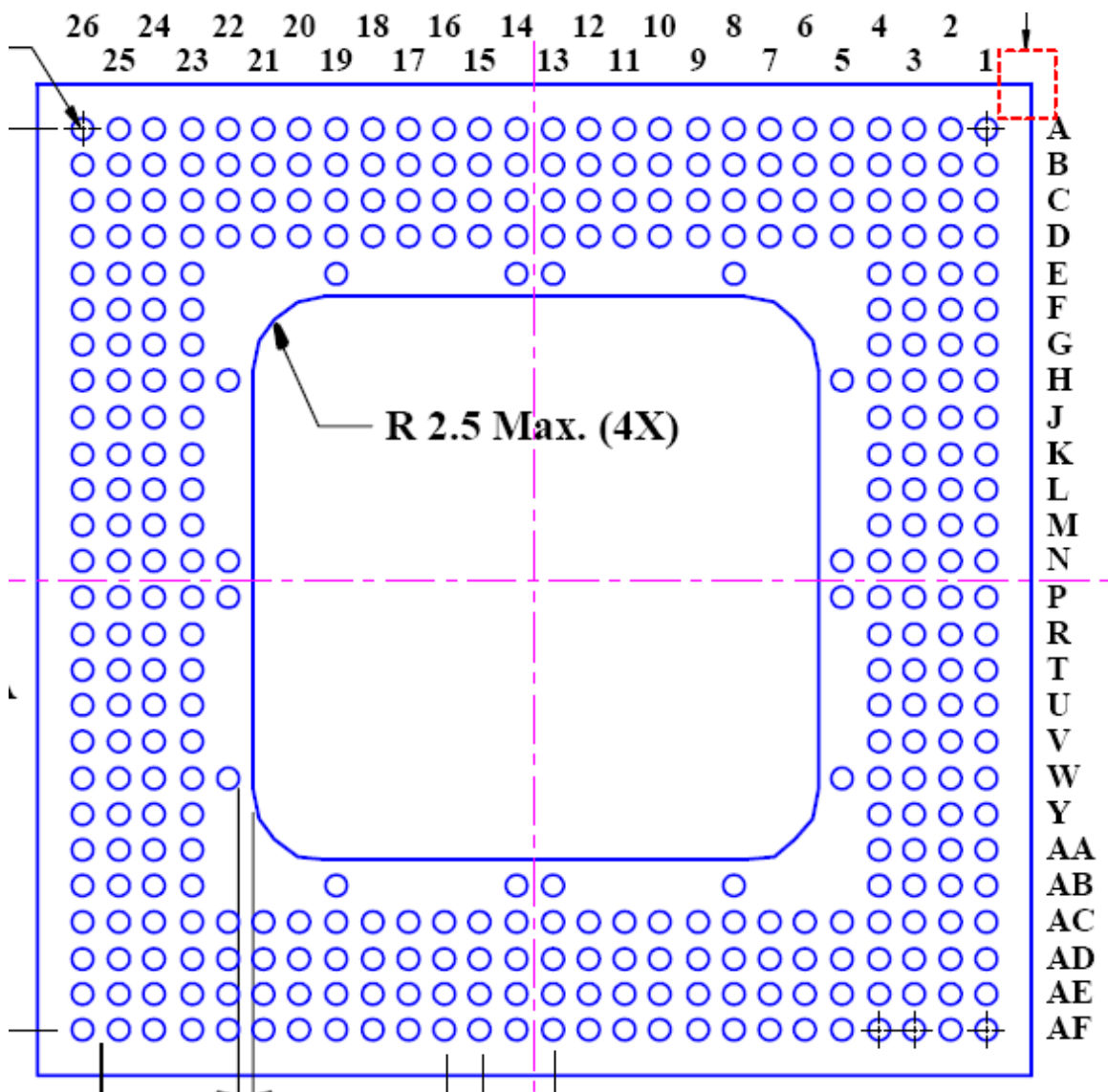
Fig. 9.2 Bottom View of the Processor

9.2   Signals of VIA Processor discussed earlier

The following lines discuss the various signals associated with the processor.

A[31:3]# The address Bus provides addresses for physical memory and external I/O devices. During cache inquiry cycles, A31#-A3# are used as inputs to perform *snoop cycles*. This is an output signal when it sends and address to the memory and I/O device. It serves as both input and output during snoop cycles. It is synchronized with the Bus Clock (BCLK)

Snoop cycles: The term "snooping" commonly refers to at least three different actions.

- *Inquire Cycles: These are bus cycles, initiated by external logic, that cause the processor to look up an address in its physical cache tags.*

- *Internal Snooping: These are internal actions by the processor (rather than external logic) that are taken during certain types of cache accesses in order to detect self-modifying code.*
- *Bus Watching: Some caching devices watch their address and data bus continuously while they are held off the bus, comparing every address driven by another bus master with their internal cache tags and optionally updating their cached lines on the fly, during write backs by the other master.*

A20M# A20 Mask causes the CPU to make (force to 0) the A20 address bit when driving the external address bus or performing an internal cache access. A20M# is provided to emulate the 1 M Byte address wrap-around that occurs on the x86. Snoop addressing is not affected. It is an input signal. If it is not used then it is connected to the power supply. This is not synchronized with the Bus Clock or anything.

ADS# Address Strobe begins a *memory/I/O cycle* and indicates the address bus (A31#-A3#) and transaction request signals (REQ#) are valid. This is an output signal during addressing cycle and an input/output signal during *transaction request cycles*. This is synchronized with the bus clock.
Memory /I/O cycle: The memory and input output data transfer (read or write) is carried out in different clock cycles. The address is first loaded on the address bus. The processor being faster waits till the memory or input/output is ready to send or receive the date through the data bus. Normally it takes more than one clock cycle.
Transaction Request Cycle: When the external device request the CPU to transmit data. The request comes through this line.

BCLK Bus Clock: provides the fundamental timing for the CPU. The frequency of the input clock determines the operating frequency of the CPU's bus. External timing is defined referenced to the rising edge of CLK. It is an Input clock signal.

BNR# Block Next Request: signals a bus stall by a bus agent unable to accept new transactions. This is an input or output signal and is synchronized with the bus clock.

BPRI# Priority Agent Bus Request arbitrates for ownership of the system bus. Input and is synchronized with the Bus clock.
Bus Arbitration: At times external devices signal the processor to release the system address/data/control bus from its control. This is achieved by an external request which normally comes from the external devices such as a DMA controller or a Coprocessor.

BR[4:0]: Hardware strapping options for setting the processors internal clock multiplier. By strapping these wires to the supply or ground (some times they can be kept open for making them 1). This option divides the input clock.

BSEL[1:0]: Bus frequency select balls (BSEL 0 and BSEL 1) identify the appropriate bus speed (100 MHz or 133 MHz). It is an output signal.

BR0#: It drives the BREQ[0]# signal in the system to request access to the system bus.

D[63:0]#: Data Bus signals are bi-directional signals which provide the data path between the CPU and external memory and I/O devices. The data bus must assert DRDY# to indicate valid data transfer. This is both input as well as output.

DBSY#: Data Bus Busy is asserted by the data bus driver to indicate data bus is in use. This is both input as well as output.

DEFER#: Defer is asserted by target agent and indicates the transaction cannot be guaranteed as an in-order completion. This is an input signal.

DRDY#: Data Ready is asserted by data driver to indicate that a valid signal is on the data bus. This is both input and output signal.

FERR#: FPU Error Status indicates an unmasked floating-point error has occurred. FERR# is asserted during execution of the FPU instruction that caused the error. This is an output signal.

FLUSH#: Flush Internal Caches writing back all data in the modified state. This is an input signal to the CPU.

HIT#: Snoop Hit indicates that the current cache inquiry address has been found in the cache. This is both input as well as output signal.

HITM#: Snoop Hit Modified indicates that the current cache inquiry address has been found in the cache and dirty data exists in the cache line (modified state). (both input/output)

INIT#: Initialization resets integer registers and does not affect internal cache or floating point registers. (Input)

INTR: Maskable Interrupt I. This is an input signal to the CPU.

NMI: Non-Maskable Interrupt I

LOCK#: Lock Status is used by the CPU to signal to the target that the operation is *atomic*.
An atomic operation is any operation that a CPU can perform such that all results will be made visible to each CPU at the same time and whose operation is safe from interference by other CPUs. For example, reading or writing a word of memory is an atomic operation.

NCHCTRL: The CPU uses this ball to control integrated I/O pull-ups. A resistance is to be connected here to control the current on the input/output pins.

PWRGD (power good) Indicates that the processor's VCC is stable. It is an input signal.

REQ[4:0]#: Request Command is asserted by bus driver to define current transaction type.

RESET#: This is an input that resets the processor and invalidates internal cache without writing back.

RTTCTRL: The CPU uses this ball to control the output impedance.

RS[2:0]#: Response Status is an input that signals the completion status of the current transaction when the CPU is the response agent.

SLP#: Sleep when asserted in the stop grant state, causes the CPU to enter the *sleep state*.

Different Sleep states

"Stop Grant"
Power to CPU is maintained, but no instructions are executed. The CPU halts itself and may shut down many of its internal components. In Microsoft Windows, the "Standby" command is associated with this state by default.

"Suspend to RAM"
All power to the CPU is shut off, and the contents of its registers are flushed to RAM, which remains on. This system state is the most prone to errors and instability.

"Suspend to Disk"
CPU power shut off, but RAM is written to disk and shut off as well. In Microsoft Windows, the "Hibernate" command is associated with this state. Because the contents of RAM are written out to disk, system context is maintained. For example, unsaved files would not be lost following this.

"Soft Off"
System is shut down, however some power may be supplied to certain devices to generate a wake event, for example to support automatic startup from a LAN or USB device. In Microsoft Windows, the "Shut down" command is associated with this state. Mechanical power can usually be removed or restored with no ill effects.

Processor "C" power states
Processor "C" power states are also defined. These are typically implemented in laptop platforms only. Here the cpu consumes less power while still doing work, and the tradeoff comes between power and performance, rather than power and latency.

SMI#: System Management (SMM) Interrupt forces the processor to save the CPU state to the top of SMM memory and to begin execution of the SMI services routine at the beginning of the defined SMM memory space. An SMI is a high-priority interrupt than NMI.

STPCLK#: Stop Clock Input causes the CPU to enter the stop grant state.

TRDY#: Target Ready Input indicates that the target is ready to receive a write or write-back transfer from the CPU.

VID[3:0]: Voltage Identification Bus informs the regulatory system on the motherboard of the CPU Core voltage requirements. This is an output signal.

9.3 Conclusion

In this chapter the various signals of a typical general purpose processor has been discussed. Broadly we can classify them into the following categories.

Address Signals: They are used to address the memory as well as input/output devices. They are often multiplexed with other control signals. In such cases External Bus controllers latch these address lines and make them available for a longer time for the memory and input/output devices while the CPU changes the status of the same. The Bus controllers drive their inputs which are

connected to the CPU to high impedance so as not to interfere with the current state of these lines from the CPU.

Data Signals: These lines carry the data to and fro the processor and memory or i/o devices. Transceivers are connected on the data path to control the data flow. The data flow might succeed some bus transaction signals. This bus transaction signals are necessary to negotiate the speed mismatch between the input/output and the processor.

Control Signals: These can be generally divided into the following groups
Read Write Control
Memory Write The processor issues this signal while sending data to the memory
Memory Read The processor issues this signal while reading the data from the memory
*I/O Read* The input/output read signal which is generally preceded by some bus transaction signals
I/O Write The input/output read signal which is generally succeeded by some bus transaction signals
These read write signals are not generally directly available from the CPU. They are decoded from a set of status signal by an external bus controller.

Bus Transaction Control

- **Master versus Slave**

Bus master	**master send address**	**Bus slave**
	data can go either way	
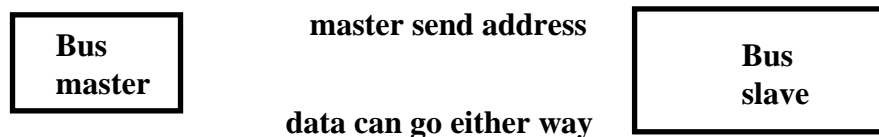
A bus transaction includes two parts: sending the address and receiving or sending the data. Master is the one who starts the bus transaction by sending the address. Slave is the one who responds to the address by sending data to the master if the master asks for data and receiving data from master if master wants to send data. These are controlled by signals like Ready, Defer etc.

Bus Arbitration Control

Bus Master	**Control: master initiates requests**	**Bus Slave**
	Data can go either way	
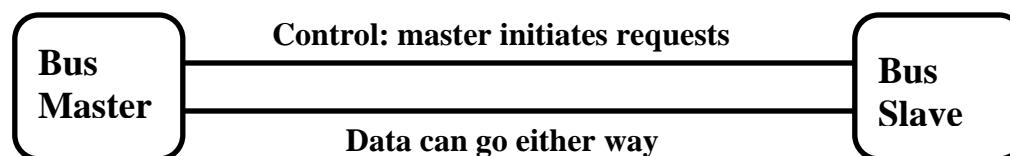
This is known as requesting to obtain the access to a bus. They are achieved by the following lines.
Bus Request: The slave requests for the access grant
Bus Grant: Gets the grant signal
Lock: For specific operations the bus requests are not granted as the CPU might be doing some important operations.

Interrupt Control

In a multitasking environment the Interrupts are external signals to the CPU for emergency operations. The CPU executes the interrupt service routines while acknowledging the interrupts. The interrupts are processed according to their priority. More discussion is available in subsequent lessons.

Processor Control

These lines are activated when there is a power on or the processor comes up from a power-saving mode such as sleep. These are
Reset
Test lines etc.
Some of the above signals will be discussed in the subsequent lessons.

9.4   Questions and Answers

Q1.   What is maximum memory addressing capability of the processor discussed in this lecture?

Ans: The number of address lines is 32. Therefore it can address 2^{32} locations which is 4G bytes

Q2.   What do you understand by POST in a desktop computer?

Ans: It is called Power On Self Test. This is a routine executed to check the proper functioning of Hard Disk, CDROM, Floppy Disk and many other on-board and off-board components while the computer is powered on.

Q3.   Describe the various power-saving modes in a general purpose CPU?

Ans: *Refer to: Sleep Mode in Text*

Q4.   What could be the differences in design of a processor to be used in the following applications?
          LAPTOP
          Desktop
          Motor Control

Ans:
LAPTOP processor: should be complex General Purpose Processor with low power consumption and various power saving modes.

Desktop: High Performance processor which has no limit on power consumption.

Motor Control: Simple low power specialized processor with on-chip peripherals with Real Time Operating System.

Q5.   What is the advantage of reducing the High state voltage from 5 V to 3.5 volts? What are the disadvantages?

Ans:

      It reduces the interference but decreases the noise accommodation.

Q6. What is the use of Power-Good signal?

Ans:

It is used to know the quality of supply in side the CPU. If it is not good there may mal-operations and data loss.