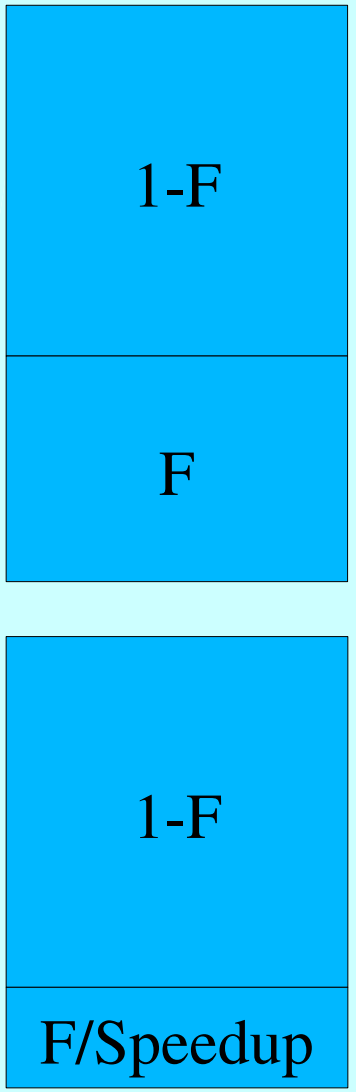
LECTURE - 03

Amdahl's Law

- Amdahl's law:
  - Diminishing returns
  - Limit on overall speedup

$$Overall\ speedup = \frac{(1-F)+F}{(1-F)+\frac{F}{Speedup}}$$

- Corollary: make the common case fast



Illustrating Amdahl's Law

- Example: implement cache, or faster ALU?
  - Cache improves performance by 10x
  - ALU improves performance by 3x
- Depends on fraction of instructions
  - Suppose $F_{mem} = 0.2, F_{alu} = 0.5, F_{other} = 0.3$

$$Speedup\ with\ cache = \frac{1}{0.8 + 0.2/10} = 1.22$$

$$Speedup\ with\ faster\ ALU = \frac{1}{0.5 + 0.5/3} = 1.5$$

Example continued...

- Fixing $F_{alu} = 0.5$ for what value of F_{mem} is adding a cache better?

$$\frac{1}{1 - F_{mem} + F_{mem}/10} \geqslant 1.5$$

$$\Rightarrow F_{mem} \geqslant \frac{10}{27} = 0.36$$

The CPU Performance Equation

$$CPU\ time = Num.\ clock\ cycles \times Clock\ cycle\ time$$

OR

$$CPU\ time = Num.\ of\ clock\ cycles \div Clock\ rate$$

For a program,

$$Num.\ of\ clock\ cycles$$

$$= Instruction\ Count \times Cycles\ Per\ Instruction$$

$$= IC \times CPI$$

Putting these together

$$CPU\ time = IC \times CPI \times Cycle\ time$$

More on the Equation

- This form is convenient
  - Involves many relevant parameters
- Remembering is easy

$$CPU\ time = \frac{Seconds}{Program}$$

$$= \frac{Seconds}{Clock\ cycle} \times \frac{Clock\ cycles}{Instruction} \times \frac{Instructions}{Program}$$

- With CPI as the independent variable

$$CPI = \frac{CPU\ time}{Clock\ cycle\ time \times IC}$$

Other Convenient Forms of the Equation

- Number of clock cycles can be counted as:

$$CPU\ clock\ cycles = \sum_{i=1}^{n} CPI_i \times IC_i$$

$$Hence,\ CPU\ time = \left(\sum_{i=1}^{n} CPI_i \times IC_i\right) \times Clock\ cycle\ time$$

- Calculating CPI in terms of CPI_i

$$CPI = \frac{CPU\ time}{Clock\ cycle\ time \times IC} = \sum_{i=1}^{n} CPI_i \times \left(\frac{IC_i}{IC}\right)$$

Usefulness of the Equation

- IC_i easier to measure than F_i
  - Equivalently, F_i is measured through IC_i
- Equation includes relevant parameters such as the cycle time

Measuring the Parameters for the Equation

- Clock cycle time:
  - Easy for existing architectures
  - Needs to be estimated in the design process
- Instruction Count:
  - Requires a compiler
  - And, simulator/interpreter, or instrumentation code
- CPI for each instruction type:
  - Easy for simple architectures
  - Pipelines, caches introduce complications
  - Need to simulate and measure average CPI

A Design Example

- A design choice for conditional branch instructions:
  - Choice 1: condition code is set by a compare instruction, checked by the next (branch) instruction
    - 20% instructions are branches, and another 20% are compares
    - 2 cycles per branch, 1 cycle for all others
    - Clock-rate is 25% faster
  - Choice 2: single instruction for compare and branch
- Which choice is better?

Solution for Design Example

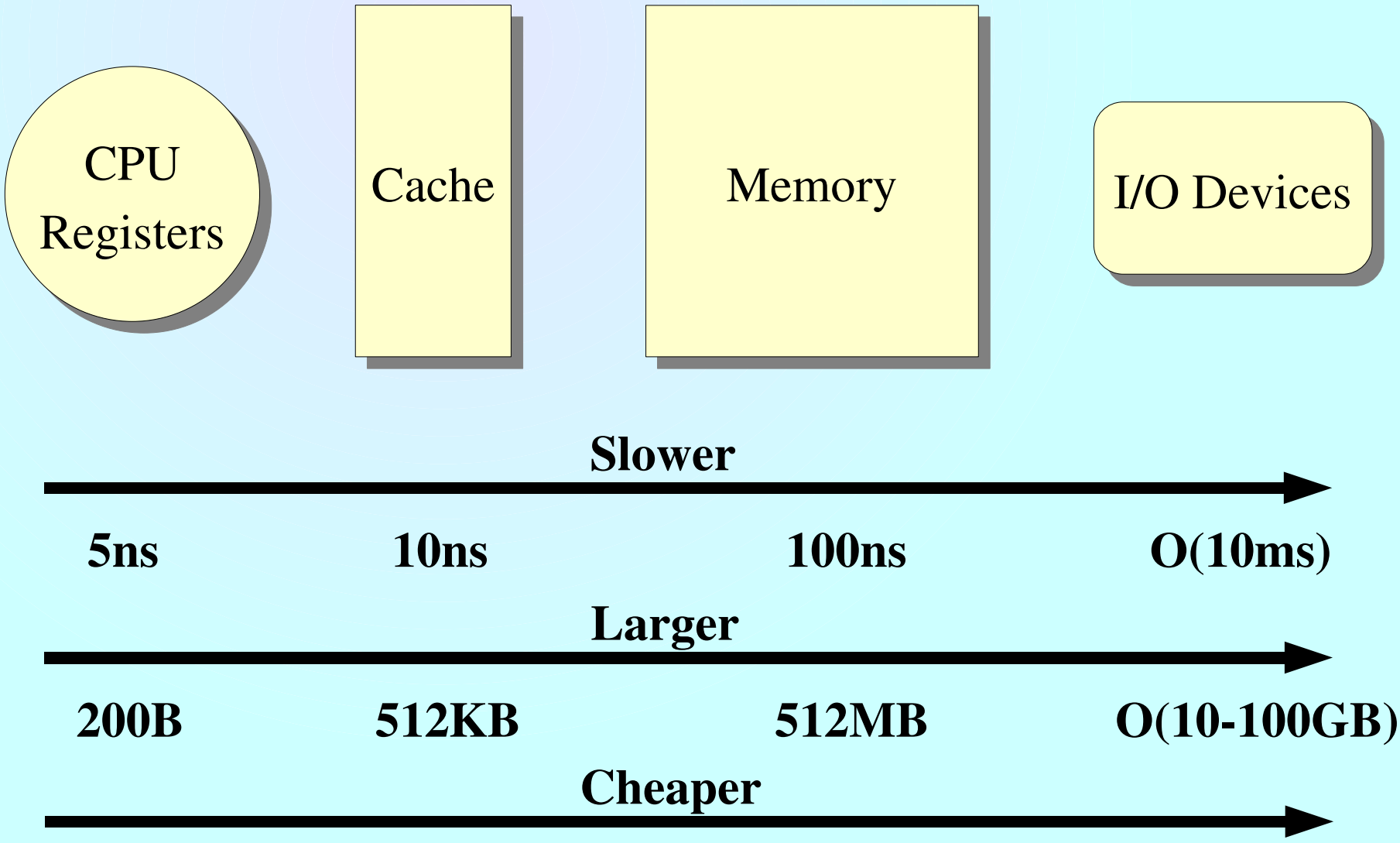
$$CPU\ time_1 = \frac{IC_1 \times [(0.8 \times 1) + (0.2 \times 2)]}{1.25 \times C} = \frac{IC_1}{C} \times \frac{1.2}{1.25}$$

$$CPU\ time_2 = \frac{IC_1 \times [(0.6 \times 1) + (0.2 \times 2)]}{C} = \frac{IC_1}{C}$$

Detailed Example: Using Caches

- Thumb rule in hardware design:
  - *Smaller is faster*
    - Signal propagation delay is lesser
    - More power per memory cell
- Observation w.r.t. software:
  - *Locality of reference*
  - Spatial as well as temporal

The Memory Hierarchy



Modifying the CPU Performance Equation

- Caches involved *hits* and *misses*
- Cache miss ==> memory stalls

$$CPU\ time = (CPU\ clock\ cycles + Memory\ stall\ cycles) \times Clock\ cycle$$

$$Memory\ stall\ cycles = Num.\ misses \times Miss\ penalty$$

$$= IC \times Misses\ per\ instruction \times Miss\ penalty$$

$$= IC \times Mem.\ refs.\ per\ instruction \times Miss\ rate \times Miss\ penalty$$

- Equation in the final form is useful: parameters can be measured

Some Numerics...

$$Fraction\ of\ memory\ access\ instructions = 0.4$$

$$CPI\ for\ memory\ instructions\ (hits) = 2$$

$$CPI\ for\ other\ instructions = 1$$

$$Choice\ 1: 0.04\ miss\ rate\ ,\ 25\ cycle\ penalty$$

$$Choice\ 2: 0.02\ miss\ rate\ ,\ 50\ cycle\ penalty$$

Which is a better choice?

What is the overall average CPI?

$$CPI_{avg} = (0.6 \times 1) + (0.4 \times 2) + (1 + 0.4) \times 0.02 \times 50 = 2.8$$

Next week...

- Instruction set architecture
- Pipelining
- Pipelining hazards