LECTURE - 28

Lecture Outline

- Consistency models
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- ***Scribe for today?***

Sequential Consistency

- Sequential consistency: result of execution same as if:
  - Accesses executed by a processor are in order
  - Accesses among different processors are interleaved
- That is, there exists *some interleaving* which will lead to the same result on a uni-processor
  - Or, a multi-processor with no caches, and no write-buffers, and only a single centralized memory

Implementing Sequential Consistency

- Need to guarantee that a write/read completes before any other access (by the same processor)
- Write completes == all invalidations have reached
- This implies that write buffers cannot used (writes cannot be delayed in general)

Synchronized Programs

- Programs which protect access to shared locations through synchronization operations
- More formally:
  - In every possible execution, for every shared data
  - Write by a processor, and access (read/write) by another processor
  - Are separated by a synchronization operation
- That is, the program is *data-race-free*
- Observation: most programs are synchronized

Sequential Consistency and Synchronized Programs

- Sequential consistency guarantees uni-processor-like behaviour for *any* program
  - True for synchronized programs too
- But sequential consistency is *not necessary* for uni-processor-like behaviour of synchronized programs
- Define looser consistency models
  - Can be implemented more efficiently than sequential consistency

Memory Access Orderings

- Four possibilities:
  - R --> R, R --> W, W --> W, W --> R
- Sequential consistency guarantees all four orderings are preserved (in each processor)
- Define synchronization operation S
  - Synchronization acquire: Sa, release: Sr
- We only need to preserve:
  - W --> Sr, R --> Sr
  - Sa --> W, Sa --> R
  - S --> S

Relaxed Consistency Models

- Total Store Order (TSO), or Processor Consistency: relax W-->R
- Partial Store Order: relax W-->W also
- Weak Ordering: relax R-->R, R-->W also
- Release consistency: relax Sr-->W, Sr-->R, W-->Sa, R-->Sa