# LECTURE - 30

# Lecture Outline

- I/O and Buses
- Some queuing theory
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- ***Scribe for today?***

# Buses for Communication

- Between CPU/Memory, and with I/O devices
- Advantages:
  - Low-cost
  - Flexible/versatile
- Disadvantage:
  - Communication bottleneck
    - Bandwidth limited due to length, number of devices

# Bus Design Choices

- CPU/Memory buses vs. I/O buses
- Design choices in general:
  - Bus width
  - Data width
  - Transfer size
  - Number of masters
  - Split transaction
  - Synchronous vs. asynchronous

# Other Design Choices

- Connecting I/O to memory or cache
- Memory mapped vs. dedicated I/O instructions
- Polling vs. interrupt-driven
- Direct Memory Access (DMA)
  - I/O processors for more intelligence

# I/O Performance

- Producer-Server Model
- Throughput vs. Response Time
- Response time and think time
- Queuing theory
  - Arrival rate, service time, utilization
  - Little's law
  - Squared coefficient of variance
  - Average residual time
  - Response time and utilization
  - M/G/1 and M/M/1 models