

# Digital VLSI Testing

## Week 1 Assignment Solution

Q1. Primary objective of testing is to guarantee

- (A) Fault-free products
- (B) Detection of design error
- (C) Reduction of product cost
- (D) All of these

Ans: A

Q2. Rule of ten states that the cost of detecting faulty IC increases from device level to system level by an order of

- (A) 10
- (B) 100
- (C) 1000
- (D) 1

Ans: B

Q3. Input to a testing process

- (A) Test stimuli
- (B) Circuit under test
- (C) Both (A) and (B)
- (D) None of these

Ans: C

Q4. Output of a testing process

- (A) Test response
- (B) Circuit under test
- (C) Both (A) and (B)
- (D) None of these

Ans: A

Q5. Verification targets

- (A) Design errors
- (B) Manufacturing errors
- (C) Both (A) and (B)
- (D) None of these

Ans: A

Q6. Testing targets

- (A) Design errors
- (B) Manufacturing errors
- (C) Both (A) and (B)
- (D) None of these

Ans: B

Q7. In a certain batch of 10000 chips produced 100 are detected faulty at the manufacturing site while 10 more fails in the field. The yield of the process is

- (A) 99%
- (B) 98.5%
- (C) 90%
- (D) None of these

Ans: A

Q8. In the manufacturing process noted in Q7, the reject rate is

- (A) 98.5%
- (B) 0.1%
- (C) 90%
- (D) 0.2%

Ans: B

Q9. System availability is defined as the

- (A) Fraction of time system is operating normally
- (B) Total duration of time for which system is available
- (C) Fraction of time system is powered on
- (D) None of these

Ans: A

Q10. Online testing is done

- (A) When the system is powered on
- (B) Suspending system operation
- (C) Concurrently with system operation
- (D) Partially shutting down the system

Ans: C

Q11. Offline testing is done

- (A) Taking system out of service
- (B) Often periodically
- (C) Both (A) and (B)
- (D) None of these

Ans: C

Q12. Applying all possible test patterns to a CUT is called

- (A) Exhaustive testing
- (B) Complete testing
- (C) Functional testing
- (D) None of these

Ans: A

Q13. A quantity to measure quality of a test set is

- (A) Fault coverage
- (B) Test coverage
- (C) Total coverage
- (D) None of these

Ans: A

Q14. A PCB with 50 chips, each having 90% fault coverage and 90% yield has a reject rate of

- (A) 41.9%
- (B) 52.4%
- (C) 51.2%
- (D) None of these

Ans: B

Q15. With a multiple fault model with  $k$  types of faults, a circuit with  $n$  fault sites will have number of faults equal to

- (A)  $(k+1)^n$
- (B)  $(k+1)^n - 1$

- (C)  $k^n$
- (D)  $k^n - 1$

Ans: B

# Digital VLSI Testing

## Week 2 Assignment Solution

Q1. DFT stands for

- (A) Design Find Testability
- (B) Design Fine Testability
- (C) Design Future Testability
- (D) Design For Testability

Ans: D

Q2. Effort needed to test a circuit is called

- (A) Test complexity
- (B) Testability
- (C) Test effort
- (D) Relative testability

Ans: B

Q3. Controllability reflects difficulty to

- (A) Get a value at a primary output
- (B) Set a value at a primary output
- (C) Control all inputs of a logic gate
- (D) Set any line in the circuit to a desired value

Ans: D

Q4. Observability reflects difficulty to

- (A) Propagate primary input value to a point
- (B) Propagate a point value to a primary output
- (C) Observe primary output
- (D) Observe primary input

Ans: B

Q5. 0-controllability of a NAND gate is

- (A)  $1 - (\text{output } 1\text{-controllability})$
- (B)  $\prod (\text{input } 1\text{-controllabilities})$
- (C)  $\prod (\text{input } 0\text{-controllabilities})$
- (D)  $1 - \prod (\text{input } 0\text{-controllabilities})$

Ans: B

Q6. Three modes of operation in scan are

- (A) Normal, Shift, Capture
- (B) Normal, Scan, Capture
- (C) Scan, Shift, Capture
- (D) Normal, Scan, Shift

Ans: A

Q7. Inputs to a scan cell are

- (A) Data and Scan
- (B) Parallel and Serial
- (C) Parallel and Scan
- (D) Serial and Scan

Ans: A

Q8. Muxed-D scan cell has

- (A) A multiplexer and a latch
- (B) A multiplexer and a flipflop
- (C) A multiplexer or a latch
- (D) A multiplexer or a flipflop

Ans: B

Q9. Number of clocks in a clocked scan cell is

- (A) 1
- (B) 2
- (C) Any number
- (D) None of these

Ans B

Q10. Number of latches in a LSSD cell is

- (A) 1
- (B) 2
- (C) Any number
- (D) None of these

Ans: B

Q11. A partial scan design converts

- (A) 10% of its flipflops to scan
- (B) 1% of its flipflops to scan
- (C) Any number of flipflops to scan
- (D) None of these

Ans: C

Q12. Sequential depth of a structure graph is equal to its maximum

- (A) Level
- (B) Degree
- (C) Children
- (D) Nodes

Ans: A

Q13. Bus contention can occur during

- (A) Capture
- (B) Shift
- (C) Both A and B
- (D) None of these

Ans: B

Q14. Clock gating is

- (A) Good for testing
- (B) Good for design
- (C) Both A and B
- (D) None of these

Ans: B

Q15. Asynchronous set/reset is

- (A) Avoided for testing
- (B) May be used for design
- (C) Both A and B
- (D) None of these

Ans: C

# Digital VLSI Testing

## Week 3 Assignment Solution

1. Logic Simulation is performed to
  - a. Predicts the behaviour of faulty circuits
  - b. Find out the location of faults in faulty circuits
  - c. Predict the behaviour of a design prior to its physical realization
  - d. Optimize the number of logic gates used to design a circuit

ANSWER: c. Predict the behaviour of a design prior to its physical realization

2. What is the disadvantage of using ternary logic or three valued logic symbol?
  - a. Sequential circuits cannot be described using a three valued logic symbol
  - b. A signal may be reported as unknown when its value can be uniquely determined as '0' or '1'
  - c. Unnecessary use of the "UNKNOWN" logic states 'U' or 'X', which is not required
  - d. None of these

ANSWER: b. A signal may be reported as unknown when its value can be uniquely determined as '0' or '1'

3. Which of the following is not true for compiled code simulation?
  - a. It is a Cycle-based simulation method
  - b. It is highly efficient for low switching activity circuits
  - c. It is based on parallel simulation
  - d. The compilation time of compiled code simulation is its main drawback for larger circuits

ANSWER: b. It is highly efficient for low switching activity circuits

4. Which of the following is not true for Event driven simulation?
  - a. Can speed up the simulation process over compiled code simulation
  - b. Requires much complex scheduler and memory management
  - c. For a change in input vector, all the gates are evaluated
  - d. Efficient for low-activity circuits

ANSWER: c. For a change in input vector, all the gates are evaluated

5. Fault simulation detects
  - a. Fault coverage
  - b. Set of undetected faults
  - c. Faulty outputs
  - d. All of these

ANSWER: d. All of these

6. What is fault dropping?
- Randomly eliminating some of the faults from the fault list to save simulation time
  - Not performing the fault simulation of already detected faults
  - Not performing simulation of some of the faults with an hope that some future test pattern may detect the fault
  - Not performing simulation of some of the faults compromising on fault coverage

ANSWER: b. Not performing the fault simulation of already detected faults

7. What is not true for High-level programming language source code?
- It is easier to debug
  - It generates the target machine code directly
  - It can be ported to any target machine that has the compiler
  - Limited in applications due to long compilation time

ANSWER: b. It generates the target machine code directly

8. Complexity of deductive fault simulation technique is
- $O(n^3)$
  - $O(n^2)$
  - $O(n^2 \log n)$
  - $O(n \log n)$

ANSWER: b.  $O(n^2)$

9. Which of the following is not true for Deductive Fault Simulation
- Simulate all faults in one pass
  - Not easy to handle unknowns
  - Applicable for gate delay timing model
  - Suffers from memory management problem

ANSWER: c. Applicable for gate delay timing model

10. For sequential circuits, which of the fault simulation is the most popular?
- Differential fault simulation
  - Parallel pattern single fault propagation
  - Concurrent fault simulation
  - Both A and C

ANSWER: d. Both A and C

11. What is dynamic hazard?
- The transient pulse on a signal line whose value does not change
  - The transient pulse during a 0-to-1 transition
  - The transient pulse during a 1-to-0 transition

- d. Both B and C

Answer: d. Both B and C

12. Which of the following fault simulation strategy is not capable of delay and functional modelling?
- a. Parallel fault simulation
  - b. Deductive fault simulation
  - c. Concurrent fault simulation
  - d. Both A and B

ANSWER: D. Both A and B

13. Which of the following fault simulation strategy is the fastest?
- a. Parallel fault simulation
  - b. Differential fault simulation
  - c. Deductive fault simulation
  - d. Concurrent fault simulation

ANSWER: b. Differential fault simulation

14. For a sufficiently large circuit, comparatively which of the following fault simulation technique suffers from shortage of memory problem?
- a. Parallel fault simulation
  - b. Differential fault simulation
  - c. Deductive fault simulation
  - d. Concurrent fault simulation

ANSWER: d. Concurrent fault simulation

15. For which of the following fault simulation techniques, multi-values fault simulation is the most challenging?
- a. Serial fault simulation
  - b. Differential fault simulation
  - c. Parallel fault simulation
  - d. Concurrent fault simulation

ANSWER: c. Parallel fault simulation

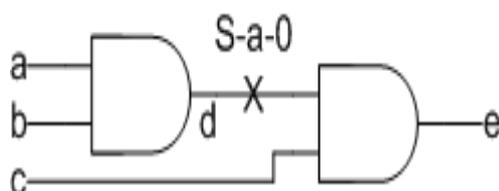
## Digital VLSI Testing

### Week 4 Assignment Solution

1. ATPG stands for
  - a) Advanced Test Pattern Generator
  - b) Active Test Pattern Generator
  - c) Automatic Test Pattern Generator
  - d) Both b and c

ANSWER: (c) Automatic Test Pattern Generator

2. Determine the test vector generated by ATPG to detect a stuck-at-0 (S-a-0) fault at the net 'd' in the given circuit.



- a)  $a = 0, b = 1, c = 0$
- b)  $a = 0, b = 1, c = 1$
- c)  $a = 1, b = 1, c = 0$
- d)  $a = 1, b = 1, c = 1$

ANSWER: (d)  $a = 1, b = 1, c = 1$

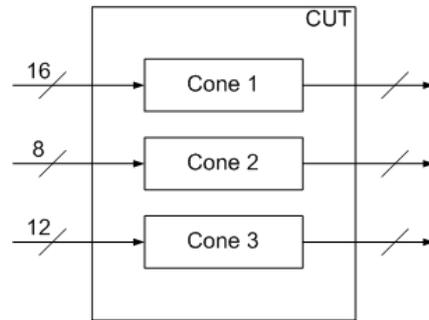
3. For a 4-bit ripple carry adder with all full adders, the probability of detecting a stuck-at-1 fault at one of its output bits, given the test set contains 50 test vectors, is
  - a)  $50/256$
  - b)  $206/256$
  - c)  $50/512$
  - d)  $462/512$

ANSWER: (c)  $50/512$

4. The total number of test patterns required to exhaustively test a 128-to-1 multiplexer with minimum number of select lines is
  - a)  $2^{128}$
  - b)  $2^{135}$
  - c)  $2^{256}$
  - d)  $2^{121}$

ANSWER: (b)  $2^{135}$

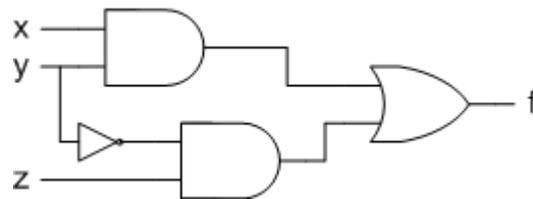
5. A circuit under test (CUT) is divided into three partitions (cones) as shown below. The total number of test patterns required to pseudo exhaustively test the CUT is



- a)  $2^{16+8+12}$   
 b)  $2^{16} + 2^8 + 2^{12}$   
 c)  $2^{16 \times 8 \times 12}$   
 d)  $2^{16} \times 2^8 \times 2^{12}$

ANSWER: (b)  $2^{16} + 2^8 + 2^{12}$

6. The Boolean expression obtained, using Boolean difference, to excite a stuck-at-1 fault at the input 'y' of the following circuit is



- a)  $xy\bar{z} + \bar{x}yz$   
 b)  $x\bar{y}z + \bar{x}yz$   
 c)  $x\bar{y}\bar{z} + \bar{x}\bar{y}z$   
 d)  $x\bar{y}\bar{z} + \bar{x}yz$

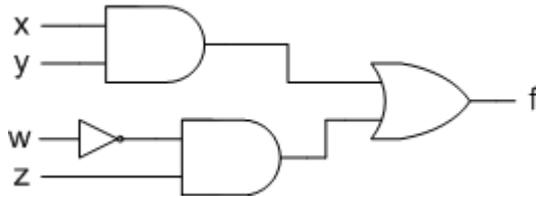
ANSWER: (c)  $x\bar{y}\bar{z} + \bar{x}\bar{y}z$

7. Consider a combinational CUT with five inputs a, b, c, d, and e. The number of possible test vectors, according to Branch-and-Bound search tree, that correspond to the solution space with a = 0, b = 1, and c = 0 is

- a) 8  
 b) 4  
 c) 32  
 d) 1

ANSWER: (b) 4

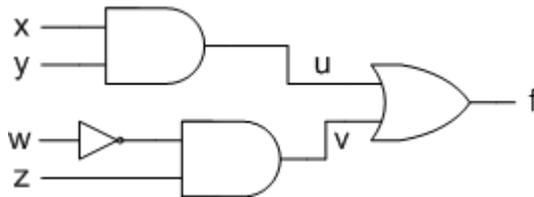
8. In the following circuit, to detect a stuck-at-1 fault at 'f' using basic ATPG for fanout-free circuits, which of the following recursive calls are necessary to excite the fault?



- a) JustifyFanoutFree(C,f,0)
- b) JustifyFanoutFree(C,x,0)
- c) Both a and b
- d) None of the above

ANSWER: (c) Both a and b

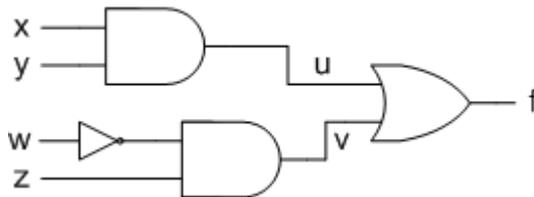
9. Which of the following recursive calls are not necessary, assuming they are executed one after the other, to propagate a fault-effect from 'v' to 'f', in the circuit given below.



- a) PropagateFanoutFree(C,v)
- b) JustifyFanoutFree(C,u,0)
- c) JustifyFanoutFree(C,u,1)
- d) JustifyFanoutFree(C,y,0)

ANSWER: (c) JustifyFanoutFree(C,u,1)

10. Applying the knowledge of D-algorithm, determine the test vector to propagate a stuck-at-1 fault at net 'v' in the circuit given below.



- a)  $x = 0, y = 0, w = 1, z = 0$
- b)  $x = 0, y = 0, w = 0, z = 0$
- c)  $x = 0, y = 1, w = 1, z = 0$
- d) Any of the above

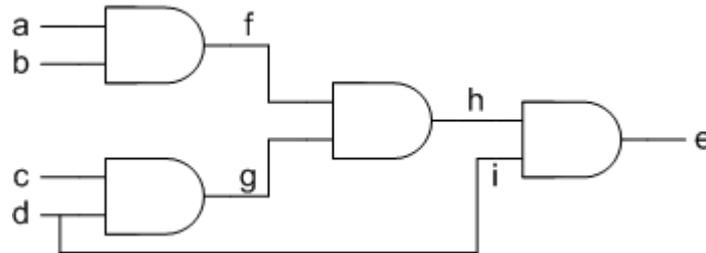
ANSWER: (d) Any of the above

11. PODEM stands for

- a) Peak Output Decision Making
- b) Path Oriented Decision Making
- c) Path Output Decision Making
- d) Peak Oriented Decision Making

ANSWER: (b) Path Oriented Decision Making

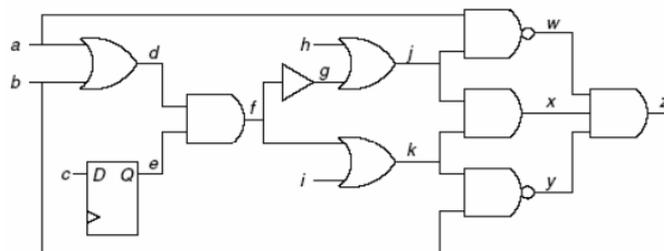
12. Applying the knowledge of PODEM algorithm, determine which of the following faults become untestable for the circuit given below.



- a) Stuck-at-1 at 'i'
- b) Stuck-at-1 at 'g'
- c) Stuck-at-0 at 'i'
- d) Stuck-at-1 at 'h'

ANSWER: (a) Stuck-at-1 at 'i'

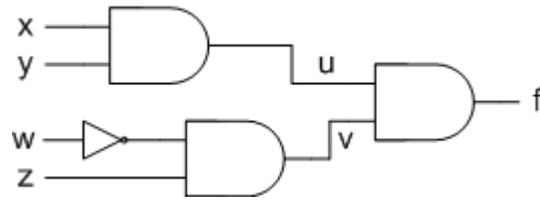
13. For the circuit given below, which of the following are a subset of direct implications for  $d = 0$ ?



- a)  $a = 1, b = 0, f = 1$
- b)  $a = 0, b = 1, f = 1$
- c)  $a = 0, b = 0, f = 0$
- d)  $a = 0, b = 0, f = 1$

ANSWER: (c)  $a = 0, b = 0, f = 0$

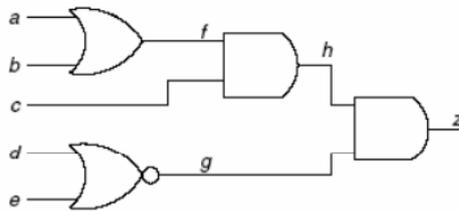
14. Which of the following faults for the given circuit are undetectable when  $y = 0$ ?



- a) 'f' stuck-at-1
- b) 'u' stuck-at-1
- c) 'v' stuck-at-1
- d) 'y' stuck-at-1

ANSWER: (c) 'v' stuck-at-1

15. For the circuit shown below, which of the following combinations may raise a multiline conflict?



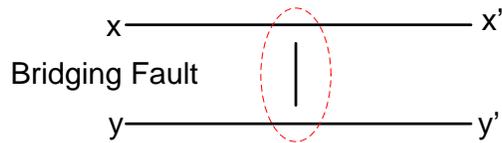
- a)  $f = 1, h = 1, z = 0$
- b)  $f = 1, h = 0, z = 1$
- c)  $f = 1, h = 1, z = 1$
- d)  $b = 1, c = 0, h = 0$

ANSWER: (b)  $f = 1, h = 0, z = 1$

# Digital VLSI Testing

## Week 5 Assignment Solution

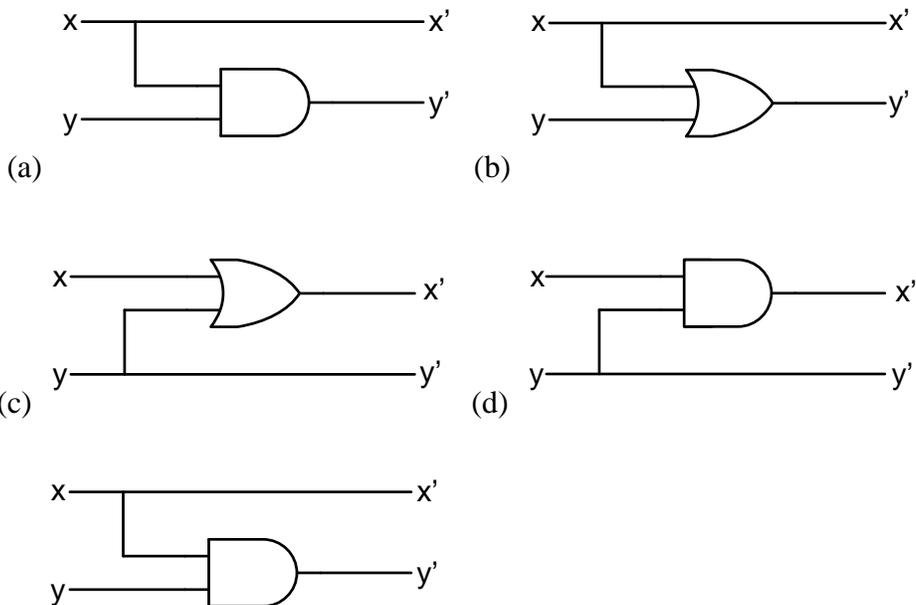
1. In which of the following condition(s) bridging fault can be ignored?



- a.  $X = 1$  and  $Y = 1$
- b.  $X = 0$  and  $Y = 0$
- c.  $X = 1$  and  $Y = 0$
- d. Both A and B

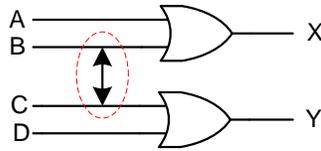
ANSWER: d. Both A and B

2. For the bridge-fault type  $x \text{ Dom}0 y$  ( $x$  dominated  $y$  if  $x = 0$ ), which of the following fault model should be considered.



ANSWER: a.

3. For the circuit given below, if there exists an AND bridge fault between the nets B and C, which of the following test vector (A,B,C,D) can be used detect the fault.



- (a) (0,0,1,0)
- (b) (1,0,1,1)
- (c) (a) & (b) both
- (d) None of them

ANSWER: a. (0, 0, 1, 0)

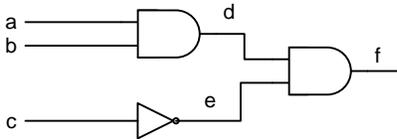
4. Select the Test Vector such that all the faults (f1-f5) can be detected using minimum number of test vectors.

	F1	F2	F3	F4	F5
V1	×		×		×
V2				×	
V3	×	×			
V4	×				×

- (a) V1,V2,V3
- (b) V1,V3,V4
- (c) V2,V3,V4
- (d) V1,V2,V4

ANSWER: a. V1, V2, V3

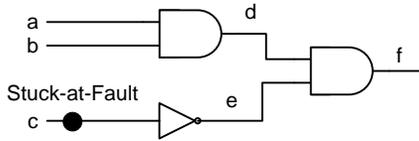
5. For the rising path  $\uparrow bdf$  in the circuit below



- (a) a,c ,e are the off inputs
- (b) a,c are the off inputs
- (c) a,e are the off inputs
- (d) none of the above is true

ANSWER: c. a,e are the off inputs

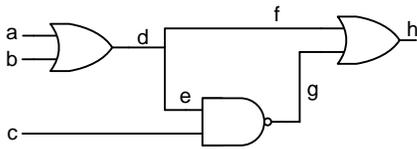
6. The rising path  $\uparrow bdf$  in the circuit below, which of the following statement is true



- (a) Single Path Sensitizable , if c has s-a-0 fault
- (b) Single Path Sensitizable , if c has s-a-1 fault
- (c) For both the cases
- (d) Single Path Unsensitizable

ANSWER: a. Single Path Sensitizable , if c has s-a-0 fault

7. For the following path  $\downarrow$ bdfgh in then given circuit, which of the following statement is true



- (a) Robustly Testable
- (b) Unrobustly Testable
- (c) False Path
- (d) None of the above

ANSWER: b. Unrobustly Testable

8. Using the Five-valued System, solve the following equation:  $S0 \text{ XNOR } U1 = ?$

- (a) U0
- (b) S0
- (c) U1
- (d) None of them

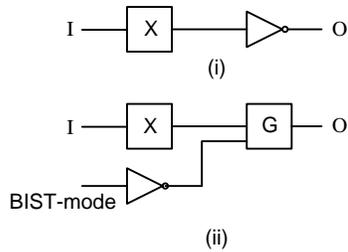
ANSWER: a. U0

9. Unknown sources resulting from combinational feed back loops can be avoided in BIST using

- (a) 0-control point
- (b) 1-control point
- (c) Bypass logic
- (d) Scan point

ANSWER: d. Scan point

10. To block the unknown source in circuit (i) using embedded 1-control point, what should be the two input gate placed in place of block G in the circuit (ii)?



- (a) AND Gate
- (b) OR Gate
- (c) NAND Gate
- (d) NOR Gate

ANSWER: c. NAND Gate

11. One-hot decoder is used in BIST to avoid bus contentions arising due to

- (a) Tri-state Buses
- (b) False Paths
- (c) Floating Ports
- (d) Multi-Cycle Paths

ANSWER: d. Multi-Cycle Paths

12. Which of the following statement is false

- (a) In Psuedo-Random Testing it is difficult to determine the fault coverage
- (b) In Psuedo-Random Testing it is difficult to determine the required test length
- (c) Binary counters are used in Exhaustive Testing
- (d) Maximum Length LFSR are used in Exhaustive Testing

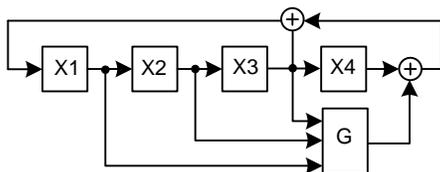
ANSWER: d. Maximum Length LFSR are used in Exhaustive Testing

13. Which of the following circuit is RP resistant?

- (a) A 5-i/p OR gate with a single s-a-0 fault at the o/p node
- (b) A 5-i/p AND gate with a single s-a-1 fault at the o/p node
- (c) A 5-i/p NAND gate with a single s-a-1 fault at the o/p node
- (d) A 5-i/p NOR gate with a single s-a-1 fault at the o/p node

ANSWER: c. A 5-i/p NAND gate with a single s-a-1 fault at the o/p node

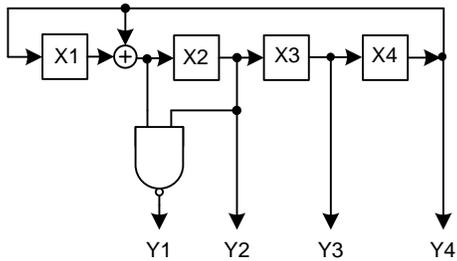
14. Replace block G with a 3 i/p logic gate such that the following circuit becomes a complete LFSR



- (a) With a 3 i/p AND gate
- (b) With a 3 i/p NAND gate
- (c) With a 3 i/p OR gate
- (d) With a 3 i/p NOR gate

ANSWER: d. With a 3 i/p NOR gate

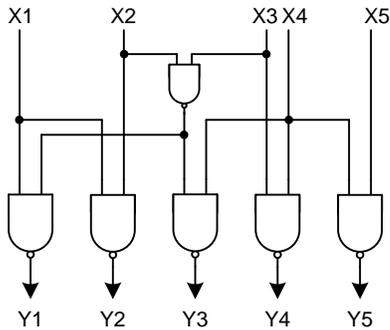
15. For a weighted LFSR shown in the figure below, what should be the probability of obtaining a logic 1 value at Y1, when the probability of obtaining a logic 1 value at X1, X2, X3, X4 are P1, P2, P3 and P4 respectively.



- (a)  $P2 * [P1 * (1 - P4) + P4 * (1 - P1)]$
- (b)  $P1 * P2$
- (c)  $P1 * P2 * P3$
- (d)  $P4 * [P1 * (1 - P2) + P2 * (1 - P1)]$

ANSWER: a.  $P2 * [P1 * (1 - P4) + P4 * (1 - P1)]$

16. A Psuedo-Exhaustive Pattern Generator will consider the following circuit as



- (a) (5,1) CUT
- (b) (5,2) CUT
- (c) (5,3) CUT
- (d) (5,4) CUT

ANSWER: c. (5,3) CUT

## Digital VLSI Testing

### Week 6 Assignment Solution

1. As the gate count of a circuit increases, the volume of test data required for testing the circuit \_\_\_\_\_.
  - a. Increases exponentially
  - b. Increases linearly
  - c. Remains constant
  - d. None of the above

Answer: (a) Increases exponentially

2. Which of the following is not a feature of test data compression?
  - a. Reduce test data volume
  - b. Reduce test time
  - c. Increase fault coverage
  - d. Reduce the memory cost in the ATE.

Answer: (c) Increase fault coverage

3. Which of the following in test compression architecture is true?
  - i) Compressed stimulus → Decompressor → Stimulus
  - ii) Response → Compactor → Compressed Response
  - a. Only (i)
  - b. Only (ii)
  - c. Both (i) and (ii)
  - d. None of the above.

Answer: (c) Both (i) and (ii)

4. In Huffman code, for test stimulus compression, input symbols and output code words
  - a. Symbols have fixed size while code words have variable sizes.
  - b. Symbols have variable sizes while code words have fixed size.
  - c. Both symbol and code words are having fixed size.
  - d. Both symbol and code words have variable sizes.

Answer: (a) Symbols have fixed size while code words have variable sizes.

5. For a dictionary based coding with a dictionary of size D, the length of the code words whose representative are stored in the dictionary is
  - a. D
  - b. D + 1
  - c.  $\lceil \log_2 D \rceil + 1$
  - d.  $\log_2(D + 1)$

Answer: (c)  $\lceil \log_2 D \rceil + 1$

6. For a circuit with N scan chains the code length of the non-dictionary element of a dictionary based coding with dictionary size D

- a. N
- b. N+1
- c.  $\lceil \log_2 D \rceil + 1$
- d.  $\log_2(N + 1)$

Answer: (b) N+1

7. Between Illinois scan and Broadcast scan method, which of the following have higher fault coverage?
- a. Illinois scan method
  - b. Broadcast scan method
  - c. Both of them have same fault coverage
  - d. Cannot be determined

Answer: (a) Illinois scan method

8. The drawback of Illinois scan which operated in serial scan mode
- a. Fault coverage decreases
  - b. Compression ratio decreases
  - c. Area overhead increases
  - d. Both a and b

Answer: (b) Compression ratio decreases

9. Table I shows an Input test set and the corresponding Huffman codes for it. If we implement selective Huffman coding, then what should be the length of the output test set. [When the length of the output test set is 240 bits as shown in the table I. Consider 3 most frequently occupied patterns to be coded only]

Symbol	Frequency	Pattern	Huffman Code
S <sub>0</sub>	22	0010	10
S <sub>1</sub>	13	0100	00
S <sub>2</sub>	7	0110	110
S <sub>3</sub>	5	0111	010
S <sub>4</sub>	3	0000	0110
S <sub>5</sub>	2	1000	0111
S <sub>6</sub>	2	0101	11100
S <sub>7</sub>	1	1011	111010
S <sub>8</sub>	1	1100	111011
S <sub>9</sub>	1	0001	111100
S <sub>10</sub>	1	1101	111101
S <sub>11</sub>	1	1111	111110
S <sub>12</sub>	1	0011	111111
S <sub>13</sub>	0	1110	—
S <sub>14</sub>	0	1010	—
S <sub>15</sub>	0	1001	—

- a. 194
- b. 181
- c. 145
- d. 168

Answer: (a) 194

10. For the test pattern given below, form blocks each of which consist of 3 bits. What should be the length of the Huffman coded output test set in bits?

“101100101000110101100”

- a. 11
- b. 12
- c. 13
- d. 14

Answer: (c) 13

11. What should be the minimum length of the output coded (compressed) sequence using Run-Length code for the following test set? [For reference see the table below]

“100100010000000101001101”

Symbol	Codeword
1	000
01	001
001	010
0001	011
00001	100
000001	101
0000001	110
0000000	111

- a. 27
- b. 24
- c. 18
- d. 21

Answer: (a) 27

12. Assume that a CUT produces 16 8-bit wide output patterns. Determine the number of output patterns, if the output patterns from the CUT are sent through a space compactor that has a compaction factor of 2.

- a. 16
- b. 8
- c. 4
- d. 32

Answer: (a) 16

13. Assume that a CUT produces 8 16-bit wide output patterns. Determine the width of output patterns, if the output patterns from the CUT are sent through a time compactor that has a compaction factor of 2.

- a. 8
- b. 16
- c. 4
- d. 2

Answer: (b) 16

14. Assume that a CUT produces 16 8-bit wide output patterns. Determine the number of output patterns, if the output patterns from the CUT are sent through a time compactor that has a compaction factor of 4.

- a. 16
- b. 8
- c. 4
- d. 32

Answer: (c) 4

15. Assume that a CUT produces 16 8-bit wide output patterns. Determine the width of output patterns, if the output patterns from the CUT are sent through a space compactor that has a compaction factor of 4.

- a. 16
- b. 8
- c. 4
- d. 2

Answer: (d) 2

## Digital VLSI Testing

### Week 7 Assignment Solution

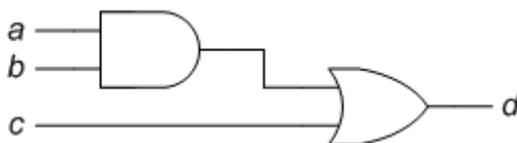
1. Which of the following statements is false?
  - a. Power consumption of a circuit is lower in normal mode than in test mode.
  - b. Test power depends on successive test patterns.
  - c. DFT circuitry is utilized more in normal mode than in test mode.
  - d. Switching activity of nodes of a circuit is more in test mode than in normal mode.

ANSWER: (c) DFT circuitry is utilized more in normal mode than in test mode.

2. A CUT has four independent blocks, B1, B2, B3, and B4, whose test power consumption values are given as 100 mW, 150 mW, 200 mW, and 500 mW, respectively. If said that the maximum power consumption of the CUT should not exceed 800 mW at test, which of the following are valid?
  - a. Testing of B1, B2, B3, and B4 together.
  - b. Testing of B4, B2, and B3 together.
  - c. Testing of B1, B2, and B4 together.
  - d. All of the given options.

ANSWER: (c) Testing of B1, B2, and B4 together.

3. For the circuit given below, determine the total switching power at the output signal, for the given transitions at the inputs:  $abc: 000 \rightarrow 010 \rightarrow 110 \rightarrow 101 \rightarrow 111$ . For each transition at the output, the power consumed is  $1 \mu\text{W}$ .



- a.  $5 \mu\text{W}$
- b.  $1 \mu\text{W}$
- c.  $2 \mu\text{W}$
- d.  $3 \mu\text{W}$

ANSWER: (b)  $1 \mu\text{W}$

4. Which of the following test patterns has got minimum transition in its signals?
  - a.  $1110 \rightarrow 1011 \rightarrow 0110 \rightarrow 1100$
  - b.  $0100 \rightarrow 1100 \rightarrow 1000 \rightarrow 0000$
  - c.  $0001 \rightarrow 1110 \rightarrow 1111 \rightarrow 0000$
  - d. All have equal number of transitions

ANSWER: (b)  $0100 \rightarrow 1100 \rightarrow 1000 \rightarrow 0000$

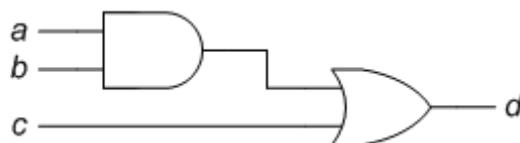
5. Which of the following statements is TRUE?
- External circuit testing, using an ATE, does not have the provision of omitting redundant test patterns.
  - Internal circuit testing, using a BIST, does not have the provision of omitting redundant test patterns.
  - Both BIST based testing and ATE based does not have the provision of omitting redundant test patterns.
  - None of the given options.

ANSWER: (b) Internal circuit testing, using a BIST, does not have the provision of omitting redundant test patterns.

6. An 8-bit LFSR is used to generate pseudo-random vectors to test a CUT using BIST technique. Of the vectors generated, only 139 are found to be useful in detecting faults of the CUT. Determine the maximum number of times the transmission gates network gets disabled, if Vector Filtering technique is applied to the BIST.
- 115
  - 139
  - 117
  - 116

ANSWER: (d) 116

7. Determine the contents of the seed memory, if Re-seeding LFSR technique is applied in BIST, to test the following CUT for Stuck-at faults at  $c$ .



- 001, 000
- 100, 110
- 010, 111
- Any of the above

ANSWER: (a) 001, 000

8. For LFSR tuning in BIST, the parameters that can be controlled are
- Size and Speed
  - Polynomial and Size
  - Speed and Seed value

d. Polynomial and Seed value

ANSWER: (d) Polynomial and Seed value

9. A clash occurs when

- a. the MSB of the last response differs from the LSB of next test vector
- b. the LSB of the last response differs from the MSB of next test vector
- c. the MSB of the last response and the LSB of next test vector are same
- d. the LSB of the last response and the MSB of next test vector are same

ANSWER: (a) the MSB of the last response differs from the LSB of next test vector

10. What is the advantage of clock gating?

- a. It helps to reduce the number of test pattern to test a circuit
- b. It improves the fault coverage
- c. It helps to reduce the test mode power
- d. It reduces the test application time

ANSWER: (c) It helps to reduce the test mode power

11. For the following test vector, what will be the minimum value of transition count if we fill all the don't-cares using minimum transition filling?

01XX10X0XXX1X0XX1XX1XXX100010X0X

- a. 12
- b. 10
- c. 8
- d. 11

ANSWER: (c) 8

12. Power aware test scheduling may

- a. Reduce the total test time
- b. Increase the total test time
- c. Increases fault coverage
- d. Increases the temperature of the circuit

ANSWER: (b) Increase the total test time

13. The don't care bits in the test patterns can be filled to achieve

- a. Low test power
- b. Low test data volume
- c. Both low test power and low test data volume simultaneously

- d. Both low test power and low test data volume, but not simultaneously

ANSWER: (d) Both low test power and low test data volume, but not simultaneously

14. In Testing the successive test patterns are expected to be

- a. Highly correlated
- b. Highly uncorrelated
- c. Exactly same
- d. Can be either correlated or uncorrelated

ANSWER: (b) Highly uncorrelated.

15. The dynamic power of a circuit can be calculated as (C = capacitance,  $V_{DD}$  = supply voltage, f = operating frequency,  $\alpha$  = transition probability )

- a.  $P = CV_{DD}^2 f \alpha$
- b.  $P = CV_{DD} f \alpha$
- c.  $P = C^2 V_{DD} f \alpha$
- d.  $P = (CV_{DD})^2 f \alpha$

ANSWER: (a)  $P = CV_{DD}^2 f \alpha$

# Digital VLSI Testing

## Week 8 Assignment Solution

1. Input Cone of Dependency of a line in a circuit suggests
  - a. The primary outputs to which the effect of the line is propagating
  - b. The primary inputs that are affecting the line
  - c. The fanout cone of the line
  - d. None of the given options

ANSWER: b. The primary inputs that are affecting the line

2. Drawback of the Hamming Distance based thermal-aware test vector reordering approach is
  - a. It may lead to an increase in the transitions at primary inputs other than in the cone of hottest blocks
  - b. It increases the transitions at primary inputs other than in the cone of hottest blocks as well as increases average temperature.
  - c. It concentrate on minimizing circuit transitions rather than peak temperature of the circuit
  - d. Average temperature of the chip increases

ANSWER: b. It increases the transitions at primary inputs other than in the cone of hottest blocks as well as increases average temperature.

3. The drawback of HPSO (Thermal Simulator Integrated PSO) is
  - a. It cannot accurately estimate the temperature
  - b. Time complexity becomes very large
  - c. Space complexity becomes very large
  - d. Fault coverage drops down

ANSWER: b. Time complexity becomes very large

4. In the context of thermal aware don't care filling which flip-flops are called critical flip-flops of a particular block?
  - a. Only the flip-flops which belong to that block
  - b. The flip-flops which are only in the near fan-in cone of a gate within the block
  - c. All the flip-flops which are critically damaged due to heating
  - d. The flip-flops which are either within the block or in the near fan-in cone of a gate within the block

ANSWER: d. The flip-flops which are either within the block or in the near fan-in cone of a gate within the block

5. The drawback of PEAKASO algorithm is
  - a. It concentrate on minimizing circuit transitions rather than peak temperature of CUT
  - b. The time complexity of the algorithm is very large
  - c. The average temperature of the CUT increase
  - d. Both a and c

ANSWER: d. Both a and c

6. You are given the following two sets of test vectors. What is the Hamming Distance between them?

100011010110101

110101110110010

- a. 9
- b. 8
- c. 7
- d. 6

ANSWER: c. 7

7. *G<sub>best</sub>* for a PSO algorithm indicates

- a. Initial set of random solution.
- b. The position vector of the best solution this particle has achieved so far.
- c. The best position, obtained so far, by any particle in the population.
- d. The final best solution.

ANSWER: c. The best position, obtained so far, by any particle in the population.

8. What is the advantage of Particle Swarm Optimization over Genetic Algorithm?

- a. PSO concentrates in smaller search space, thus gives more optimized results
- b. PSO has lesser number of tuning parameters than GA
- c. PSO is faster than GA
- d. Both b and c

ANSWER: d. Both b and c

9. In the context of thermal-aware don't-care filling, what does a high weightage factor of a block signifies?

- a. The block will consume more power when transitions occur at the flip-flops
- b. The block will consume less power when transitions occur at the flip-flops
- c. The block contains more number of flip-flops
- d. The block contains more number of logic gates

ANSWER: a. The block will consume more power when transitions occur at the flip-flops

10. What does a Vector Filtering BIST do?

- a. It filter out the don't-care bits in the generated test patterns
- b. It inhibits the test patterns, which don't detect any new faults, from reaching to the circuit
- c. It filter out the test patterns with high transition probability
- d. None of the options

ANSWER: b. It inhibits the test patterns, which don't detect any new faults, from reaching to the circuit

11. The four mandatory pins of a test access port in boundary scan are

- a. TDI, TDO, TMS, TCK
- b. TDI, TDO, TRST, TCK
- c. TDI, TDO, TMS, TRST
- d. TDI, TRST, TMS, TCK

ANSWER: a. TDI, TDO, TMS, TCK

12. Operation modes of BSC are

- a. Normal, Shift, Capture, Update
- b. Normal, Scan, Capture, Output
- c. Scan, Shift, Catch, Output

- d. Scan, Capture, Update, Output

ANSWER: a. Normal, Shift, Capture, Update

13. Steps in an execution of INTEST instruction are

- a. Shift-DR – Update-DR – Shift-DR – Capture-DR
- b. Shift-DR – Capture-DR – Update-DR – Shift-DR
- c. Shift-DR – Update-DR – Capture-DR – Shift-DR
- d. Shift-DR – Capture-DR – Shift-DR – Update-DR

ANSWER: c. Shift-DR – Update-DR – Capture-DR – Shift-DR

14. Steps in an EXTEST interconnection to test interconnection from Chip1 and Chip2 are

- a. Shift-DR (Chip1) – Update-DR (Chip1) – Capture-DR (Chip 2) – Shift-DR (Chip 2)
- b. Shift-DR (Chip1) – Capture-DR (Chip 2) – Update-DR (Chip1) – Shift-DR (Chip 2)
- c. Shift-DR (Chip2) – Update-DR (Chip2) – Capture-DR (Chip 1) – Shift-DR (Chip 1)
- d. Shift-DR (Chip2) – Capture-DR (Chip 1) – Update-DR (Chip 2) – Shift-DR (Chip 1)

ANSWER: a. Shift-DR (Chip1) – Update-DR (Chip1) – Capture-DR (Chip 2) – Shift-DR (Chip 2)

15. Which of the following functions is not provided by the TAP controller?

- a. Perform test capture operation
- b. Perform test update operation
- c. Perform test data compression
- d. Shift test data in and out.

ANSWER: c. Perform test data compression

# Digital VLSI Testing

## Week 9 Assignment Solution

1. VSIA stands for
  - a. Virtual System Interface Alliance
  - b. Virtual Standards Interface Alliance
  - c. Virtual Socket Interface Alliance
  - d. Virtual Silicon Interface Alliance

ANSWER: c. Virtual Socket Interface Alliance

2. The standard that has been announced to facilitate SoC testing is
  - a. IEEE 1149
  - b. IEEE 1500
  - c. IEEE 1149.1
  - d. IEEE 1149.6

ANSWER: b. IEEE 1500

3. Which of the following factors can create conflicts while performing test scheduling of an embedded core-based SoC?
  - a. SoC test time, test precedence constraints, SoC area, and SoC power
  - b. SoC test time, SoC area, SoC power, and sharing of TAMs
  - c. SoC test time, SoC power, test precedence constraints, and sharing of TAMs
  - d. SoC area, SoC power, and SoC test time

ANSWER: c. SoC test time, SoC power, test precedence constraints, and sharing of TAMs

4. Which of the following are the wrapper modes of an IEEE 1500 wrapper?
  - a. Normal, Serial Test, Parallel Test, Bypass
  - b. Normal, Serial, I-T Test, Bypass
  - c. Normal, Serial, Exttest, Bypass
  - d. Any of the given options

ANSWER: c. Normal, Serial, Exttest, Bypass

5. Which of the following are the events of WBR (WBC)
  - a. Shift, Capture, Import, Update, Transfer
  - b. Shift, Update, Capture, Apply, Transfer
  - c. Capture, Update, Apply, Transfer, Import
  - d. None of the given options

ANSWER: b. Shift, Update, Capture, Apply, Transfer

6. Which of the following statements are true?
  - a. CTAG is associated with the cores that deploy IEEE 1500 test standard
  - b. JTAG is associated with the cores that deploy IEEE 1149.1 test standard
  - c. Both (a) and (b) are true
  - d. Both (a) and (b) are false

ANSWER: c. Both (a) and (b) are true

7. What is the functionality of TAM?
  - a. It transports test data from the source to the core and from the core to the sink
  - b. In transports control signal from the source to the core and from the core to the sink
  - c. It performs test scheduling
  - d. It isolates an embedded core from the surrounding logic

ANSWER: a. It transports test data from the source to the core and from the core to the sink

8. What is the functionality of a test wrapper?
  - a. Wrapper acts as a communication bridge between the TAM and the core
  - b. Wrapper isolates an embedded core from the surrounding logic
  - c. Wrapper provides width adaptation between core I/O pins and TAM pins
  - d. All of these

ANSWER: d. All of these

9. How can you address the problem of long test application time in SoC Testing?
  - a. Serial testing of all the cores
  - b. Parallel testing of all the cores
  - c. An efficient test scheduling strategy
  - d. Both b and c

ANSWER: d. Both (b) and (c)

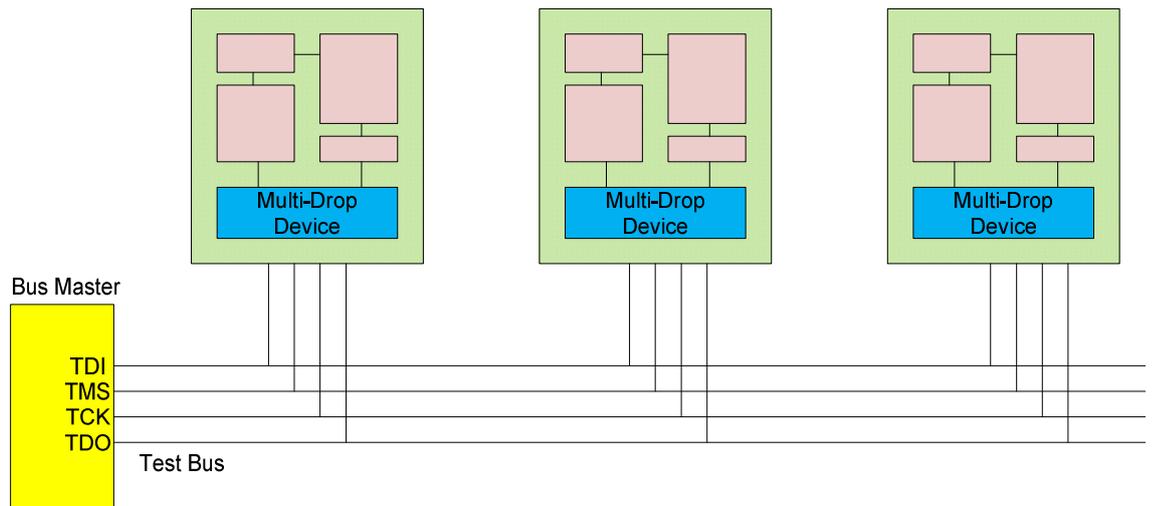
10. Which of the following is the goal of IEEE 1500 Core Test Standard?
  - a. Test the cores using 1500 TAM lines
  - b. Define test interface between core and SoC
  - c. Designing a test scheduling strategy
  - d. Calculating the fault coverage

ANSWER: b. Define test interface between core and SoC

11. Which of the following is not a Wrapper Series Control signal?
  - a. SelectWIR
  - b. CaptureWR
  - c. ModifyWR
  - d. TransferDR

ANSWER: c. ModifyWR

12. The following architecture of Bus Master for Chip with Boundary Scan is a



- a. Ring architecture with shared TMS
- b. Ring architecture with separated TMS
- c. Star architecture
- d. Multi-Drop Architecture

ANSWER: d. Multi-Drop Architecture

13. Which of the following statements are true?

- a. Test Standard 1149.1 is used for board level testing and 1150 is used for core level testing
- b. Test Standard 1149.1 is used for core level testing and 1150 is used for board level testing
- c. Both Test Standard 1149.1 and 1150 are used for both board level testing
- d. Both Test Standard 1149.1 and 1150 are used for both core level testing

ANSWER: a. Test Standard 1149.1 is used for board level testing and 1150 is used for core level testing

14. Embedded core test requires the following hardware components :

- A) A wrapper
  - B) A source/sink for test patterns
  - C) A on-chip Test Access Mechanism (TAM)
- a. A and B only
  - b. B and C only
  - c. A and C only
  - d. A, B and C

ANSWER: d. A, B and C

15. Which of the following techniques can be used to avoid SoC test problems arises due to the deeply embedded cores present on a chip?

- a. DFT

- b. BIST
- c. Design of Proper Test Access Mechanism
- d. Hierarchical test management

ANSWER: d. Hierarchical test management

## Digital VLSI Testing

### Week 10 Assignment Solution

1. Which of the following statements is true in the context of Wrapper Operation Modes?
  - a. In normal mode, the functional inputs of a core are connected to its functional outputs
  - b. In serial bypass mode, the functional inputs of a core are connected to its functional outputs
  - c. Both (a) and (b)
  - d. None of the given options

ANSWER: (a) In normal mode, the functional inputs of a core are connected to its functional outputs

2. Which of the following statements are false in the context of Wrapper Operation Modes?
  - a. In serial internal test mode, the serial test input passes through the internal scan chains present in a core
  - b. In serial external test mode, the serial input does not pass through the internal scan chains present in a core
  - c. Both (a) and (b)
  - d. None of the given options

ANSWER: (d) None of the given options

3. A core has got three functional inputs, two functional outputs, and three internal scan chains, each containing five flip-flops. Determine the minimum number of cycles needed for testing the core with a wrapper, if the number of TAM lines is two.
  - a. Five
  - b. Ten
  - c. Fifteen
  - d. Twenty

ANSWER: (b) Ten

SOLUTION: There are three functional inputs, two functional outputs, and three internal scan chains each with five flip-flops. Thus there are a total of twenty flip-flops. If the number of TAM lines available is two, then they can be equally divided among the flip-flops, which results in ten flip-flops per a TAM line. Thus, the minimum number of cycles needed to test such a core with the given TAM line constraint is TEN.

4. Which of the following is not a TAM type?
  - a. Multiplexed access
  - b. Transparent paths
  - c. Reuse system bus

- d. Isolation bus

ANSWER: (d) Isolation bus

- 5. Test rail TAM architecture is a combination of
  - a. Daisy chain and multiplexed architectures
  - b. Daisy chain and distributed architectures
  - c. Multiplexed and distributed architectures
  - d. Daisy chain, multiplexed, and distributed architectures

ANSWER: (b) Daisy chain and distributed architectures

- 6. A SoC consists of seven cores (C0 through C6), of which C0, C1, and C2 share a test bus, C3 and C4 share a test bus, and the remaining cores share a test bus. Given the test times of cores C0 through C6 as 200, 130, 400, 530, 230, 550, and 110, respectively. Determine the test time of the SoC, provided the cores that share a TAM are tested serially.
  - a. 2150
  - b. 730
  - c. 760
  - d. 660

ANSWER: (c) 760

SOLUTION: Test time of SoC = Maximum of the test times of all test buses. Since the cores sharing a test bus are tested serially,  $C0 + C1 + C2 = 730$ ;  $C3 + C4 = 760$ ;  $C6 + C7 = 660$ . Thus, the test time is Maximum (730, 760, 660), which is 760.

- 7. Two objectives of wrapper design algorithm are to minimize
  - a. Length of longest wrapper chain and average scan cells per chain
  - b. Length of longest wrapper chain and number of chains
  - c. Number of chains and average scan cells per chain
  - d. Length of smallest wrapper chain and number of chains

ANSWER: (b) Length of longest wrapper chain and number of chains

- 8. Modes of 1500 wrapper are
  - a. Normal, Serial, 1-N, Bypass, Isolation, Exttest
  - b. Normal, Serial, 1-N, Bypass, Isolation, Exttest, Intest
  - c. Normal, Serial, Bypass, Exttest
  - d. Normal, Serial, Bypass, Intest, Exttest

ANSWER: (a) Normal, Serial, 1-N, Bypass, Isolation, Exttest

9. Steps in an execution of INTEST instruction are
- Shift-DR – Update-DR – Shift-DR – Capture-DR
  - Shift-DR – Capture-DR – Update-DR – Shift-DR
  - Shift-DR – Update-DR – Capture-DR – Shift-DR
  - Shift-DR – Capture-DR – Shift-DR – Update-DR

ANSWER: (c) Shift-DR – Update-DR – Capture-DR – Shift-DR

10. In a virtual TAM environment, ATE has 6 pins out of which 3 can operate at a frequency 4 times that of the SoC. Calculate the number of TAM lines that can be supported for the SoC using the concept of virtual TAM.
- 6
  - 9
  - 12
  - 15

ANSWER: (d) 15

11. In a Rectangular Bin packing approach, which of the following option is true?

**Statement 1.** The width of the bin is fixed, the height of the bin has to be minimized

**Statement 2.** The height of the bin is fixed, the width of the bin has to be minimized

**Statement 3.** The height and width of the rectangles represent allocated test width to a core and corresponding test time of the core respectively.

**Statement 4.** The width and height of the rectangles represent allocated test width to a core and corresponding test time of the core respectively.

- Statement 1 and 3 are true
- Statement 2 and 3 are true
- Statement 1 and 4 are true
- Statement 2 and 4 are true

ANSWER: (b) Statement 2 and 3 are true

12. What is the advantage of selecting Pareto optimal points while allocating test pins to a core?
- It gives the best test time for a given number of test pins
  - This is the least number of test pins must be provided to a core to obtain a certain test time.
  - The points in the scheduler, where a new core can start its testing.
  - The points in the scheduler, where a currently tested core finishes its testing.

ANSWER: (b) This is the least number of test pins must be provided to a core to obtain a certain test time.

13. The advantage of Network-on-Chip over System-on-Chip in the context of test mechanism is

- a. In NoC environment, more cores can be tested in parallel than SoC environment
- b. In NoC environment, using the network reuse phenomenon, test time can be reduced even under power constraints, with minimized pin count and area overhead.
- c. NoC uses high speed data channel to send the test data, hence, testing is faster.
- d. Both a and b

ANSWER: (c) Both a and b

14. Which of the following is not true in the context of Network on Chip?

- a. Cores are connected to NoC by routers or switches.
- b. Data are organized by packets.
- c. Test data are sent to the cores using virtual TAM mechanism.
- d. Various network topologies and routing algorithms are used.

ANSWER: (c) Test data are sent to the cores using virtual TAM mechanism.

15. What are the advantages of multi speed TAM architecture in SoC Testing?

- a. Facilitate efficient use of high data-rate tester channels
- b. Avoid on-chip hardware overhead
- c. A better test scheduling strategy which helps to reduce test times of bottleneck cores.
- d. All of these

ANSWER: (d) All of these

# Digital VLSI Testing

## Week 11 Assignment Solution

1. Which of the following design features facilitates the use of Network-on-Chip in SoCs?
  - a. Reusability of physical channels
  - b. Degradation in signal integrity
  - c. Increase in power consumption
  - d. None of the given options

ANSWER: (a) Reusability of physical channels

2. Which of the following drawbacks facilitates the use of Network-on-Chip based testing in SoCs?
  - a. Non-reusability of mission-mode communication
  - b. Dedicated test access mechanism hardware
  - c. Both (a) and (b)
  - d. None of the given options

ANSWER: (c) Both (a) and (b)

3. Which of the following statements is TRUE for a Network-on-Chip based testing system?
  - a. Channels and routers are not used as test access mechanism elements
  - b. Input and output ports of testing circuit are associated with cores
  - c. Both (a) and (b)
  - d. None of the given options

ANSWER: (b) Input and output ports of testing circuit are associated with cores

4. One of the drawbacks of non-pre-emptive test scheduling in Network-on-Chip using dedicated routing path is
  - a. High power consumption
  - b. Pipelined test sessions
  - c. Complex test logic
  - d. None of the given options

ANSWER: (b) Pipelined test sessions

5. Which of the following orders satisfies for a successful Network-on-Chip based SoC test sequence?
  - a. Cores, Routers, Interconnects
  - b. Routers, Cores, Interconnects
  - c. Interconnects, Routers, Cores
  - d. Any of the given options

ANSWER: (c) Interconnects, Routers, Cores

6. Which of the following statements regarding a router are TRUE?
- Routers are used to implement functions of switching
  - Router testing can be treated as sequential circuit testing
  - Test pattern broadcast can be applied in router testing
  - All of the given options

ANSWER: (d) All of the given options

7. Which one is not true for ILP based solution for test scheduling of NoC?
- ILP based solution gives exact results
  - It can work for only smaller problem (i.e. a smaller NoC with less number of Cores and I/Os)
  - It takes minimal amount of CPU time to obtain the results
  - It deals with only integer values.

ANSWER: (c) It takes minimal amount of CPU time to obtain the results

8. The difference between ILP based and Heuristic based solution of NoC test scheduling is
- ILP gives optimal results while Heuristic gives near optimal result
  - CPU time for Heuristic solution is huge, while ILP based solution can obtain results within few minutes for any size of the circuit
  - For a larger circuit, ILP is the most suitable test scheduling strategy
  - Both ILP and heuristic can only deal with integer values.

ANSWER: (a) ILP gives optimal results while Heuristic gives near optimal result

9. The test wrapper of an NoC
- Wraps only the cores
  - Wrap both core and router
  - Reuse the packing and unpacking mechanism from mission mode
  - Both b and c

ANSWER: (d) Both b and c

10. For an Integrated test scheduling which of the following is not true?
- Routers must be tested separately from the cores
  - Routers on a path should be all tested before functional cores on that path to be tested
  - At least one I/O pair should be used for router testing at any time
  - Resource conflict must be checked

ANSWER: (a) Routers must be tested separately from the cores

11. The advantage of using variable on-chip test clocks in power-aware test scheduling of NoC is

- a. High power consumption cores can be tested at slower frequency and low power cores can be tested at faster frequency
- b. High power consumption cores can be tested at faster frequency and low power cores can be tested at slower frequency
- c. Multi-frequency testing makes proper utilization of test resources, hence reduces test time
- d. Both a and c

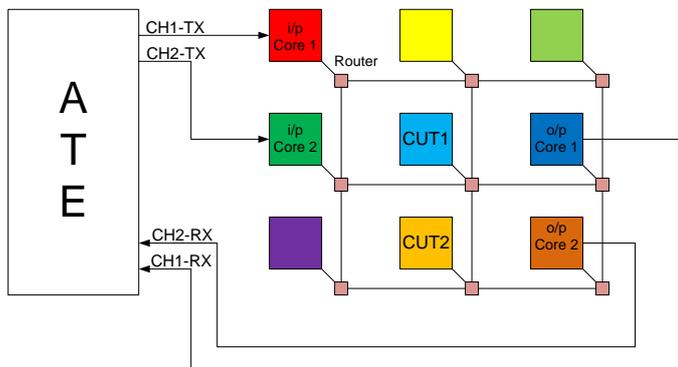
ANSWER: (d) Both a and c

12. Which of the following is not true for router testing?

- a. Control logic is tested using scan testing phenomenon
- b. All routers can be tested in parallel by test pattern broadcasting
- c. Router testing considers the testing of routing, FIFO, arbitration, and flow control modules only
- d. The comparator implemented using XOR gate does not have the diagnostic capability

ANSWER: (d) The comparator implemented using XOR gate does not have the diagnostic capability

13. For the diagram given below, choose the correct option.



- a. It is possible to conduct parallel testing using XY routing algorithm
- b. It is possible to conduct parallel testing using YX routing algorithm
- c. Both A and B are true
- d. Both A and B are false

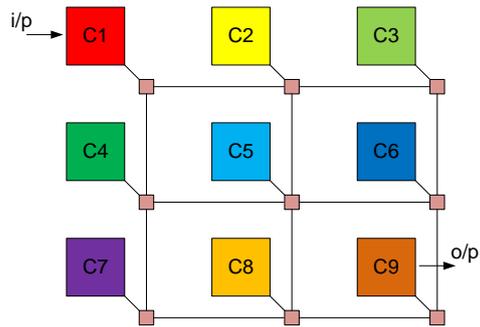
ANSWER: (d) Both A and B are false

14 . Which of the following statement is false in the context of the reuse of NoC as test access mechanism (TAM) for the embedded cores?

- a. Reduces the test time of the system.
- b. Increases the test time of the system.
- c. NoC reuse is limited by the on-chip routing resources
- d. Efficient test scheduling methods are required to provide feasible test time

ANSWER: (b) Increases the test time of the system.

15. If C1 is tested at time unit 1 then C9 will be tested in which of the following time units provided the routers present in the NoC supports multi-cast.



- a. 3
- b. 4
- c. 5
- d. 1

ANSWER: (c) 5

# Digital VLSI Testing

## Week 12 Assignment Solution

1. RAM coupling faults are
  - a. State coupling, Injection coupling, Zero coupling
  - b. Stuck coupling, Inversion coupling, Idempotent coupling
  - c. State coupling, Injection coupling, Idempotent coupling
  - d. State coupling, Inversion coupling, Idempotent coupling

ANSWER: d. State coupling, Inversion coupling, Idempotent coupling

2. Zero-One Algorithm for memory test can detect
  - a. All stuck at faults
  - b. All address decoder faults
  - c. All stuck at and address decoder faults
  - d. All stuck at faults if address decoder is correct

ANSWER: d. All stuck at faults if address decoder is correct

3. TAGS procedure will NOT delete which of the templates
  - a. (...rr...)
  - b. (r)(r)
  - c. ...(w)
  - d. (...rw...)

ANSWER: d. (...rw...)

4. Multi-Port faults in a multi-port memory include
  - a. Stuck-Open Fault
  - b. Address Decoder Fault
  - c. Interport Word Line Short
  - d. Intraport Word Line Short

ANSWER: c. Interport Word Line Short

5. Which of the following test sequence is considered in testing RAM circuits?
  - a. Full probe test, Post burn-in test, Pre burn-in test, Final test
  - b. Full probe test, Pre burn-in test, Post burn-in test, Final test
  - c. Full probe test, Final test, Pre burn-in test, Post burn-in test
  - d. Post burn-in test, Full probe test, Pre burn-in test, Final test

ANSWER: b. Full probe test, Pre burn-in test, Post burn-in test, Final test

6. Refresh logic is associated with
  - a. Both DRAM and SRAM
  - b. DRAM but not SRAM
  - c. SRAM but not DRAM
  - d. Neither DRAM nor SRAM

ANSWER: b. DRAM but not SRAM

7. Determine the test time required to test a 1G memory when the test is run at 1GHz, given that its test complexity is:  $N$ ,  $10N$ ,  $N\log N$ .
- 1.05s, 10.5s, 31.8s
  - 2.10s, 21.0s, 63.6s
  - 0.53s, 5.25s, 15.9s
  - 1.05s, 1.05s, 1.05s

ANSWER: a. 1.05s, 10.5s, 31.8s

8. Which of the following fault model is not related to the faults occurring in Memory Cell Arrays (MCAs) –
- Stuck-at faults
  - Transition faults
  - Address Decoder faults
  - All of the above

ANSWER: c. Address Decoder faults

9. Which of the following abnormal behaviour is not addressed by Address Decoder faults –
- Given a certain address no cell will be accessed
  - A certain cell can be accessed by multiple addresses
  - A certain cell is never accessed by any address
  - A transition in one cell inverts the content of another

ANSWER: d. A transition in one cell inverts the content of another

10. Which of the following statement is not true in the context of MSCAN RAM test algorithm –
- It can be represented as  $\{\uparrow(w0); \uparrow(r0); \uparrow(w1); \uparrow(r1)\}$
  - SAFs are detected if the address decoder is fault free
  - All the  $\downarrow/1$  TFs can be detected
  - All the CFs cannot be detected

ANSWER: c. All the  $\downarrow/1$  TFs can be detected

11. Which of the following statement is not true in the context of Checker board RAM test algorithm –
- While creating the checker board pattern, the physical layouts of the memory cells must be considered.
  - It can detect DRFs and Shorts between cells
  - It can detect SAFs and half of the TFs
  - It can detect all the CFs

ANSWER: d. It can detect all the CFs

12. The complexity of the GALPAT and WALPAT test algorithms are –
- $O(4N^2)$  and  $O(2N^2)$
  - $O(2N^2)$  and  $O(4N^2)$
  - $O(4N^2)$  and  $O(4N^2)$
  - $O(2N^2)$  and  $O(2N^2)$

ANSWER: a.  $O(4N^2)$  and  $O(2N^2)$

13. Which of the following statement is not true in the context of the following March Tests – MATS++, March X and March C-

- a. SAFs can be detected with 100% fault coverage by all of them
- b. TFs can be detected with 100% fault coverage by all of them
- c. CFid can be detected with 100% fault coverage by all of them
- d. CFin can be detected with 100% fault coverage by both March X and March C-

ANSWER: c. CFid can be detected with 100% fault coverage by all of them

14. Complexity of the RAMSES algorithm is –

- a.  $O(N^2)$
- b.  $O(N^3)$
- c.  $O(N)$
- d.  $O(4N)$

ANSWER: a.  $O(N^2)$