

## Unit 12 - Introduction to Digital Testing

### Course outline

How to access the portal ?

Introduction and Overview of VLSI Design

Scheduling in High-Level Synthesis

Resource Sharing and Binding in HLS

Logic Synthesis

Physical Design

Introduction to Verification Techniques

Syntax and semantics of CTL, Equivalences between CTL formulas and Introduction to Model Checking

CTL Model checking Algorithms and Introduction to Binary Decision Diagrams

Binary Decision Diagram and Symbolic model checking

Introduction to Digital Testing

- ☐ Introduction to Digital VLSI Testing
- ☐ Functional and Structural Testing
- ☐ Fault Equivalence
- ☐ Quiz : Week 9 Assignment

Fault Simulation and Testability Measures

Combinational Circuit Test Pattern Generation

Sequential Circuit Testing and Scan Chains

Built In Self Test (BIST)

### Week 9 Assignment

The due date for submitting this assignment has passed.

**Due on 2016-09-26, 23:58 IST.**

#### Submitted assignment

1) Murphy's Law states that \_\_\_\_\_

1 point

- ☐ If anything can go wrong, it will
- ☐ If nothing goes wrong, it will
- ☐ If anything can go wrong, it will not
- ☐ If nothing goes wrong, it will not

**No, the answer is incorrect.**

**Score: 0**

**Accepted Answers:**

*If anything can go wrong, it will*

2) The "DFT" stands for \_\_\_\_\_

1 point

- ☐ Design for technique
- ☐ Design for testability
- ☐ Data flow-based testing
- ☐ None of the above

**No, the answer is incorrect.**

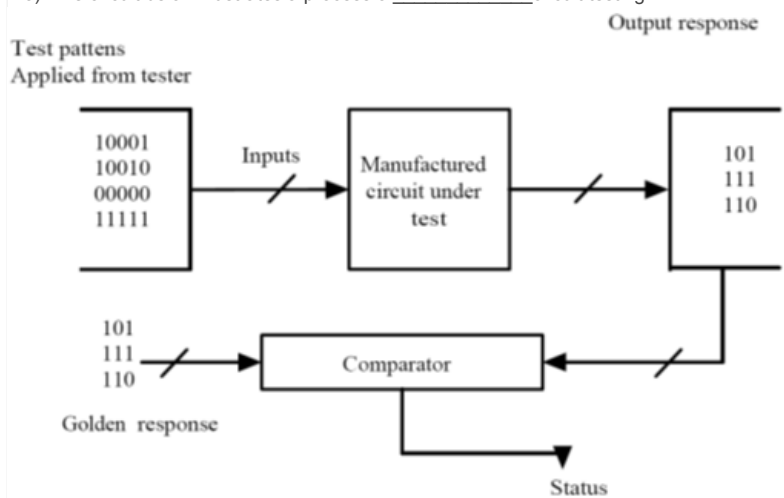
**Score: 0**

**Accepted Answers:**

*Design for testability*

3) The circuit below illustrates a process of \_\_\_\_\_ circuit testing

1 point



- ☐ Digital
- ☐ Analog
- ☐ Both Analog and Digital
- ☐ None of the above

**No, the answer is incorrect.**

**Score: 0**

**Accepted Answers:**

## Digital

4) What will be the value of the output O in the figure below if first ten inputs are set to 0 while rests are set to 1? **1 point**



- ☐ 0
- ☐ 1
- ☐ non-deterministic
- ☐ none of the above

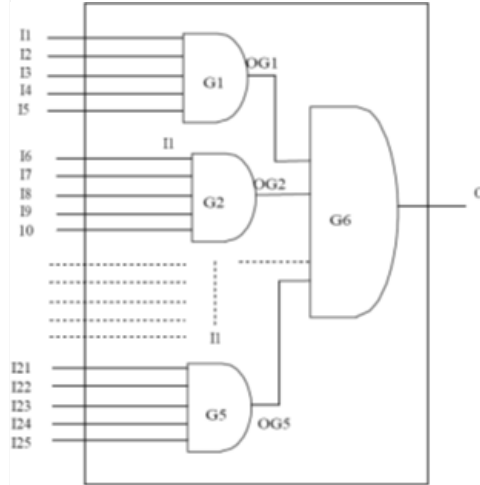
No, the answer is incorrect.

Score: 0

Accepted Answers:

0

5) How many test patterns are needed to test the system of Q4 if one implements it as shown below? **1 point**



- ☐ 25
- ☐ 60
- ☐ 192
- ☐ 160

No, the answer is incorrect.

Score: 0

Accepted Answers:

192

6) The unintended difference between the implemented hardware in silicon and its intended design in a circuit is called \_\_\_\_\_ **1 point**

- ☐ Fault
- ☐ Error
- ☐ Defect
- ☐ Noise

No, the answer is incorrect.

Score: 0

Accepted Answers:

Defect

7) An "effect" of some \_\_\_\_\_ is called \_\_\_\_\_ **1 point**

- ☐ Defect, Error
- ☐ Fault, Defect
- ☐ Error, Fault
- ☐ Fault, Error

No, the answer is incorrect.

Score: 0

**Accepted Answers:***Defect, Error*

8) Abstraction of a \_\_\_\_\_ at the fault modeling level is called \_\_\_\_\_

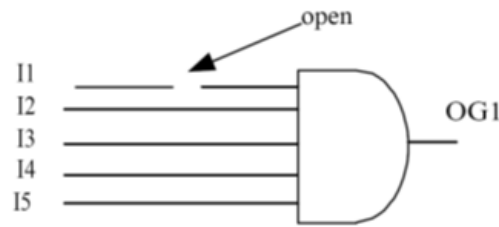
1 point

- ☐ Fault, Error
- ☐ Defect, Fault
- ☐ Error, Defect
- ☐ Fault, Defect

**No, the answer is incorrect.****Score: 0****Accepted Answers:***Defect, Fault*

9) The input wire I1 in the figure below is left unconnected with the gate due to incomplete doping of metal. This

1 point



unconnected net I1 is a \_\_\_\_\_

- ☐ Defect
- ☐ Error
- ☐ Fault
- ☐ None of the above

**No, the answer is incorrect.****Score: 0****Accepted Answers:***Defect*

10) A short between a group of nets is called a \_\_\_\_\_ fault.

1 point

- ☐ Bridging
- ☐ Stuck-at-1
- ☐ Stuck-at-0
- ☐ Delay

**No, the answer is incorrect.****Score: 0****Accepted Answers:***Bridging*

11) A circuit with n nets can have \_\_\_\_\_ possible stuck-at faults under single stuck-at fault model.

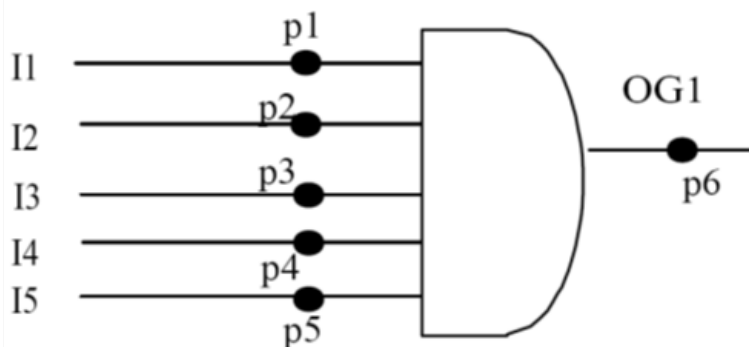
1 point

- ☐  $2^n$
- ☐  $n^2$
- ☐ infinite
- ☐  $2 \times n$

**No, the answer is incorrect.****Score: 0****Accepted Answers:** *$2 \times n$* 

12) How many stuck-at faults are possible in the AND-gate shown in the figure below ?

1 point



- ☐ 6

- ☐ 12
- ☐ 11
- ☐ 10

No, the answer is incorrect.

Score: 0

Accepted Answers:

12

13) The equivalent faults have \_\_\_\_\_ the same set of test patterns.

1 point

- ☐ Exactly
- ☐ Not Exactly
- ☐ Sometimes
- ☐ None of the above

No, the answer is incorrect.

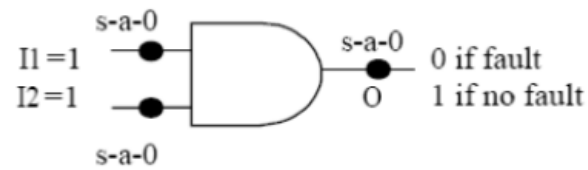
Score: 0

Accepted Answers:

Exactly

14) What is the minimum number of test patterns to test all the stuck-at-0 faults in the AND-gate shown in the figure below

1 point



- ☐ 1
- ☐ 2
- ☐ 3
- ☐ 4

No, the answer is incorrect.

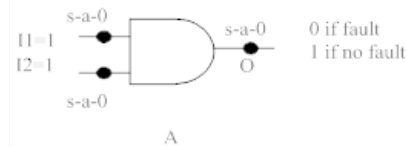
Score: 0

Accepted Answers:

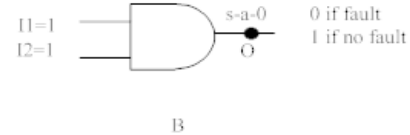
1

15) Which options shown in the figure below, represents correct fault collapsing on an AND gate by fault equivalence.

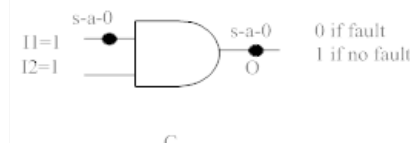
2 points



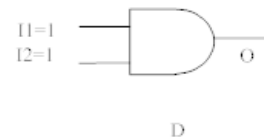
A



B



C



D

- ☐ A
- ☐ B
- ☐ C
- ☐ D

No, the answer is incorrect.

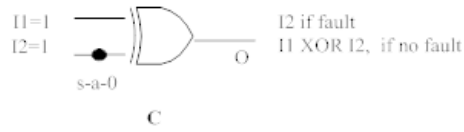
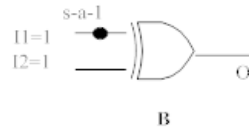
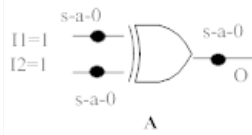
Score: 0

Accepted Answers:

B

16) Which option shown in the figure below represents correct fault collapsing on an XOR gate by fault equivalence.

1 point



cannot be collapsed using equivalence

D

- ☐ A  
☐ B  
☐ C  
☐ D

No, the answer is incorrect.

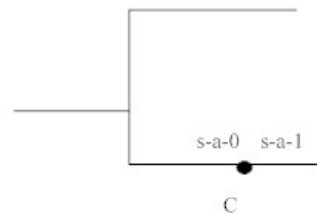
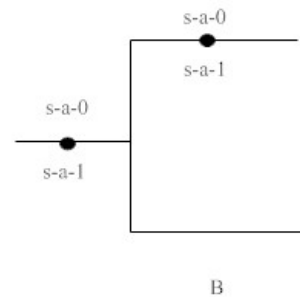
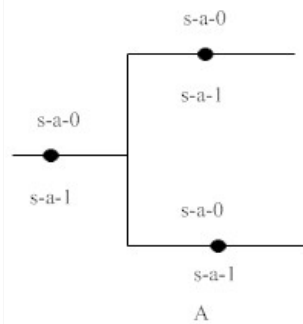
Score: 0

Accepted Answers:

D

17) Which option shown in the figure below, represents correct fault collapsing on Fanout by equivalence.

1 point



Faults cannot be collapsed

D

- ☐ A  
☐ B  
☐ C  
☐ D

No, the answer is incorrect.

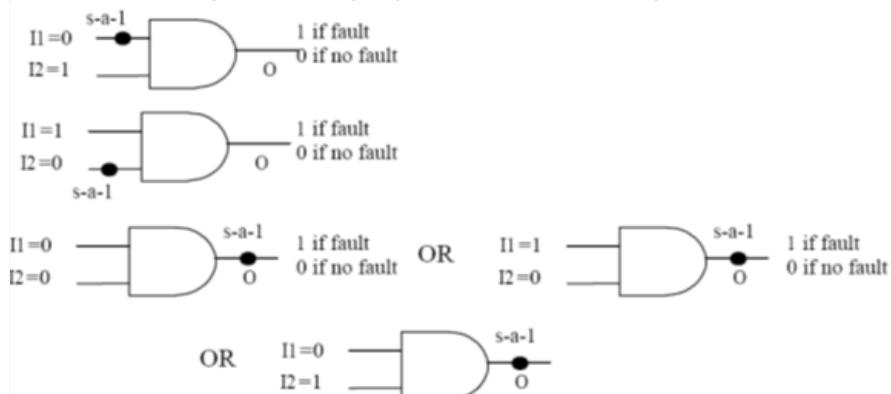
Score: 0

Accepted Answers:

D

18) The fault collapsing shown in the figure given below is carried out using \_\_\_\_\_

1 point



- ☐ Fault Equivalence  
☐ Fault Dominance

- ☐ Both (a) and (b)  
☐ None of the above

No, the answer is incorrect.

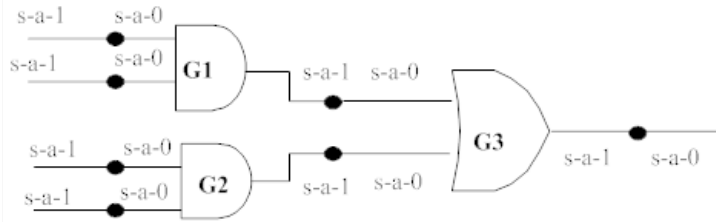
Score: 0

Accepted Answers:

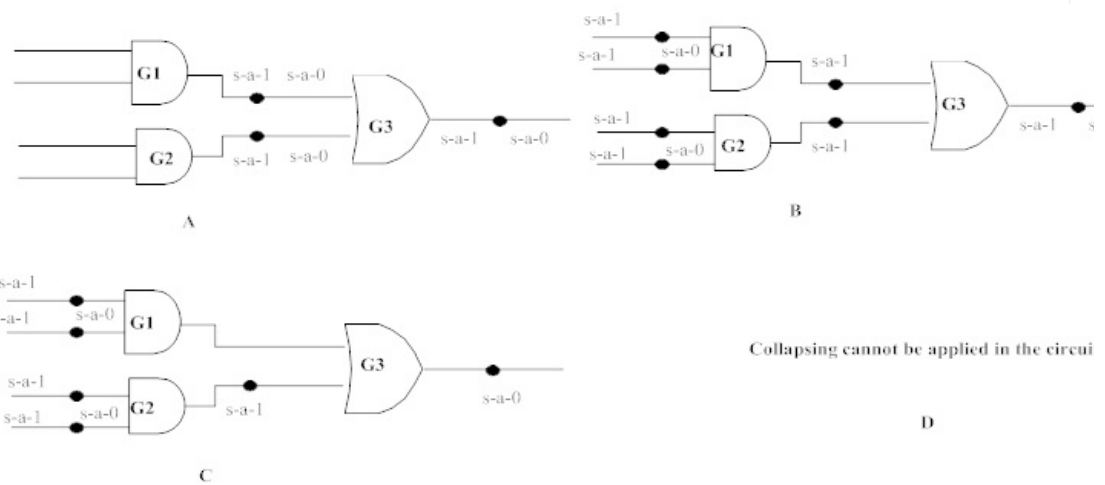
Fault Dominance

19) Consider the circuit shown below.

3 points



After fault collapsing is applied using "Equivalence", which of the following option illustrates the correct list of remaining faults.



- ☐ A  
☐ B  
☐ C  
☐ D

No, the answer is incorrect.

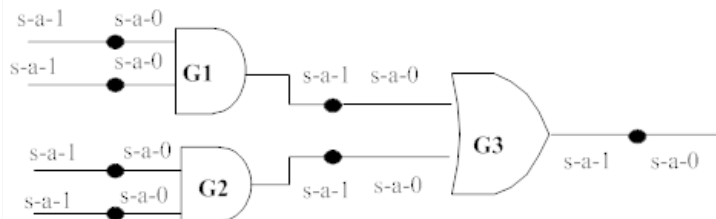
Score: 0

Accepted Answers:

C

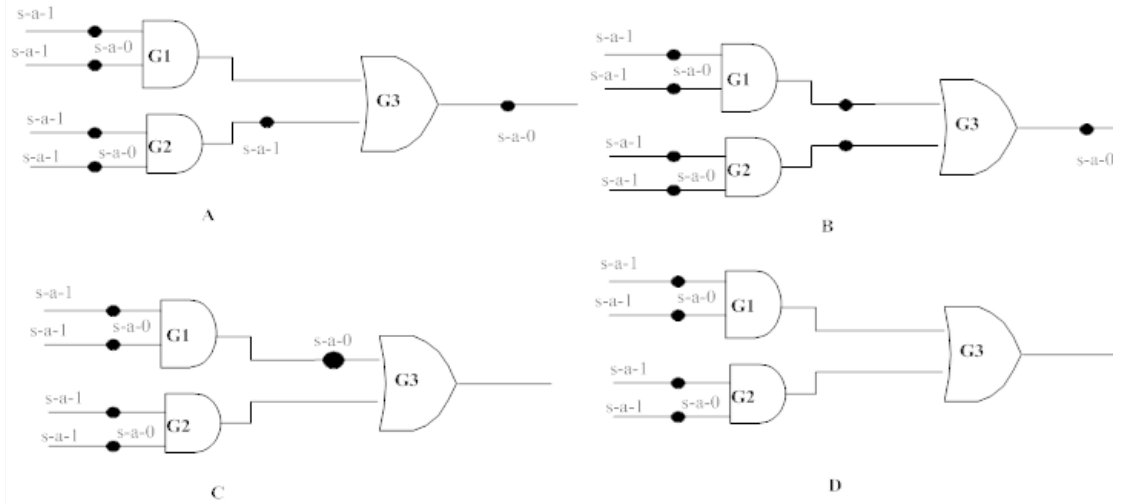
20) Consider the circuit shown below.

3 points



After fault collapsing is applied using "equivalence" and "dominance", which of the following option illustrates the correct list of

remaining faults.



- ☐ A
- ☐ B
- ☐ C
- ☐ D

No, the answer is incorrect.

Score: 0

Accepted Answers:

D

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