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NPTEL

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Courses » VLSI Design Verification and test

Announcements

Course

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# Unit 8 - Introduction to Verification Techniques

## Course outline

How to access the portal ?

Introduction and Overview of VLSI Design

Scheduling in High-Level Synthesis

Resource Sharing and Binding in HLS

Logic Synthesis

Physical Design

Introduction to Verification Techniques

☐ Introduction to formal methods for design verification

☐ Temporal Logic: Introduction and Basic Operations on Temporal Logic

☒ Syntax and Semantics of CTL

☐ Quiz : Week 5-- Assignment

Syntax and semantics of CTL, Equivalences between CTL formulas and Introduction to Model Checking

CTL Model checking Algorithms and Introduction to Binary Decision Diagrams

Binary Decision Diagram and Symbolic model checking

Introduction to Digital Testing

## Week 5--Assignment

The due date for submitting this assignment has passed.

**Due on 2016-08-28, 23:58 IST.**

### Submitted assignment

1) Which one of the followings is true?

1 point

- ☐ Propositional logic = Predicate logic
- ☐ Propositional logic is subset of predicate logic
- ☐ Predicate logic is subset of propositional logic
- ☐ None of the above

No, the answer is incorrect.

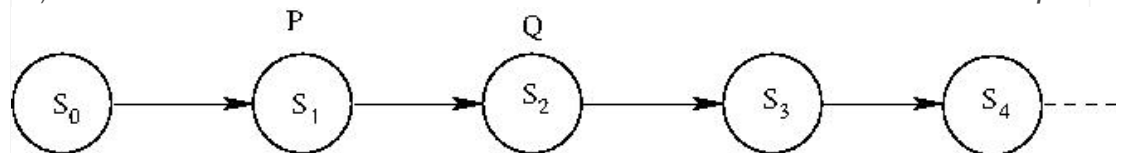
Score: 0

Accepted Answers:

Propositional logic is subset of predicate logic

2)

1 point



Consider the system shown in the figure. In which state the temporal logic  $(P \rightarrow XQ)$  is not satisfied?

- ☐  $S_0$
- ☐  $S_1$
- ☐  $S_2$
- ☐ None

No, the answer is incorrect.

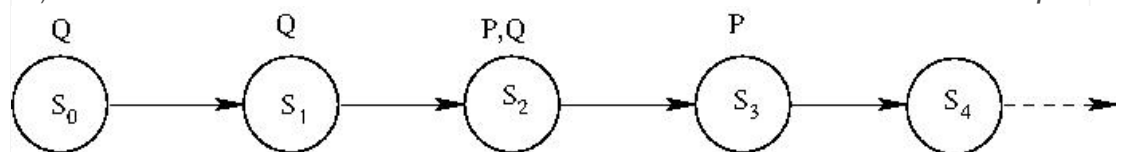
Score: 0

Accepted Answers:

None

3)

1 point



Consider the system shown in the figure and the temporal logic  $(P \wedge \blacksquare Q)$ . Which one of the followings is true? The symbol  $\blacksquare$  stands for globally past.

- ☐  $(P \wedge \blacksquare Q)$  is satisfied in state  $S_3$
- ☐  $(P \wedge \blacksquare Q)$  is satisfied in state  $S_1$
- ☐  $(P \wedge \blacksquare Q)$  is satisfied in state  $S_2$

Fault Simulation  
and Testability  
Measures

Combinational  
Circuit Test Pattern  
Generation

Sequential Circuit  
Testing and Scan  
Chains

Built In Self Test  
(BIST)

☐ None

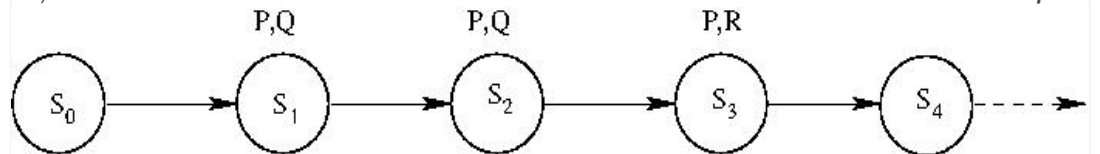
No, the answer is incorrect.

Score: 0

Accepted Answers:

$(P \wedge \neg Q)$  is satisfied in state  $S_2$

4)



Consider the system shown in the figure and the temporal logic  $(P \rightarrow (QUR))$ . Which one of the followings is true?

- ☐  $(P \rightarrow (QUR))$  is not satisfied in state  $S_0$
- ☐  $(P \rightarrow (QUR))$  is not satisfied in state  $S_4$
- ☐  $(P \rightarrow (QUR))$  is not satisfied in states  $S_1$ ,  $S_2$  and  $S_3$
- ☐  $(P \rightarrow (QUR))$  is satisfied in all states

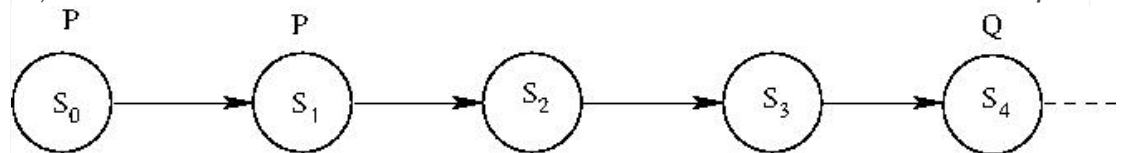
No, the answer is incorrect.

Score: 0

Accepted Answers:

$(P \rightarrow (QUR))$  is satisfied in all states

5)



Consider the system shown in the figure and the temporal logic  $(PV(FQ))$ . Which one of the followings is true?

- ☐  $(PV(FQ))$  is satisfied only in state  $S_0$
- ☐  $(PV(FQ))$  is satisfied only in state  $S_1$
- ☐  $(PV(FQ))$  is not satisfied only in state  $S_4$
- ☐  $(PV(FQ))$  is satisfied in all states

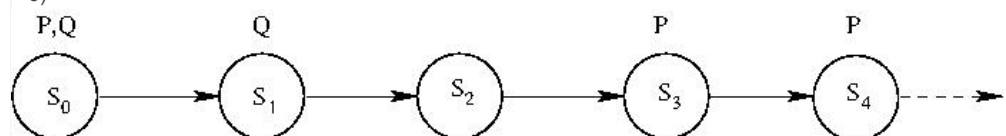
No, the answer is incorrect.

Score: 0

Accepted Answers:

$(PV(FQ))$  is satisfied in all states

6)



Consider the model shown in the figure. Choose the correct one. The symbol  $\bullet$  stands for previous past operator.

- ☐  $(PV \bullet Q)$  is not satisfied in state  $S_2$
- ☐  $(PV \bullet Q)$  is not satisfied in state  $S_1$
- ☐  $(PV \bullet Q)$  is satisfied in all states
- ☐  $(PV \bullet Q)$  is only satisfied in state  $S_0$

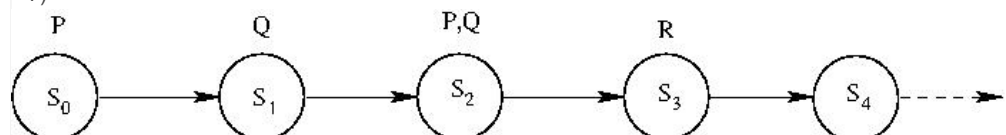
No, the answer is incorrect.

Score: 0

Accepted Answers:

$(PV \bullet Q)$  is satisfied in all states

7)



Consider the model shown in the figure. Choose the incorrect one.

- ☐  $((P \rightarrow Q) \text{ UR})$  is satisfied in the state  $S_2$
- ☐  $((P \rightarrow Q) \text{ UR})$  is satisfied in the state  $S_1$
- ☐  $((P \rightarrow Q) \text{ UR})$  is satisfied in the state  $S_0$
- ☐ None

No, the answer is incorrect.

Score: 0

Accepted Answers:

$((P \rightarrow Q) \text{ UR})$  is satisfied in the state  $S_0$

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