

NPTEL

reviewer1@nptel.iitm.ac.in ▼

Courses » VLSI Design Verification and test

Announcements Course Ask a Question Progress Mentor

Unit 7 - Physical Design

Course outline	WEEK 4 ASSIGNMENT	
low to access	The due date for submitting this assignment has passed. Due on 2016-08-22, 23:58 IS	T.
he portal ?	Submitted assignment	
Introduction and	1) Which of the following statement(s) is (are) true about moore style FSM?	oint
Overview of VLSI Design	the output is a function of the present state.	
	the output is a function of the present state and inputs.	
cheduling in igh-Level	the output is a function of the next state.	
ynthesis	the output is a function of the next state and inputs.	
Resource	No, the answer is incorrect. Score: 0	
Sharing and Binding in HLS	Accepted Answers:	
	the output is a function of the present state.	
ogic Synthesis	2) Which of the following statement(s) is(are) incorrect about Boolean expressions? 1 po	oint
Physical Design	All Boolean expressions can be implemented as a two-level logic function.	
Physical Design	All Boolean expressions can be implemented as a three-level logic function.	
(Part-1)	All Boolean expressions can be implemented as a four-level logic function.	
O Physical Design (Part-2)	None of the above	
,	No, the answer is incorrect.	
Physical Design (Part-3)	Score: 0	
Quiz : WEEK 4	Accepted Answers: None of the above	
ASSIGNMENT		
ntroduction to	3) The ON-set of a Boolean function is composed of the following min-terms: 1, 2, 5, 6, 7, 9, 2 poi 10. The don't cares are: 0, 3, 11, 13. The cardinality of the exhaustive set of prime implicants is:	ints
erification echniques	O 5	
	© 6	
Syntax and	0 4	
semantics of CTL,	O 7	
Equivalences between CTL	No, the answer is incorrect.	
ormulas and	Score: 0	
ntroduction to Model Checking	Accepted Answers:	
	6	
CTL Model checking	4) The minimum number of essential prime implicants for the Boolean function in Q3 are: 2 points	ints
Algorithms and	O 4	
ntroduction to Binary Decision	O 3	

Binary Decision Diagram and Symbolic model checking

Introduction to Digital Testing

Fault Simulation and Testability Measures

Combinational Circuit Test Pattern Generation

Sequential Circuit Testing and Scan Chains

Built In Self Test (BIST)

2

No, the answer is incorrect.

Score: 0

5

Accepted Answers:

3

5) For the ESPRESSO algorithm, which of the following statement(s) is(are) true:

1 point

- The expand step produces a cover over prime implicants.
- The irredundant step produces a cover over essential prime implicants.
- The reduce step retains a cover over all prime implicants.
- None of the above.

No, the answer is incorrect.

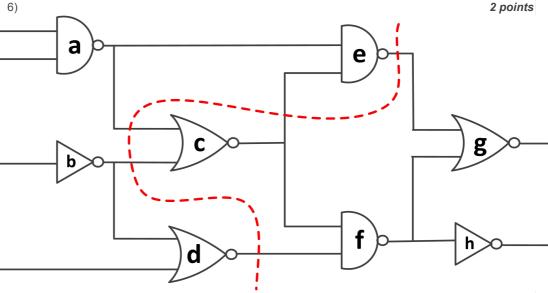
Score: 0

Accepted Answers:

The expand step produces a cover over prime implicants.

The irredundant step produces a cover over essential prime implicants.

The reduce step retains a cover over all prime implicants.



For the given circuit diagram with the initial partition as shown through the cut line, obtain a netlist. With this netlist as an input, a correct enumeration of the vertices on each side of the partition after the second iteration of the inner repeat loop in the Kernighan-Lin (KL) algorithm is:

- Partition-1: a, e, f, g. Partition-2: b, c, d, h
- Partition-1: a, c, e, g. Partition-2: b, d, f, h
- Partition-1: a, c, g, h. Partition-2: b, d, e, f
- Partition-1: c, d, f, g. Partition-2: a, b, e, h

No, the answer is incorrect.

Score: 0

Accepted Answers:

Partition-1: a, c, e, g. Partition-2: b, d, f, h

7) For Q6, the absolute gain (g) at the end of the third iteration is:

2 points

- _ -2
- 2
- _ -1
- 0 1

No, the answer is incorrect.

Score: 0

Accepted Answers:

-2

8) For Q6, the final partition and cut-size is:

Partition-1: a, b, c, h. Partition-2: d, f, g, e and cut-size: 2

Partition-1: a, f, c, e. Partition-2: d, b, g, h and cut-size: 1

Partition-1: a, b, c, e. Partition-2: d, f, g, h and cut-size: 3

Partition-1: a, b, g, h. Partition-2: d, f, c, e and cut-size: 4

No, the answer is incorrect.

Score: 0

Accepted Answers:

Partition-1: a, b, c, e. Partition-2: d, f, g, h and cut-size: 3

Previous Page

End

© 2014 NPTEL - Privacy & Terms - Honor Code - FAQs -



A project of



In association with



Funded by

Government of India Ministry of Human Resource Development

Powered by

