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Courses » VLSI Design Verification and test

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Unit 4 - Resource Sharing and Binding in HLS

Course **WEEK 3 ASSIGNMENT** outline The due date for submitting this assignment has passed. Due on 2016-08-15, 23:58 IST. How to access Submitted assignment the portal? Introduction and Overview of VLSI 1) Two operations are compatible when: 1 point Design They are non-concurrent or are of the same type. Scheduling in They are concurrent and are of the same type. **High-Level Synthesis** They are non-concurrent and are of the same type. They are concurrent or are of different types. Resource No, the answer is incorrect. Sharing and **Binding in HLS** Score: 0 **Accepted Answers:** Resource They are non-concurrent and are of the same type. Sharing and Binding in HLS 2) Which of the following statements are true: 2 points (Part-1) Resource Comparability graph satisfies transitive orientation property. Sharing and Vertices in an interval graph are adjacent if corresponding intervals overlap. Binding in HLS A conflict graph is an interval graph if its complement is chordal graph. (Part-2) Chromatic number of a chordal graph can be obtained in polynomial time. Resource All of the above. Sharing and Binding in HLS No, the answer is incorrect. (Part-3) Score: 0 Resource **Accepted Answers:** Sharing and Binding in HLS Comparability graph satisfies transitive orientation property. (Part-4) Vertices in an interval graph are adjacent if corresponding intervals overlap. Chromatic number of a chordal graph can be obtained in polynomial time. Resource Sharing and 3) A basic block consists of the following expression: K = ((x + y) + (y + z)) * ((y + z) + (y * z) + 2 pointsBinding in HLS (z * w)). The latency bound is 4. The minimum number of resource instances required to this basic block (Part-5) when '*' and '+' are conflicting. Resource Sharing and 0 2 Binding in HLS 3 (Part-6) 0 4 Resource **5** Sharing and Binding in HLS No, the answer is incorrect. (Part-7) Score: 0 Quiz: WEEK 3 **Accepted Answers: ASSIGNMENT**

7/2018	VLSI Design Verification and test Unit 4 - Resource Sharing and Binding in HLS	
Logic Synthesis	4	
Physical Design	4) Two registers in the same register bank can have:	2 point
Physical Design	overlapping life times, but non-overlapping access times.	
Introduction to	overlapping life times and overlapping access times.	
Verification Techniques	non-overlapping life times, but overlapping access times.	
	non-overlapping life times and non-overlapping access times.	
Syntax and	No, the answer is incorrect.	
semantics of CTL.	Score: 0	
Equivalences	Accepted Answers:	
between CTL formulas and	overlapping life times, but non-overlapping access times.	
Introduction to	non-overlapping life times and non-overlapping access times.	
Model Checking	5) Which of the following statements are true:	1 poin
CTL Model	Register banks contain MUXs at write ports and DEMUXs at read ports.	
checking	Two registers in the different banks can be accessed at the same time.	
Algorithms and Introduction to	MUXs / DEMUXs arbitrate write / read accesses to registers, respectively.	
Binary Decision Diagrams	All of the above.	
Diagrams	No, the answer is incorrect.	
Binary Decision	Score: 0	
Diagram and Symbolic model	Accepted Answers:	
checking	All of the above.	
Introduction to	6) A good solution is expected using simulated annealing if:	2 point
Digital Testing	the probability of accepting worse solutions is higher at higher temperatures.	
Fault Simulation	the probability of accepting better solutions is absolute at all temperatures.	
and Testability	the probability of accepting worse solutions is lower at higher temperatures.	
Measures	the probability of accepting worse solutions is higher at lower temperatures.	
Combinational	No, the answer is incorrect.	
Circuit Test	Score: 0	
Pattern Generation	Accepted Answers:	
	the probability of accepting worse solutions is higher at higher temperatures.	
Sequential Circuit Testing and Scan Chains	the probability of accepting better solutions is absolute at all temperatures.	
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