X

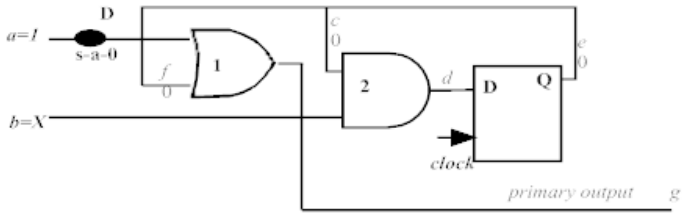
Unit 16 - Built In Self Test (BIST)

Week 12 Assignment

The due date for submitting this assignment has passed. **Due on 2016-10-14, 23:58 IST.**

Submitted assignment

1) Consider the circuit and the s-a-0 fault shown below. The input pattern(s) to test the fault is (are) _____. ***1 point***

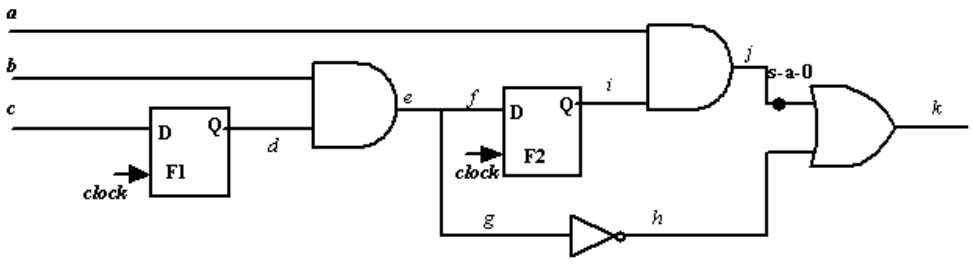


- a=X and b=0
- a=1 and b=X
- a=1 and b=X followed by a clock edge and then a=X, b=0
- a=X, b=0 followed by a clock edge and then a=1 and b=X

No, the answer is incorrect.
Score: 0

Accepted Answers:
a=X, b=0 followed by a clock edge and then a=1 and b=X

2) Consider the circuit shown below. Input of F1 is dependent on only primary inputs. On the other hand, input of F2 is dependent on primary inputs (net b) as well as the output of F1 (net d). So the circuit is _____. ***1 point***



- Cyclic
- Non-cyclic
- Some part (F1) is non-cyclic and other part (F2) is cyclic
- Some part (F2) is non-cyclic and other part (F1) is cyclic

No, the answer is incorrect.
Score: 0

Accepted Answers:
Non-cyclic

3) Consider the sequential circuit referred in Q2. If we test the s-a-0 fault on net j, the primary inputs “a”, “b”, “c” are ____ respectively. ***1 point***

- 1, 1, 1
- 1, 0, 1
- 1, 1, 0

1, 0, 0

No, the answer is incorrect.
Score: 0

Accepted Answers:
1, 1, 1

4) By setting primary inputs in the circuit referred in Q2, the secondary inputs “d” and “i” are obtained as ____ respectively. ***1 point***

- 1, 1
- 1, 0
- 0, 1
- 0, 0

No, the answer is incorrect.
Score: 0

Accepted Answers:
1, 1

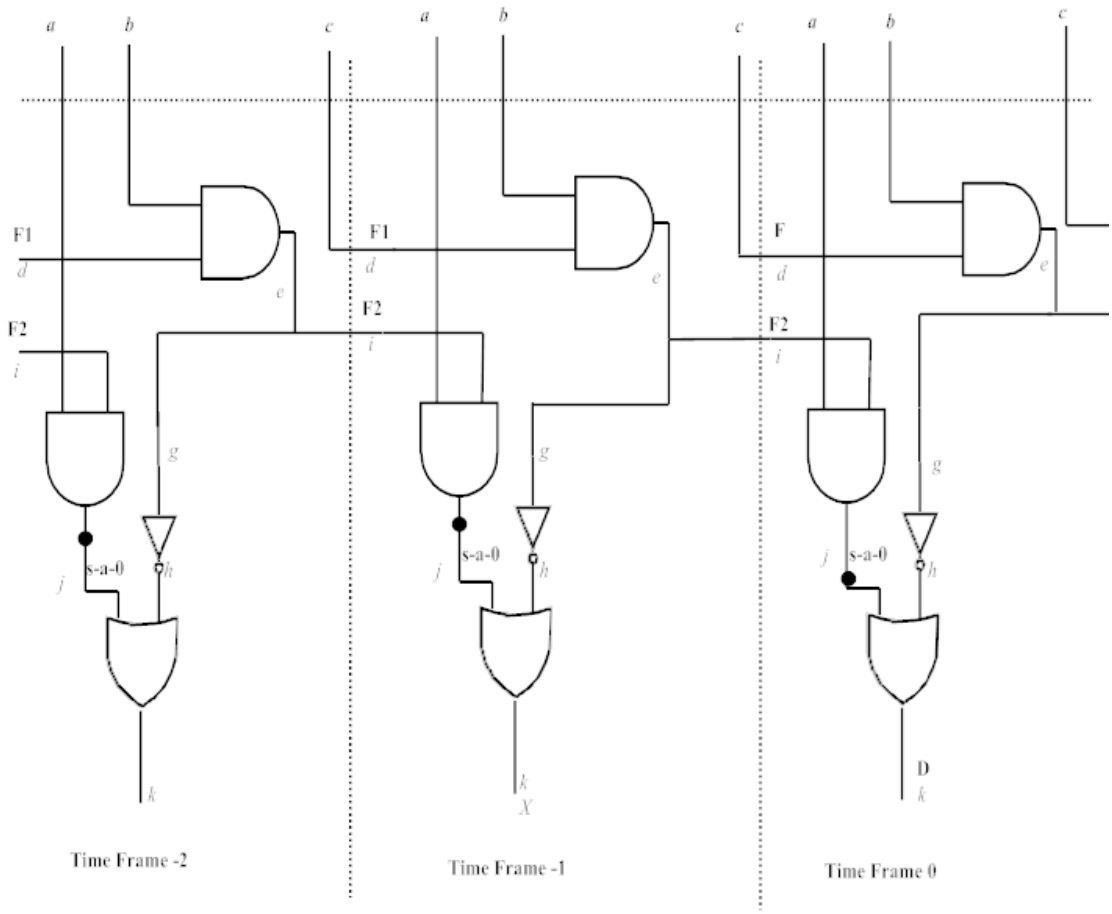
5) The secondary inputs of a cycle free sequential circuit of depth d_{seq} can be brought to controllable value is at most ____ primary input patterns and clock pulses. ***1 point***

- d_{seq}
- d_{seq} -1
- d_{seq} -2
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
d_{seq}

6) Consider the circuit shown below that demonstrates an ATPG for the s-a-0 fault in the circuit referred in Q2 using time frame expansion approach. What is the input pattern at time frame -2 ? It is assumed that a clock pulse is applied with the pattern. ***1 point***



- a=X, b=X, c=1
- a=X, b=1, c=0
- a=1, b=1, c=X
- None

No, the answer is incorrect.
Score: 0

Accepted Answers:
a=X, b=X, c=1

7) What is the input pattern at time frame -1 in circuit referred in Q6? It is assumed that a clock pulse is applied with the pattern. ***1 point***

- a=X, b=X, c=1
- a=X, b=1, c=1
- a=1, b=1, c=X
- None

No, the answer is incorrect.
Score: 0

Accepted Answers:
a=X, b=1, c=1

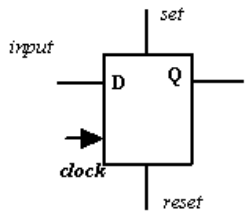
8) What is the input pattern at time frame 0 in circuit referred in Q6? It is assumed that a clock pulse is applied with the pattern. ***1 point***

- a=X, b=X, c=1
- a=X, b=1, c=1
- a=1, b=1, c=X
- None

No, the answer is incorrect.
Score: 0

Accepted Answers:
a=1, b=1, c=X

9) Consider a D- flip flop shown below and variable assignments as D=X, Q=1, clock=X. Then set-reset is assigned as ____. ***1 point***

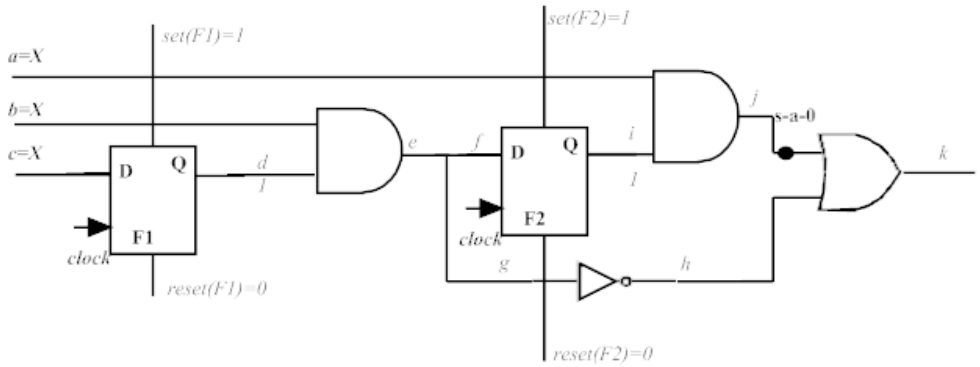


- 1-0
- 0-1
- 0-0
- 1-1

No, the answer is incorrect.
Score: 0

Accepted Answers:
1-0

10)Let us consider a circuit with set-reset assignments as shown below. In order to sensitize and propagate the effect of the fault to primary output, the test input “a”, “b”, “c” must be assigned as ____ respectively. ***1 point***

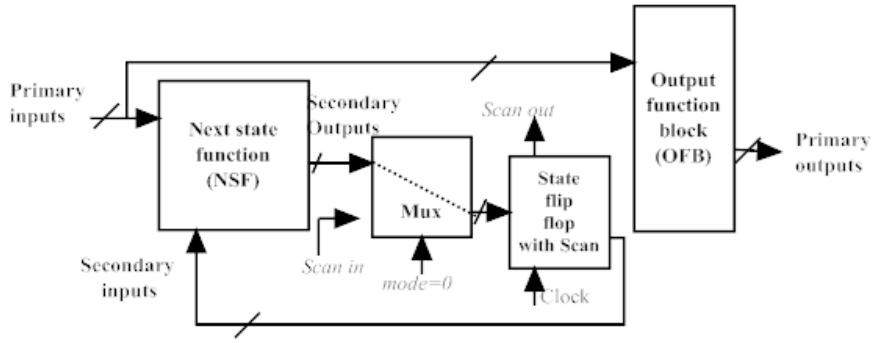


- 1, 1, X
- 0, 1, X
- 1, 1, D
- 1, 0, X

No, the answer is incorrect.
Score: 0

Accepted Answers:
1, 1, X

11)Consider a block diagram of a sequential circuit shown below. Which of the following is true? ***1 point***

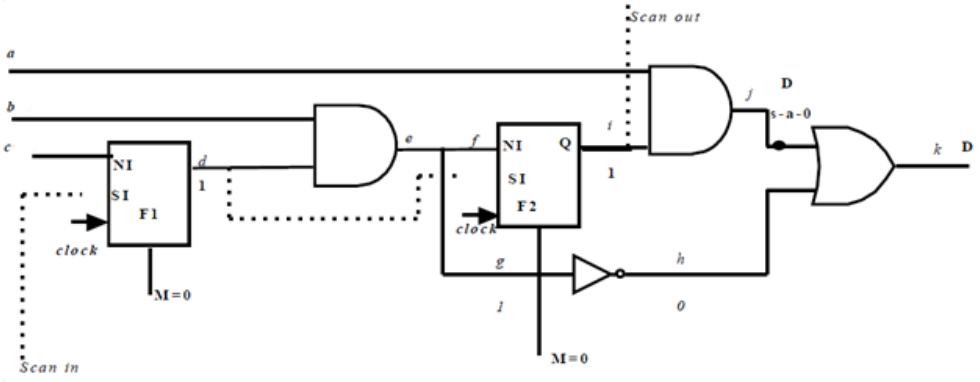


- The circuit has Scan chain and is in scan chain (test) mode
- The circuit has Scan chain and is in normal (functional) mode
- The circuit does not have scan chain
- The circuit has scan chain but is permanently disabled

No, the answer is incorrect.
Score: 0

Accepted Answers:
The circuit has Scan chain and is in normal (functional) mode

12)Consider a sequential circuit shown below, with s-a-0 fault at *j*. Assume that output of F1 and F2 are made 1 in scan mode. ***1 point***
Now scan mode is disabled by making M=0. Finally, we need to make the input pattern "a", "b", "c" as _____ respectively to test the fault.



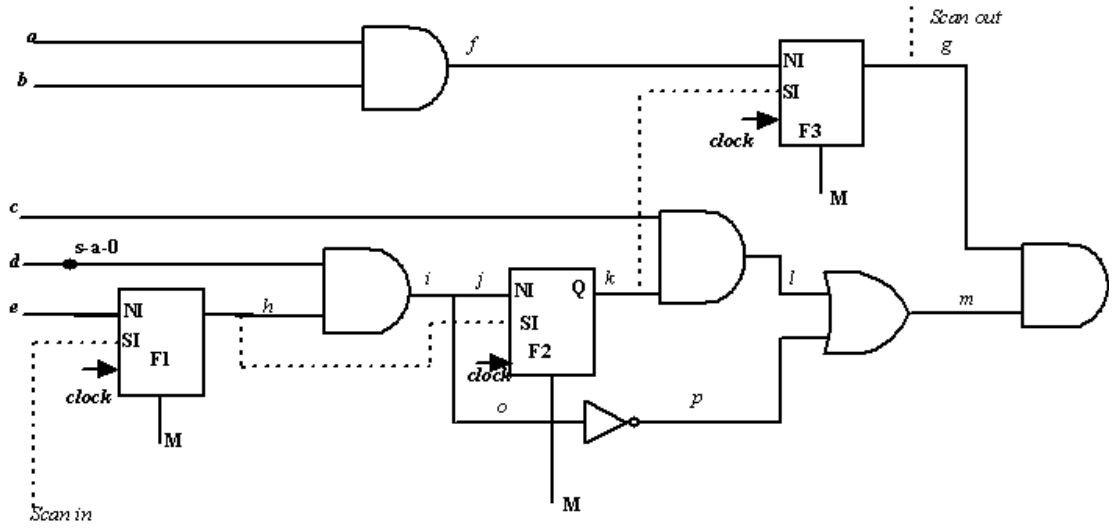
- 1, 1, X
- 1, 0, X
- 0, 1, X

0, 0, X

No, the answer is incorrect.
Score: 0

Accepted Answers:
1, 1, X

13)Consider a sequential circuit shown below that performs testing using scan chain. We need to test the s-a-0 fault at *d* and the fault propagation path is *d-i-o-p-m-n*. Which of the following can be used as a scan sequence? ***1 point***



0,0,0
1,0,1
1,0,0
1,1,0

No, the answer is incorrect.
Score: 0

Accepted Answers:
1,0,1

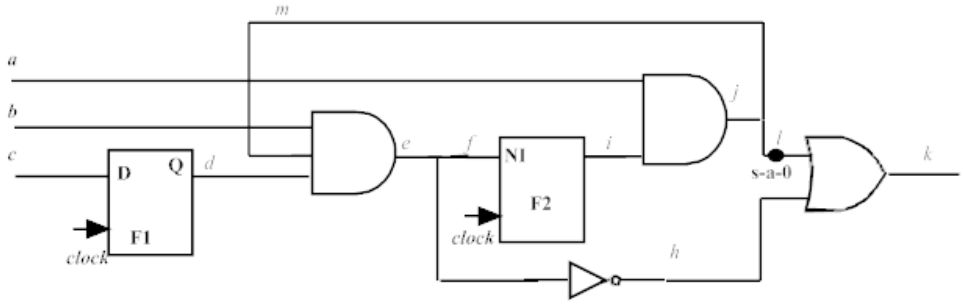
14)The “partial scan chain” method basically comprises a combination of____. ***1 point***

Scan chain scheme and Time frame expansion scheme
Scan chain scheme and internal memory.
Scan chain scheme and many extra pin outs
Scan chain scheme and Time frame expansion scheme and internal memory

No, the answer is incorrect.
Score: 0

Accepted Answers:
Scan chain scheme and Time frame expansion scheme

15)Consider the circuit shown below where we are aiming to test the s-a-0 fault. Which of the following is true? ***1 point***

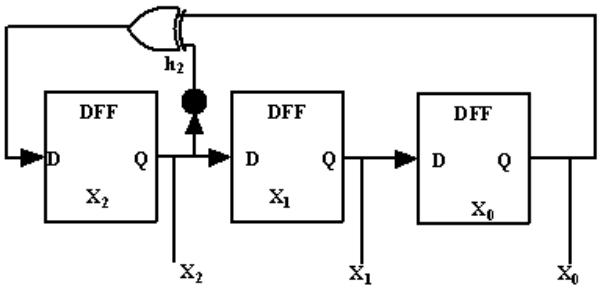


The fault cannot be tested because F1 is cyclic.
The fault cannot be tested because F2 is cyclic.
The fault cannot be tested because both F1 and F2 are cyclic
The fault can be tested.

No, the answer is incorrect.
Score: 0

Accepted Answers:
The fault cannot be tested because F2 is cyclic.

16)Consider a circuit representation below of a 3-input Linear feedback shift register (LFSR). The characteristic polynomial f(x) of the LFSR is ___. ***1 point***



- 1 + x
- $1 + x + x^2$
- $1 + x^2 + x^3$
- None

No, the answer is incorrect.
Score: 0

Accepted Answers:
$1 + x^2 + x^3$

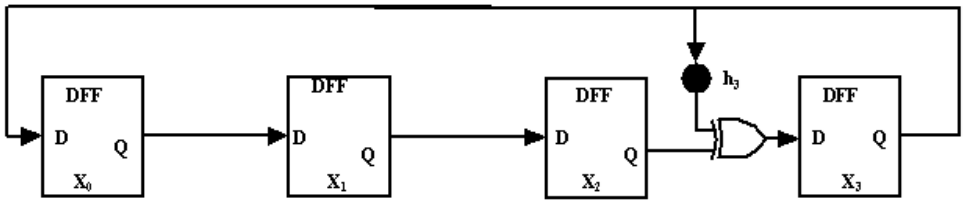
17)The characteristic polynomial f(x) for the LFSR referred in Q16 is due to the tap points h1 and h2. These are set to _____ respectively. ***1 point***

- 0,0
- 0,1
- 1,0
- 1,1

No, the answer is incorrect.
Score: 0

Accepted Answers:
0,1

18) Consider a modular LFSR shown below. The characteristic function f(x) for the circuit is _____. ***1 point***



- 1 + x
- $1 + x + x^4$
- $1 + x^2 + x^3$
- $1 + x^3 + x^4$

No, the answer is incorrect.
Score: 0

Accepted Answers:
$1 + x^3 + x^4$

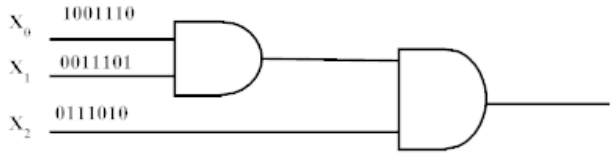
19)Only for a few characteristic polynomials the LFSR is maximal length; such polynomials are called _____ polynomials. ***1 point***

- Primitive
- Non- primitive
- Implicit
- Exhaustive

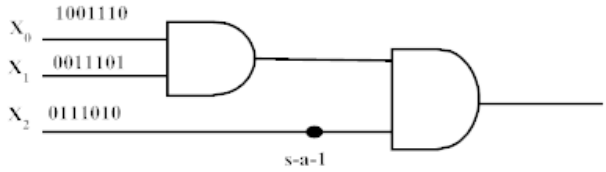
No, the answer is incorrect.
Score: 0

Accepted Answers:
Primitive

20) Consider the circuit shown below, which detects the stuck-at-1 fault using the concept of response compaction based on "number of 1s". Which of the following is true? ***1 point***



(a) Normal Circuit



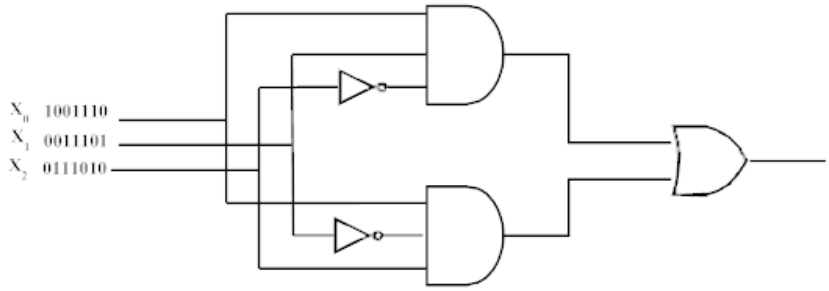
(b) Circuit with s-a-1 fault

- The fault can be detected as the number of 1s under normal condition is 1 while it is 0 under fault.
- The fault can be detected as the number of 1s under normal condition is 1 while it is 2 under fault.
- The fault can be detected as the number of 1s under normal condition is 2 while it is 1 under fault.
- The fault cannot be detected as the number of 1s under normal condition is same as that under fault.

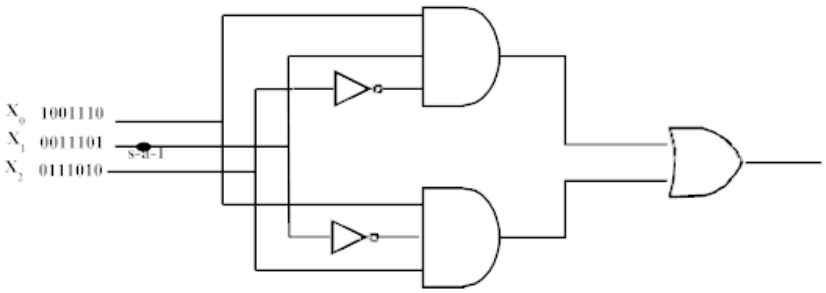
No, the answer is incorrect.
Score: 0

Accepted Answers:
The fault can be detected as the number of 1s under normal condition is 1 while it is 2 under fault.

21) Consider the circuit shown below, which detects the stuck-at-1 fault using the concept of response compaction based on "transition count". Which of the following is true? ***1 point***



(a) Normal Circuit



(b) Circuit with s-a-fault

- The fault can be detected as the transition count under normal condition is 1 while it is 0 under fault.
- The fault can be detected as the transition count under normal condition is 1 while it is 2 under fault.
- The fault can be detected as the transition count under normal condition is 2 while it is 3 under fault.
- The fault cannot be detected as the transition count under normal condition is same as that under fault.

No, the answer is incorrect.
Score: 0

Accepted Answers:

The fault can be detected as the transition count under normal condition is 2 while it is 3 under fault.

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