X

Unit 14 - Combinational Circuit Test Pattern Generation

Week 11 Assignment

The due date for submitting this assignment has passed. **Due on 2016-10-06, 23:58 IST.**

Submitted assignment

1) Which of the following statement is generally valid for a circuit? ***1 point***

- All faults are “easy to test"
- All faults are “difficult to test”
- Few faults are “easy to test” and most others are “difficult to test”
- Most faults are “easy to test” and few are “difficult to test”

No, the answer is incorrect.
Score: 0

Accepted Answers:
Most faults are “easy to test” and few are “difficult to test”

2) The test patterns for “easy to test faults” are derived by ____ ***1 point***

- Fault simulation algorithms
- Sensitization–propagation -justification approach
- Boolean Difference approach
- All the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Fault simulation algorithms

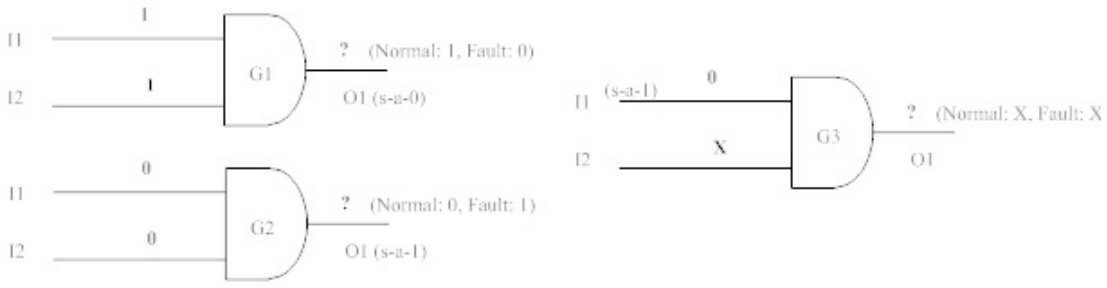
3) The test patterns for “difficult to test faults” are derived by ____ ***1 point***

- Fault simulation algorithms
- Sensitization–propagation -justification approach
- Both (a) and (b)
- Other than the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Sensitization–propagation -justification approach

4) Let us consider a 2-input AND gates shown below where the inputs are marked using notations from Roth’s 5-valued algebra. What is the output notation at the **?** marked net i.e., output of gate G1? ***1 point***



- 0
- 1
- D
- X

No, the answer is incorrect.
Score: 0

Accepted Answers:
D

5) Consider the figure referred in Q4. What is the output notation at the ? marked net i.e., output of gate G2? ***1 point***

- 0
- D'
- D
- X

No, the answer is incorrect.
Score: 0

Accepted Answers:
D'

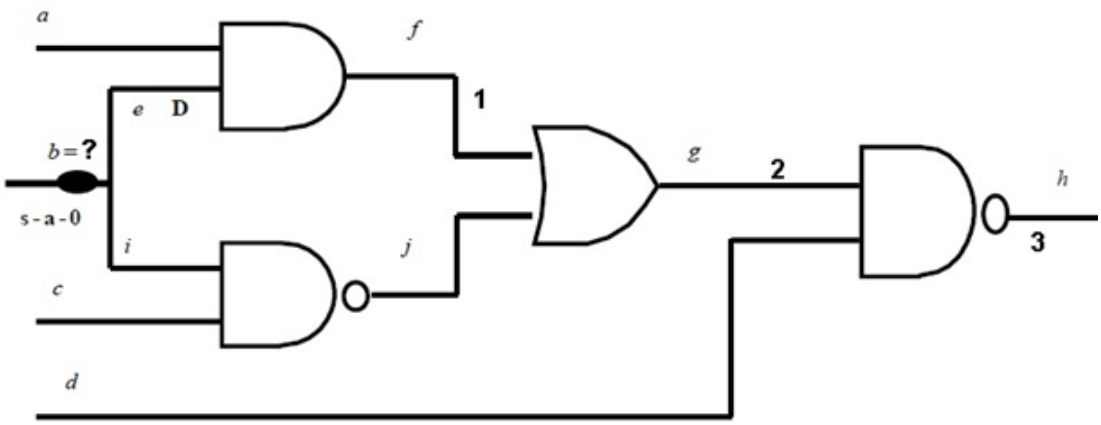
6) Consider the figure referred in Q4. What is the output notation at the ? marked net i.e., output of gate G3? ***1 point***

- 0
- 1
- D
- X

No, the answer is incorrect.
Score: 0

Accepted Answers:
X

7) If one wants to take the path “e-f-g-h” shown below for propagating the fault effect to the output *h*. The signals labeled as 1, 2, 3 in the nets of the path are assigned in terms of Roth’s 5 valued algebra. The signal value of the net labeled with 1 is _____. ***1 point***



- 0
- 1
- D
- X

No, the answer is incorrect.
Score: 0

Accepted Answers:
D

8) Consider the figure referred in Q7. The signal value of the net labeled with 2 is _____. ***1 point***

- 0
- 1
- D
- D'

No, the answer is incorrect.
Score: 0

Accepted Answers:
D

9) The signal value of the net labeled with 3 is _____. ***1 point***

- 0
- 1
- D
- D'

No, the answer is incorrect.
Score: 0

Accepted Answers:
D'

10) The path “e-f-g-h” in figure referred in Q7 cannot be used for testing the s-a-0 fault because _____. ***1 point***

- Fault cannot be sensitized
- Fault cannot be propagated to the output
- Justification conflict on the net “j”
- The statement is wrong. Path “e-f-g-h” in figure can be used for testing the s-a-0 fault.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Justification conflict on the net “j”

11) Which is (are) the singular cover for a 2-input AND gate. Let us assume A, B are the input variables and the C is the output variable. ***1 point***

- A=0, B=X, C=0
- A=X, B=0, C=0
- A=1, B=1, C=1
- All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
All of the above

12) The D-frontier comprises gates whose output value is X and at least one of its input is ____ . ***1 point***

- Only D
- Only D'
- Both (a) and (b)
- None

No, the answer is incorrect.
Score: 0

Accepted Answers:
Both (a) and (b)

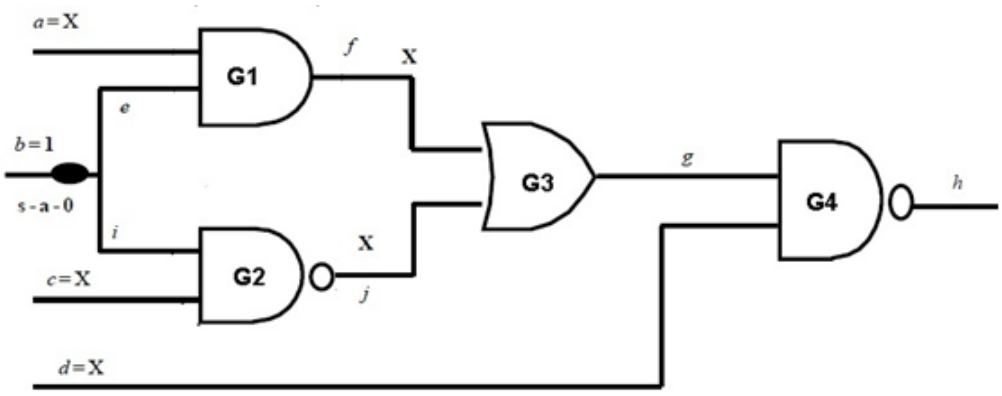
13) Any gate in D-frontier can be used for fault _____. ***1 point***

- Sensitization
- Propagation
- Justification
- All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Propagation

14) Let us consider a circuit shown below. The only way to sensitize the s-a-0 fault on the net “b” is to make it to 1. The nets “e” and “i" are assigned as _____. ***1 point***



- e=D, i=D
- e=D', i=D'
- e=D, i=D'
- e=D', i=D

No, the answer is incorrect.
Score: 0

Accepted Answers:
e=D, i=D

15) Considering the answer in Q14, which gate(s) is (are) treated as D-frontier? ***1 point***

- G1
- G2
- Both G1 and G2

- None

No, the answer is incorrect.
Score: 0

Accepted Answers:
Both G1 and G2

16) The J-frontier comprises gates whose ____. ***1 point***

- Output value is known but its inputs are not yet computed.
- Output value is not known and its inputs are not yet computed.
- Output value is known as well as its inputs are known.
- Neither output value is known nor are its inputs known.

No, the answer is incorrect.
Score: 0

Accepted Answers:
Output value is known but its inputs are not yet computed.

17) Any gate in J-frontier can be used for fault _____. ***1 point***

- Sensitization
- Propagation
- Justification
- All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Justification

18) Consider the circuit referred in Q14. Assume that it was decided that fault effect D be propagated via the net “j”. So, j=D by forward implication. Which gate is the J-frontier? ***1 point***

- G1
- G2
- Both G1 & G2
- None

No, the answer is incorrect.
Score: 0

Accepted Answers:
G1

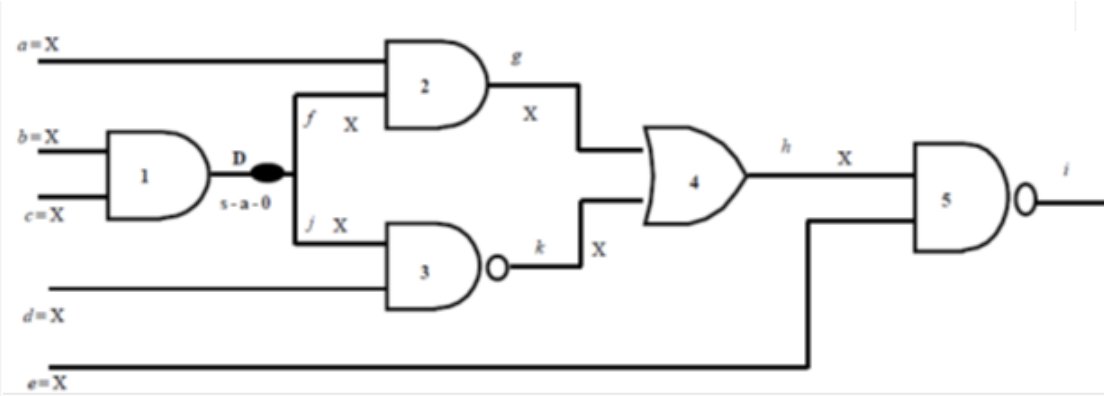
19) For the J-frontier found in Q18 and propagating the fault effect D to the net “g”, the net “f” must be set to ____. ***1 point***

- 0
- 1
- X
- D

No, the answer is incorrect.
Score: 0

Accepted Answers:
0

20) Let us consider a simple digital circuit with a s-a-0 fault at the output of gate-1 shown below. To sensitize the s-a-0 fault, 1 has to be applied in the corresponding net, thereby making signal of the net as D. Now J- frontier and D-frontier needs to be computed. Gate 1 is ___ frontier. ***1 point***



- D
- J
- Both (a) and (b)
- None

No, the answer is incorrect.
Score: 0

Accepted Answers:
J

21) Consider Level 2 and Level 3 of circuit referred in Q20. The inputs of gate-2 and gate-3 are D, and the outputs are X. D-frontier is ___. ***1 point***

- gate-2
- gate-3
- gate-2 and gate-3
- gate-1, gate-2 and gate-3

No, the answer is incorrect.
Score: 0

Accepted Answers:
gate-2 and gate-3

22) Consider the circuit referred in Q20. To justify the D at output of gate-1 using backward implication, we get input (b,c) as ____. ***1 point***

- 1,1
- 1,0
- 0,1
- 0,0

No, the answer is incorrect.
Score: 0

Accepted Answers:
1,1

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