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Courses » VLSI Design Verification and test

Announcements

Course

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Mentor

Unit 13 - Fault Simulation and Testability Measures

Course outline

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Resource Sharing and Binding in HLS

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Physical Design

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Syntax and semantics of CTL, Equivalences between CTL formulas and Introduction to Model Checking

CTL Model checking Algorithms and Introduction to Binary Decision Diagrams

Binary Decision Diagram and Symbolic model checking

Introduction to Digital Testing

Fault Simulation and Testability Measures

- ☐ Fault Simulation I
- ☐ Fault Simulation II
- ☐ Fault Simulation III
- ☐ Testability Measures (SCOAP)
- ☐ Quiz : Week 10 Assignment

Combinational Circuit Test Pattern Generation

Sequential Circuit Testing and Scan Chains

Week 10 Assignment

The due date for submitting this assignment has passed.

Due on 2016-10-01, 23:58 IST.

Submitted assignment

1) The procedure to generate a test input for a given a fault is called _____.

1 point

- ☐ Test Procedure Generation
- ☐ Test Pattern Generation
- ☐ Test Parameter Generation
- ☐ None

No, the answer is incorrect.

Score: 0

Accepted Answers:

Test Pattern Generation

2) How many broad steps are involved to generate a test pattern?

1 point

- ☐ Two
- ☐ Three
- ☐ Four
- ☐ Not fixed, depends on circuit

No, the answer is incorrect.

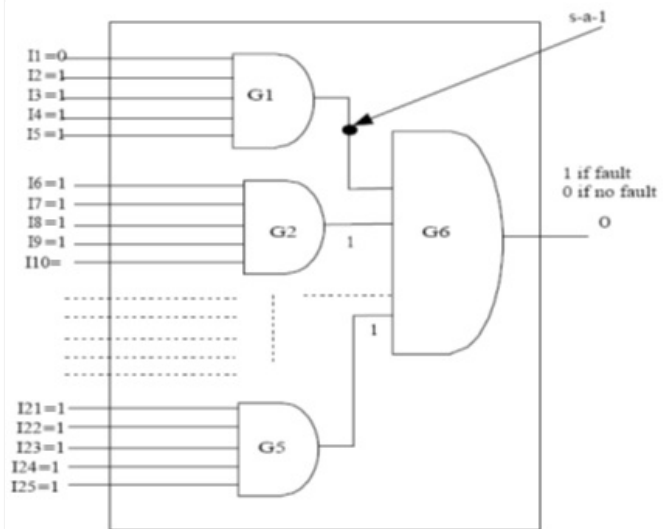
Score: 0

Accepted Answers:

Three

3) How many choices are there to sensitize the s-a-1 fault at OG1 (output of Gate 1) in Figure shown below?

1 point



- ☐ 2^5-1
- ☐ 5^2-1
- ☐ 2^5+1

Built In Self Test (BIST)

☐ 5^2+1

No, the answer is incorrect.

Score: 0

Accepted Answers:

 2^5-1

4) How many inputs patterns are possible to propagate the fault effect to OG6 (output of Gate 6) in Figure referred in Q3? **1 point**

- ☐ 1
☐ 2
☐ 3
☐ 4

No, the answer is incorrect.

Score: 0

Accepted Answers:

1

5) For your answer in previous question, the primary inputs I6 to I25 are set to _____. **1 point**

- ☐ All 1s
☐ All 0s
☐ Combination of 0s and 1s
☐ None

No, the answer is incorrect.

Score: 0

Accepted Answers:

All 1s

6) Let us take a random input "10001 11111 11111 11111 11111" for the figure referred in Q3. Then the faults detected at OG1 (output of Gate 1) and OG6 (output of Gate 6) are ____ and ____ respectively. **1 point**

- ☐ S-a-1, S-a-1
☐ S-a-0, S-a-1
☐ S-a-1, S-a-0
☐ S-a-0, S-a-0

No, the answer is incorrect.

Score: 0

Accepted Answers:

S-a-1, S-a-1

7) If some faults are difficult to be detected in a circuit, _____ approach is used to generate test patterns for them. **1 point**

- ☐ Sensitize-Propagate-Justify
☐ Random
☐ Manual
☐ None of the above

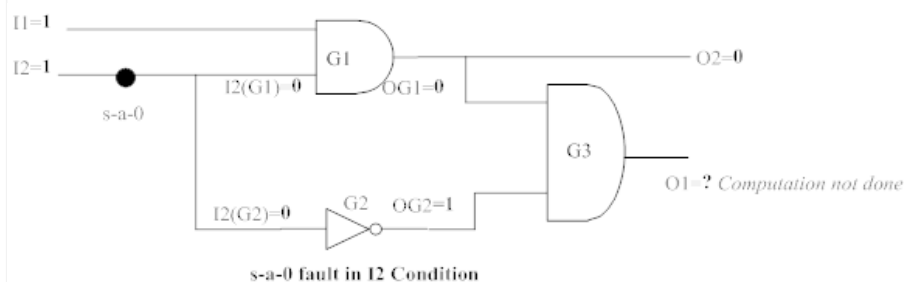
No, the answer is incorrect.

Score: 0

Accepted Answers:

Sensitize-Propagate-Justify

8) Consider an event driven simulation for a circuit shown below for input pattern I1=1, I2=1 and s-a-0 fault in I2. At time t=0 the event list = {I1=1, I2=1}. What is the activity list? **1 point**



- ☐ I2(G1), I2(G2)
☐ I2(G1), OG2, I2(G2), O2
☐ I2(G1), O2
☐ I2(G1), OG1

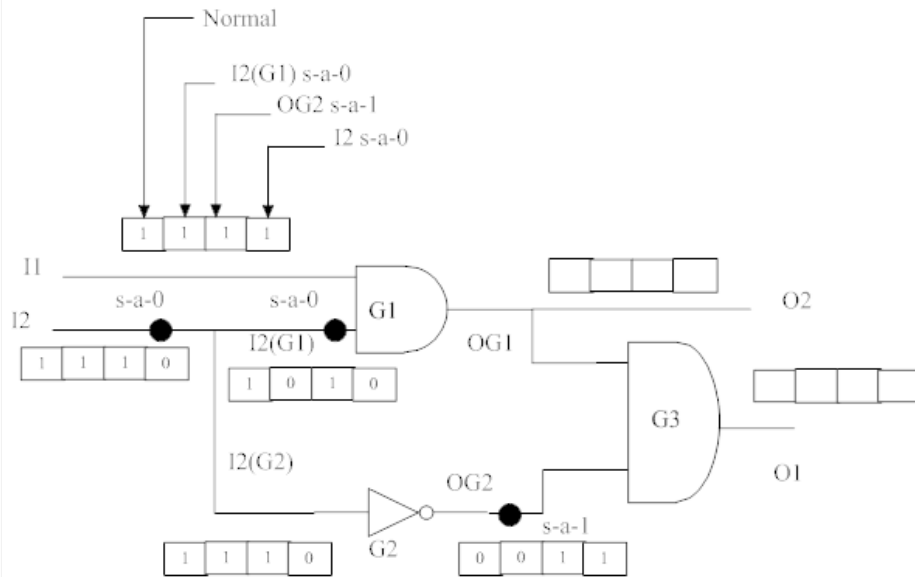
No, the answer is incorrect.

Score: 0

Accepted Answers:

I2(G1), I2(G2)

9) Let us consider a circuit shown below that that illustrates parallel fault simulation of a circuit. The simulation uses **1 point** a 4-word array. For the input I1=1 and I2=1 in the circuit, the array at the O2 is ____.



- ☐ 1000
- ☐ 0101
- ☐ 1010
- ☐ 0011

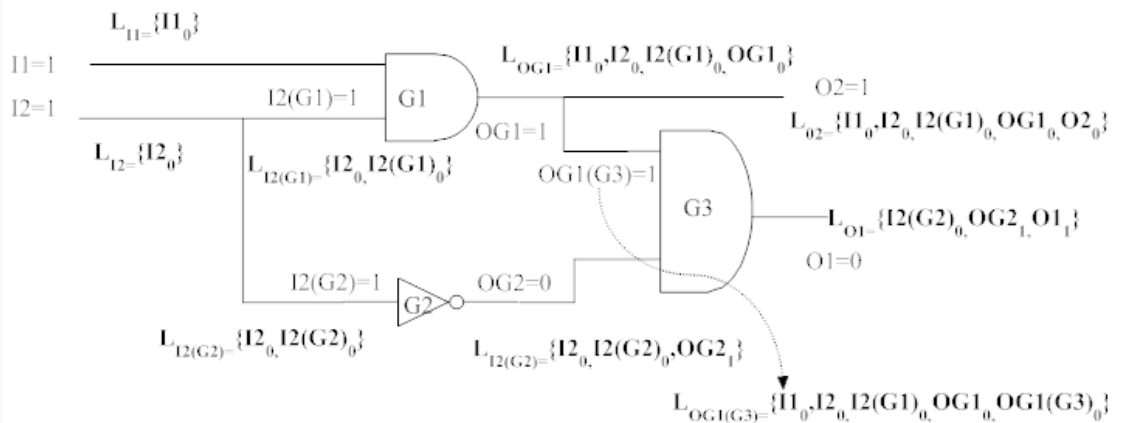
No, the answer is incorrect.

Score: 0

Accepted Answers:

1010

10) By studying the fault list at the primary outputs (L_{O1} and L_{O2}) in the circuit shown below, we find that deductive **1 point** fault simulation discovered ____ faults detectable by pattern I1=1, I2=1.



- ☐ 4
- ☐ 8
- ☐ 16
- ☐ 32

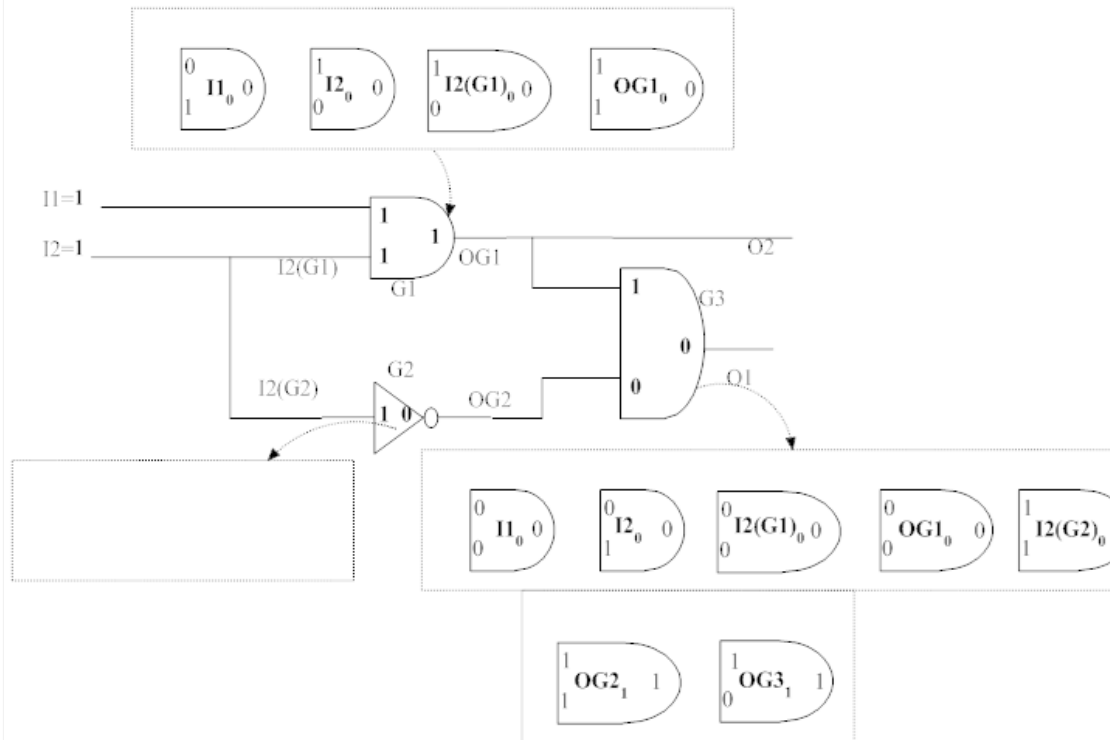
No, the answer is incorrect.

Score: 0

Accepted Answers:

8

11) Figure shown below illustrates an example of a concurrent fault simulation and the inputs are I1=1 and I2=1. The **1 point** NOT gate G2 can be affected by ____ fault(s).



- ☐ 2
☐ 3
☐ 4
☐ 5

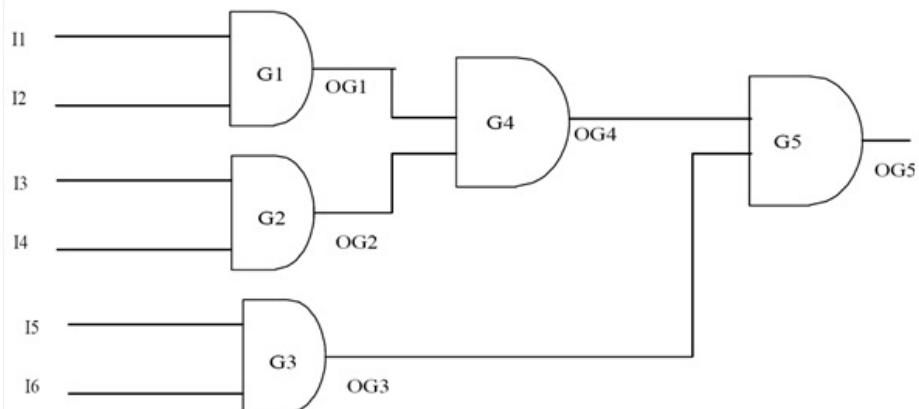
No, the answer is incorrect.

Score: 0

Accepted Answers:

3

12) Let us take the circuit shown below to test a s-a-0 fault at OG4. Note that sensitize-propagate-justify approach is **1 point** used. If the sensitization is made at OG4=1 in the circuit, then the input pattern is set as ____.



- ☐ I1=1, I2=1, I3=1, I4=1
☐ I2=1, I3=1, I4=1, I5=1
☐ I3=1, I4=1, I5=1, I6=1
☐ I1=0, I2=0, I3=0, I4=0

No, the answer is incorrect.

Score: 0

Accepted Answers:

I1=1, I2=1, I3=1, I4=1

13) If the input I1=1, I2=1, I3=1, I4=1 is applied at the circuit referred in Q12, to test a s-a-0 fault at OG4, then justification is achieved by ____.

1 point

- ☐ I5=0, I6=0
☐ I5=0, I6=1
☐ I5=1, I6=0

☐ I5=1, I6=1

No, the answer is incorrect.

Score: 0

Accepted Answers:

I5=1, I6=1

14) The SCOAP is a fast ____ technique to compute difficulty in controlling and observing signals in a net in a circuit. **1 point**

- ☐ Heuristic
☐ Deterministic
☐ Distributed
☐ ATPG based

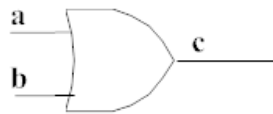
No, the answer is incorrect.

Score: 0

Accepted Answers:

Heuristic

15) We apply the SCOAP Rules to Compute Combinational Observability (CO) for the Logic Gate shown below. To observe the value of input "a" at the primary output we compute CO(a). CO(a) is _____. **1 point**



- ☐ $CC0(a) + CO(b) + 1$
☐ $CC0(b) + CO(c) + 1$
☐ $\text{Max}[CC0(b), CO(c)] + 1$
☐ $\text{Min}[CC0(b), CO(c)] + 1$

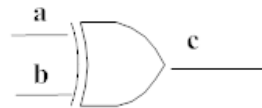
No, the answer is incorrect.

Score: 0

Accepted Answers:

$CC0(b) + CO(c) + 1$

16) In circuit shown below, CO(a) is _____. **1 point**



- ☐ $\text{Max}(CC0(b), CC1(b)) + CO(c) + 1$
☐ $\text{Min}(CC0(b), CC1(b)) + CO(c) + 1$
☐ $\text{Max}[CC0(b), CO(c)] + 1$
☐ $\text{Min}[CC0(b), CO(c)] + 1$

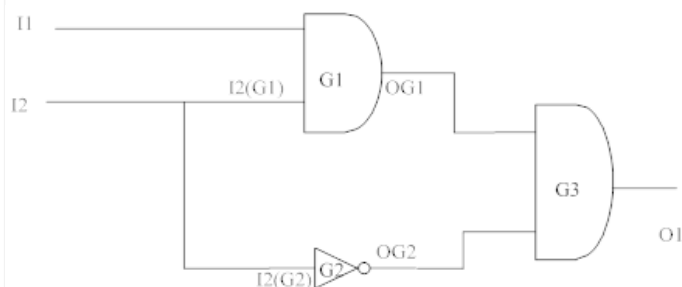
No, the answer is incorrect.

Score: 0

Accepted Answers:

$\text{Min}(CC0(b), CC1(b)) + CO(c) + 1$

17) Consider the simple circuit shown below for the Combinational Controllability Calculation in the nets. Consider Level 1 in the circuit, where all the primary input nets (I1, I2) and their fanout branches (I2(G1) and I2(G2)) are directly assigned as 1, 1, 1, 1 respectively. Now, consider Level 2 in the circuit. The value of the CC0(OG1) is _____. **1 point**



- ☐ 1
☐ 2

- ☐ 3
☐ 4

No, the answer is incorrect.

Score: 0

Accepted Answers:

2

18) Consider Level 2 in a circuit referred in Q17. The value of the CC1(OG1) is ____.

1 point

- ☐ 1
☐ 2
☐ 3
☐ 4

No, the answer is incorrect.

Score: 0

Accepted Answers:

3

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