



Unit 2 - Introduction and Overview of VLSI Design

Course outline

How to access the portal ?

Introduction and Overview of VLSI Design

- ☒ Introduction (Part-1)
- ☒ Introduction (Part-2)
- ☒ Overview of VLSI Design Flow
- ☒ High Level Synthesis Overview (Part-1)
- ☒ High Level Synthesis Overview (Part-2)
- ☐ Quiz : WEEK 1 ASSIGNMENT

Scheduling in High-Level Synthesis

Resource Sharing and Binding in HLS

Logic Synthesis

Physical Design

Introduction to Verification Techniques

Syntax and semantics of CTL, Equivalences between CTL

WEEK 1 ASSIGNMENT

The due date for submitting this assignment has passed. **Due on 2016-07-31, 05:29 IST.**

Submitted assignment

1) Determine the correct order of the design steps starting from initial concept to chip. **1 point**

- ☐ Specification, Implementation, Prototyping, Manufacturing
- ☐ Specification, Prototyping, Implementation, Manufacturing
- ☐ Prototyping, Specification, Implementation, Manufacturing
- ☐ Manufacturing, Prototyping, Specification, Implementation

No, the answer is incorrect.

Score: 0

Accepted Answers:

Specification, Implementation, Prototyping, Manufacturing

2) RTL (Register Transfer Logic) design is obtained as an output of _____ phase **1 point**

- ☐ Architectural Synthesis
- ☐ Logic Synthesis
- ☐ Geometrical Synthesis
- ☐ High-Level Synthesis

No, the answer is incorrect.

Score: 0

Accepted Answers:

Architectural Synthesis

High-Level Synthesis

3) _____ view describes the function of the circuit regardless of its implementation **1 point**

- ☐ Physical
- ☐ Structural
- ☐ Behavioral
- ☐ Logic

No, the answer is incorrect.

Score: 0

Accepted Answers:

Behavioral

4) The sequence of steps involved in architectural synthesis: **1 point**

- ☐ Scheduling, Allocation, Identifying hardware resources, Binding, Controller generation
- ☐ Identifying hardware resources, Scheduling, Allocation, Binding, Controller generation

formulas and
Introduction to
Model Checking

CTL Model
checking
Algorithms and
Introduction to
Binary Decision
Diagrams

Binary Decision
Diagram and
Symbolic model
checking

Introduction to
Digital Testing

Fault Simulation
and Testability
Measures

Combinational
Circuit Test
Pattern
Generation

Sequential
Circuit Testing
and Scan Chains

Built In Self Test
(BIST)

- ☐ Identifying hardware resources, Allocation, Binding, Scheduling, Controller generation
- ☐ Identifying hardware resources, Allocation, Scheduling, Binding, Controller generation

No, the answer is incorrect.

Score: 0

Accepted Answers:

Identifying hardware resources, Scheduling, Allocation, Binding, Controller generation

5) Registers are connected to functional units via _____ and functional units are connected to registers via _____ **1 point**

- ☐ MUXs, DMUXs
- ☐ DMUXs, MUXs

No, the answer is incorrect.

Score: 0

Accepted Answers:

MUXs, DMUXs

6) Micro-architectural optimization happens in the _____ phase **1 point**

- ☐ Architectural Synthesis
- ☐ Logic Synthesis
- ☐ Geometrical Synthesis
- ☐ High-level Synthesis

No, the answer is incorrect.

Score: 0

Accepted Answers:

Logic Synthesis

Previous Page

End