X

Unit 16 - Applications of transistors and basics of microelectronic fabrication

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Course outline

How to access the portal

Basics of semiconductor physics

Equilibrium carrier concentration

Carrier transport

p-n junction

Applications of p-n junctions and details of metal-semiconductor junction

Bipolar Junction Transistor

Metal Oxide Semiconductor Capacitor

MOSFET

Interaction

Week 12_Assignment

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment. **Due on 2019-04-24, 23:59 IST.**

1) In the three terminal breakdown measurement of a GaN HEMT with a pinch-off voltage of -2V, which of these gate voltages are permissible assuming a drain voltage of 10V (neglecting gate leakage and other leakages)? ***1 point***

- 4V
- -1V
- 1V
- -4V

No, the answer is incorrect.
Score: 0

Accepted Answers:
-4V

2) A power MOSFET is used as a switch. The switch operates in _____ region with _____ On-state resistance in on-state and _____ region in off-state with _____ breakdown voltage respectively. ***1 point***

- Linear, low, cut-off, high
- Saturation, low, cut-off, low
- Linear, high, cut-off, low
- Saturation, low, cut-off, low

No, the answer is incorrect.
Score: 0

- Switching loss
- All losses are independent of frequency of operation

No, the answer is incorrect.
Score: 0

Accepted Answers:
Switching loss

4) A transistor has a very low on-resistance, high breakdown-voltage and a very high degree of channel length modulation i.e. the output resistance of the transistor is very low. Which of the following applications can this transistor be used for? ***1 point***

- Power switching
- RF amplifier
- Analog amplifier
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Power switching

5) A process engineer is designing an nMOS transistor for high speed digital logic. Which method should he adopt for gate oxide deposition? ***1 point***

- Wet oxidation
- Dry oxidation
- Sputtering
- Evaporation

No, the answer is incorrect.
Score: 0

Accepted Answers:
Dry oxidation

6) A process engineer is designing an nMOS transistor for high speed digital logic. Which method should he adopt to get an anisotropic doping for channel? ***1 point***

- Diffusion
- Ion implantation
- Both a and b
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Ion implantation

7) In a CMOS transistor, which method should we use for source and drain contact to get a conformal metal layer? ***1 point***

- Evaporation
- Sputtering
- Both a and b
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Sputtering

8) In the fabrication lab in IISc, optical lithography is used to define 100 um interconnects for CMOS transistor. What is the wavelength used in this optical lithography technique? ***1 point***

- 365 nm
- 450 nm
- 220 nm
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
365 nm

9) A process engineer is designing an nMOS transistor for digital logic. Which method should he adopt to get anisotropic etching of silicon dioxide? ***1 point***

- Wet etching
- Dry etching
- Both a and b
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Dry etching

10) What does sub-nm technology node represent in silicon technology? ***1 point***

- Gate width
- Poly pitch
- Both a and b
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Poly pitch

Previous Page End