# Unit 6 - Week 4



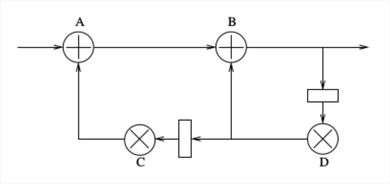
## Assignment 4

**The due date for submitting this assignment has passed.**
**As per our records you have not submitted this assignment.**

**Due on 2019-08-28, 23:59 IST.**

For the diagram shown, assume input is $x(n)$ and output is $y(n)$. Also assume that each node A, B, C, D are functional units (adders and multipliers as indicated), and that the rectangular blocks are registers(or delay elements in general).

Also assume that you have one type of hardware unit that can perform either addition or multiplication,each pipelined to depth 1 (ie, latency = 1).




1) What is the length of the critical path (in clock cycles):

No, the answer is incorrect.
Score: 0

Accepted Answers:
*(Type: Numeric) 3*

*1 point*

2) What is the minimum folding order N (number of cycles) that can be used to obtain a valid folding schedule for this architecture if only one hardware unit is available?

No, the answer is incorrect.
Score: 0

Accepted Answers:
*(Type: Numeric) 4*

*1 point*

3) What is the minimum folding order N (number of cycles) that can be used to obtain a valid folding schedule for this architecture if exactly two such hardware units are available?

No, the answer is incorrect.
Score: 0

Accepted Answers:
*(Type: Numeric) 3*

*1 point*

4) What is the minimum folding order N (number of cycles) that can be used to obtain a valid folding schedule for this architecture if unlimited hardware units are available?

No, the answer is incorrect.
Score: 0

Accepted Answers:
*(Type: Numeric) 3*

*1 point*

5) Assuming there are two hardware units available and N = 4, which of the following folding sets are valid and will not result in a negative value of $D_F$ on any edge? ***3 points***

- $S_1$ = {C, A, B, –}, $S_2$ = {D, –, –, –}
- $S_1$ = {C, A, B, –}, $S_2$ = {–, –, –, D}
- $S_1$ = {C, B, A, –}, $S_2$ = {D, –, –, –}
- $S_1$ = {C, D, A, B}, $S_2$ = {–, –, –, –}
- $S_1$ = {A, B, C, –}, $S_2$ = {D, –, –, –}
- $S_1$ = {–, A, D, –}, $S_2$ = {C, –, –, B}

No, the answer is incorrect.
Score: 0

Feedback:
***Solution:*** *This can be verified by computing $D_F$ on each edge. But even simpler is to just draw a chart of which operation happens at each time instant, and connect with edges as appropriate. This is similar to the analysis of ASAP and ALAP schedules*

Accepted Answers:
*$S_1$ = {C, A, B, –}, $S_2$ = {D, –, –, –}*
*$S_1$ = {C, D, A, B}, $S_2$ = {–, –, –, –}*
*$S_1$ = {–, A, D, –}, $S_2$ = {C, –, –, B}*

For the following questions, assume the same system above is to be implemented on a single piece of hardware, and we have proposed the folding order S = {A, B, C, D}, with N = 4

6) What is the value of $D_F$ for the edge B – D?

No, the answer is incorrect.
Score: 0

Accepted Answers:
*(Type: Numeric) 5*

*1 point*

7) What is the value of $D_F$ for the edge D – C?

No, the answer is incorrect.
Score: 0

Accepted Answers:
*(Type: Numeric) 2*

*1 point*

8) What is the value of $D_F$ for the edge D – B?

No, the answer is incorrect.
Score: 0

Accepted Answers:
*(Type: Numeric) -3*

*1 point*