

Optimization Techniques for Digital VLSI Design - - Unit 10 - Verification [Part-2]

- Ordered Binary Decision Diagrams
- High Level decision diagrams
- State based models

No, the answer is incorrect.

Score: 0

Accepted Answers: Ordered Binary Decision Diagrams

4) Choose the expression which is represented by the OBDD.

1 point



$$\overline{x_1} x_2 + x_1 \overline{x_2}$$

No, the answer is incorrect. Score: 0

Accepted Answers:

$$\overline{x_1} x_2 + x_1 \overline{x_2}$$

5)

Let $f(a,b) = \overline{ab} + \overline{ab} + a\overline{b} + a\overline{b}$ be a Boolean function. Which of the following is true:

- f is independent of only a
- f is independent of only b
- f is independent of both a and b
- None of the above

No, the answer is incorrect. Score: 0 Accepted Answers:

f is independent of both a and b

6) Bounded Model checking is generally solved using

1 point

1 point

Optimization Techniques for Digital VLSI Design - - Unit 10 - Verification [Part-2]

- Boolean Satisfiability Solvers
- Ordered Binary Decision Diagrams
- High Level decision diagrams
- None of the above

No, the answer is incorrect. Score: 0 Accepted Answers:

Boolean Satisfiability Solvers

7) Choose the correct statements:

1 point

i. In symbolic model checking, finite state machines are used represent state space.

ii. State space explosion problem may also appear in a very small system with less number of states.iii. Model checking using OBDD is called symbolic model checking.

iv. In symbolic model checking, individual states are not represented.

i.	and	iii.	are	true.
••	and		000	u ao.

- iii and iv. are true.
- i. and ii. are true.
- i., iii. and iv. are true.

No, the answer is incorrect. Score: 0

Accepted Answers:

iii and iv. are true.

8) Let B_f is a ROBDD of Boolean expression f. If B_f contains only one node and that is labeled with **1** point 1, then which of the followings is true for f?

- f is not a valid Boolean expression.
- f is not a satisfiable Boolean expression
- f is a valid Boolean expression
- None of the above

No, the answer is incorrect. Score: 0

Accepted Answers: f is a valid Boolean expression

9) Choose the Boolean expression representing all the transitions in the figure with help of OBDD. 1 point



Optimization Techniques for Digital VLSI Design - - Unit 10 - Verification [Part-2] No, the answer is incorrect. Score: 0

Accepted Answers:

$$f = \overline{x_1} \, \overline{x_2} \, \overline{x_1}' \, x_2' + \overline{x_1} \, x_2 \, x_1' \, \overline{x_2}' + x_1 \, \overline{x_2} \, x_1' \, \overline{x_2}'$$

10)

1 point

Let B_f be a OBDD representing Boolean function $f(a,b,c) = (a+\overline{a}) \wedge (b+\overline{b}) \wedge (c+\overline{c})$ Assume order of variables in all cases is $\langle a,b,c \rangle$. The number of nodes in the OBD is

- Nodes=2
- Nodes=1
- Nodes=3
- Nodes=4

No, the answer is incorrect. Score: 0

Accepted Answers: Nodes=1

11)Choose the correct statements about Bounded Model Checking:

1 point

- i. Bounded Model Checking guarantees that all detectable errors in the model will be covered.
- ii. Bounded Model Checking is used for detecting all possible faults in more accurate way.

iii. Bounded Model Checking can be used to deal with state space explosion problem up to certain extent with some compromise in verification coverage.

iv. In Bounded Model Checking we try to find a bad state or a counter example with in a fixed number of states.

- i and iii are true.
- ii and iv are true.
- iii and iv are true.
- ii and iv are true.

No, the answer is incorrect. Score: 0

Accepted Answers: *iii and iv are true.*

12) Let B_f be a ROBDD of a Boolean expression f. If there exists 4 paths to terminal node 1 and 3 **1** point paths to terminal node 0 in B_f , then what can we say about f.

- f is valid but not satisfiable
- f is valid and satisfiable
- f is neither valid nor satisfiable
- f is not valid but satisfiable

No, the answer is incorrect. Score: 0

Accepted Answers: f is not valid but satisfiable

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