X

Unit 4 - RTL Optimizations [Part-1]

Assignment for Week 2

The due date for submitting this assignment has passed. **Due on 2018-02-21, 00:00 IST.**

Submitted assignment

1) Consider the following function. Assume that integer width is 16 bits. Also, the function returns 24 bits width data. After computation of a * b, how many bits of the output needs to be truncated? ***1 point***

```
int24 fn (int a, int b)
{
    long int temp;
    temp = a * b;
    return temp;
}
```

- 4
- 8
- 12
- 16

No, the answer is incorrect.
Score: 0

Accepted Answers:
8

2) Consider the following code: ***1 point***

```
x = 3 ;
y = 1 + x ;
z = x + y * 5 ;
```

If we use constant propagation, then what will be the value of x, y and z ?

- 3, 1, 5
- 3, 4, 5
- 3, 4, 4
- 3, 4, 23

No, the answer is incorrect.
Score: 0

Accepted Answers:
3, 4, 23

3) Consider the following code. If the inner-most loop (loop_J) is only pipe lined, how many cycles is required to complete the execution of the loop? Assume that one cycle is required to execute ***1 point***

the expression acc = A[i]*j + acc?

```
dout_t loop_p(din_t A[N])
{
    int i, j
    state dout_t a;
    for(i=0; i<20; i++){    //Loop_I, outer loop
    {
      for(j=0; j<20; j++){//Loop_J, inner loop
          acc = A[i]*j + acc;
      }
    }
    return acc;
}
```

- 1
- 20
- 200
- 400

No, the answer is incorrect.
Score: 0

Accepted Answers:
400

4) Consider the following code. Assume one clock cycle is required to execute the loop body of each loop. Also assume that the Loop_1 is fully unrolled and the Loop_2 is fully pipe lined. How many time step is required to execute this code? Ignore time required to initialize etc. ***1 point***

```
void loop_seq(din_t A[N], din_t B[n], dout_t X[n], dout_t Y[N], limit1, limit2)
{
    dout_t X_out = 0;
    dout_t Y_out = 0;
    for(i=0; i< 10; i++){  //Loop_1
          X_out = X_out + A[1];
          X[1] = X_out;
    }
    for(i=0; i< 20; i++){  //Loop2
          Y_out = Y_out + B[i];
          Y[i] = Y_out
    }
}
```

- 11
- 20
- 21
- 30

No, the answer is incorrect.
Score: 0

Accepted Answers:
21

5) If we want to replace the multiplication of the expression y = x * 64 by shift operation. What would be the equivalent expression? The ‘d << k’ denotes the number d is right shifted by k bits. Similarly, ‘d >> k’ denotes that the number d is left shifted by k bits. ***0 points***

- y = x << 6
- y = x >> 6
- y = x << 5
- y = x >> 6

No, the answer is incorrect.
Score: 0

Accepted Answers:
y = x << 6

6) S1: Code motion may reduce life time of a variable and hence may reduce number of registers. ***1 point***
S2: Loop invariant code motion is used to reduce computation times.

Which one of the above statements are TRUE about code motion?

- S1
- S2
- S1 and S2
- None of the above.

No, the answer is incorrect.
Score: 0

Accepted Answers:
S1 and S2

7) Loop unrolling causes an increase in the critical path delay. The reasons are: ***1 point***

S1: Additional operations after unrolling lead to increased sharing of resources, possibly increasing the sizes of the MUXes and hence, their delay.

S2: The number of FSM states increases leading to a larger state register and ultimately to longer FSM delays

S3: A larger number of nodes need to be scheduled.

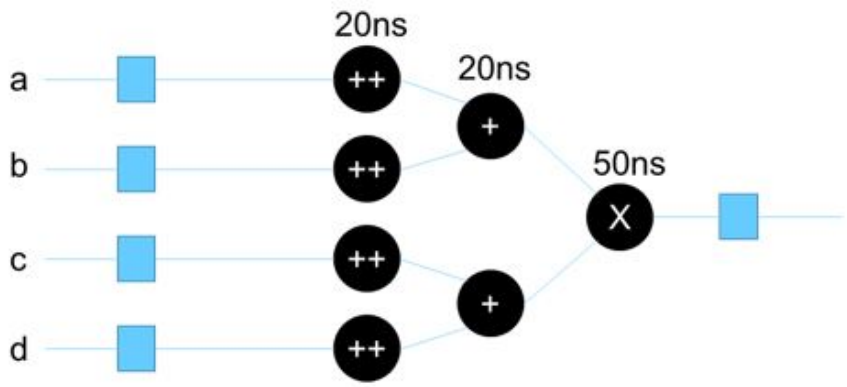
Which of them are valid reason?

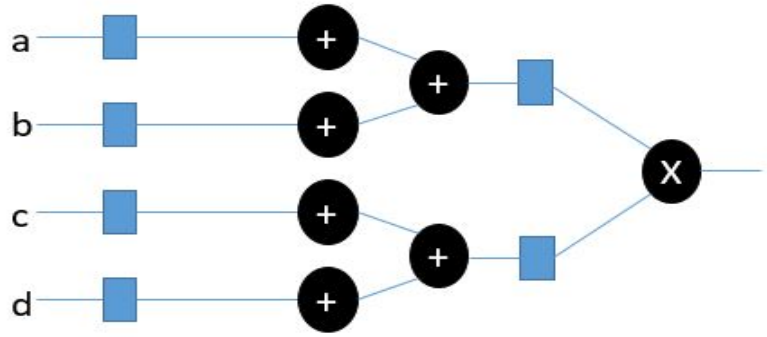
- S1 and S2
- S2 and S3
- S1 and S3
- S1, S2 and S3

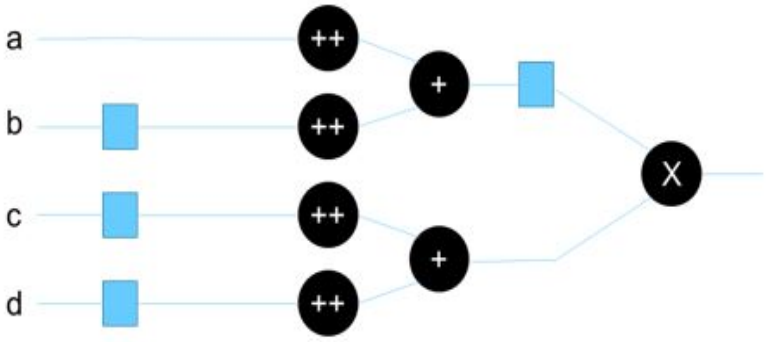
No, the answer is incorrect.
Score: 0

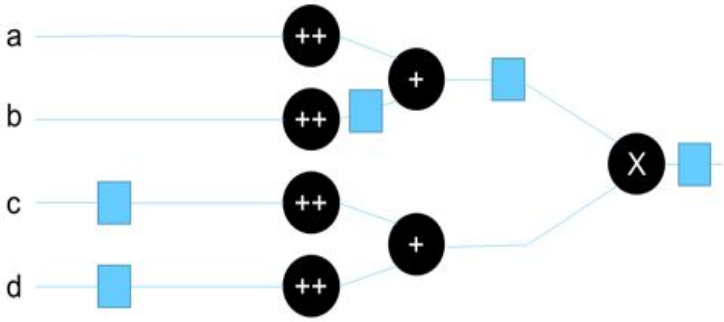
Accepted Answers:
S1, S2 and S3

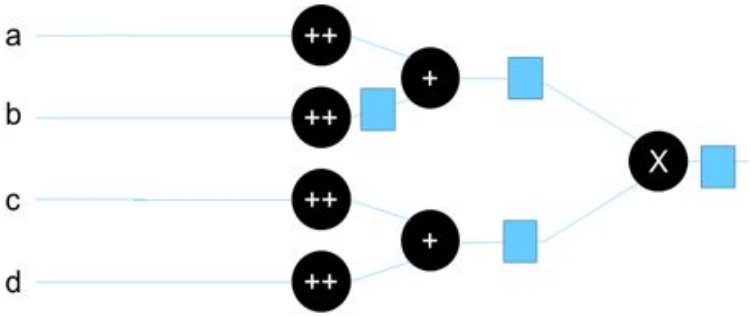
8) Consider the following circuit. What would be the correct retimed circuit? ***1 point***





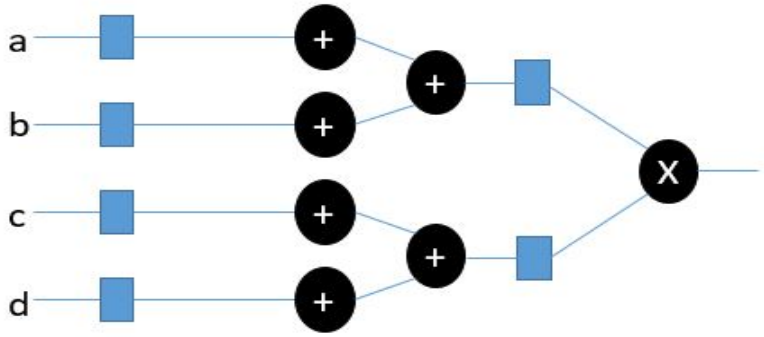






No, the answer is incorrect.
Score: 0

Accepted Answers:



9) Which one of the following is correct about the impact of variable renaming? ***1 point***

S1: Reduces computation time
S2: Always reduces the number of registers

- S1
- S2
- Both S1 and S2
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
S1

10) Which one of the following statement is correct? ***1 point***

S1: Latency is denoted by the amount of data that is processed per clock cycle
S2: Maximum allowable frequency for clock is inversely of the propagation delay as combinational logic between two flip-flops

- S1
- S2
- S1 and S2
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
S2

11) Which one of the following statement is correct? ***1 point***

S1: Replication is used to redistribute the fan-outs of high fan-out source.
S2: Replication of high-fan-out nodes is useful to reduce routing delay between flip-flops.
S3: Replication is used to move or reposition the registers in a design to improve timing.

- S1 and S2
- S1 and S3
- S2 and S3
- Only S1

No, the answer is incorrect.
Score: 0

Accepted Answers:
S1 and S2

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