X

Unit 7 - Week 6

Week 6 Assignment

Week 6 Assignment

1) Pipelining is a technique for *1 point*

- Component-Level Parallelism
- Instruction-Level Parallelism
- Core-level Parallelism
- Network-level Parallelism

Accepted Answers:
Instruction-Level Parallelism

2) Latency of the pipeline is the time taken for *1 point*

- All the instructions to be completed
- All the instruction fetches to be completed
- All the instruction execute stages to be completed
- The first instruction to be completed

Accepted Answers:
The first instruction to be completed

3) The number of registers to be inserted between two nodes in a DAG representation is decided by *1 point*

- size of the registers
- ordering in the topological sorting
- number of nodes in DAG
- number of edges in DAG

Accepted Answers:
ordering in the topological sorting

4) Stage Balancing is the process of *1 point*

- minimising the number of stages in the pipeline
- maximising the number of stages in the pipeline
- minimising the number of registers in the pipeline

- minimising the difference between the time taken by each of the stages

Accepted Answers:
minimising the difference between the time taken by each of the stages

5) An architecture with cycles per instruction(CPI) less than 1 is called **1 point**

- ILP
- Superscalar
- Pipelining
- 3DNOW

Accepted Answers:
Superscalar

6) Read After Write (RAW) hazard is called a **1 point**

- Control Hazard
- Data Hazard
- Structural Hazard
- Software Hazard

Accepted Answers:
Data Hazard

7) One of the major drawbacks of VLIW Architecture is **1 point**

- Time
- Size of memory
- Memory Aliasing
- Hardware dependency

Accepted Answers:
Memory Aliasing

8) Which one of these is a true dependency **1 point**

- WAR
- WAW
- RAR
- RAW

Accepted Answers:
RAW

9) A RAW hazard can be handled using **1 point**

- Register Renaming
- Operand Forwarding
- Pipelining
- Super-scalar operations

Accepted Answers:

Operand Forwarding

10) The hazards that Register Renaming can help in handling are **1 point**

- RAW and WAR
- WAR and RAR
- WAR and WAW
- RAW and WAW

Accepted Answers:
WAR and WAW

11) The value of Register Status indicator when the register is waiting for the value from an execution unit is **1 point**

- The register number
- Current value of register
- Execution unit number
- Expected value of the register

Accepted Answers:
Execution unit number

12) Select the most appropriate statement **1 point**
If the value for a register in the Register Status Indicator is 0, it means that

- The current register value is 0
- The current register value is being computed in some execution unit
- The current register value is either in ROB or in the register itself
- The current value of register is not available

Accepted Answers:
The current register value is either in ROB or in the register itself

13) The input and output respectively to a Content Addressable memory are **1 point**

- Address and Content
- Address and Address
- Content and Address
- Content and Program Counter

Accepted Answers:
Content and Address

Previous Page End