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Courses » Computer Organization and Architecture

Announcements **Course** Forum Progress Mentor

# Unit 12 - Week 11

## Course outline

### How to access the portal

### Week 1

### Week 2

### Week 3

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### Week 11

- Lecture 36 - Cache, Degree of Multiprogramming
- Lecture 37 (Part 1) - Shared Memory Architecture
- Lecture 37 (Part 2) - Shared Memory Architecture
- Lecture 38 (Part 1) - Virtually Indexed - Virtually Tagged and Physically Tagged Caches
- Quiz : Week 11 Assignment

## Week 11 Assignment

### Week 11 Assignment

1) In a SMA, if a core A makes a change to a variable b, the state of A is now

**1 point**

- Shared
- Invalid
- Valid
- Exclusive

#### Accepted Answers:

*Exclusive*

2) If the value of a variable a in core A and core B is changed in core B, but not reflected in core A, the state of core A is

**1 point**

- Shared
- Invalid
- Valid
- Exclusive

#### Accepted Answers:

*Invalid*

3) Multi-programming is achieved efficiently in today's processors using

**1 point**

- DMA
- Caches
- H/W Interrupt
- All of the above

#### Accepted Answers:

*DMA*

4) Using time spent on DMA for CPU computation is termed as cycle stealing

**1 point**

- True
- False

Feedback for  
Week 11

Week 11  
Solutions

**Week 12**

**Accepted Answers:**

*True*

5) Consider the following scenario. Core P1 holds an address A1 in exclusive state and it is connected to two other processors P2 and P3 through a common bus. There wont be any communication on the bus when

**1 point**

- P1 writes to A1 in P2
- P3 writes to A1 in P3
- P3 writes to A1 in P1
- P1 writes to A1 in P1

**Accepted Answers:**

*P1 writes to A1 in P1*

6) In a VIVT (Virtually Indexed Virtually Tagged) Cache, the cache is addressed using

**1 point**

- Physical Address
- Virtual Address
- Cache addressing
- Any of the above

**Accepted Answers:**

*Virtual Address*

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