



# Unit 11 - Week 10

## Course outline

### How to access the portal

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Lecture 32 - Cache

Lecture 33 - Cache Organisation

Lecture 34 - Cache - Cache Coherency, Dual Ported Cache

Lecture 35 - Multilevel Caching, Multitasking

Quiz : Week 10 Assignment

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Feedback for week 10

### Week 11

## Week 10 Assignment

Assignment Week 10

1) Transfer of data directly between a peripheral and memory without the aid of cpu is achieved **1 point** using

- NMI controller
- DDR controller
- DMA controller
- None of the above

### Accepted Answers:

*DMA controller*

2) Block Transfer from memory will be beneficial due to which of the following? **1 point**

- Spatial Locality
- Lesser Memory Latency
- Paging
- All of the above

### Accepted Answers:

*All of the above*

3) The presence of a page in a cache is detected by checking the **1 point**

- Valid bit
- Dirty bit
- Tag bit
- None of the above

### Accepted Answers:

*Tag bit*

4) In a n-way set associative cache with  $n \ll$  total number of cache lines, a given page can be **1 point** present in any of the cache lines.

- True
- False

## Week 12

**Accepted Answers:***False*5) To check a n-way set associative cache for a given page, the process needs to check **1 point**

- All the cache lines
- one cache line
- n cache lines
- Cannot be predicted

**Accepted Answers:***n cache lines*6) The problem of cache incoherency happens when **1 point**

- The modified value in cache is not reflected in the RAM
- The modified value in cache is reflected in the current core, but not in other cores
- The value in RAM has been modified by some core, but is not reflected in the cache,
- All of the above

**Accepted Answers:***All of the above*7) A modified value is simultaneously modified in a write-through cache **1 point**

- True
- False

**Accepted Answers:***True*8) A modified value is simultaneously modified in a write-back cache **1 point**

- True
- False

**Accepted Answers:***False*9) Split Caches are required for **1 point**

- Larger Cache Sizes
- Concurrent Instruction and Data Access
- managing multiple instruction fetches
- None of the above

**Accepted Answers:***Concurrent Instruction and Data Access*10) Structural Hazards due to dual ported caches are handled by **1 point**

- Giving preference to read over write
- Write-back caches
- Giving preference to write over read

None of the above

**Accepted Answers:**

*Giving preference to write over read*

11) Round Robin Scheduling is achieved using which of the following Interrupts?

**1 point**

- Timer Interrupt  
 Exception  
 Maskable Interrupt  
 None of the above

**Accepted Answers:**

*Timer Interrupt*

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