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Courses » Embedded Systems-- Design Verification and Test

Announcements **Course** Ask a Question Progress Mentor FAQ

Unit 5 - System-level Design

Course outline

How to access the portal

Introduction and Modeling

Modeling and Synthesis issues

Architectural Synthesis of Hardwares

System-level Design

- System Level Analysis
- Uniprocessor Scheduling – 1
- Uniprocessor Scheduling – 2
- Multiprocessor Scheduling – 1
- Multiprocessor Scheduling – 2
- Quiz : Assignment-4

Temporal Logic

Model Checking

Assignment-4

The due date for submitting this assignment has passed.

As per our records you have not submitted this assignment. **Due on 2018-09-05, 23:59 IST.**

1) Consider a set of 6 tasks, T1 (1, 5), T2 (2, 10), T3 (3, 15), T4 (3, 15), T5 (2, 5), and T6 (1, 2 points 5), to be executed on two unit capacity processors using either Pfair or ERfair scheduling schemes.

Notation: $T_k(e, p)$ denotes a task T_k with execution time “e” and period “p”.

What is the pseudo-deadline of second subtask of task T5 when scheduled using ERfair?

- 5
- 8
- 10
- 7

No, the answer is incorrect.
Score: 0

Accepted Answers:
5

2) Consider a set of 7 tasks, T1 (3, 10), T2 (10, 20), T3 (10, 20), T4 (6, 10), T5 (5, 10), T6 (8, 2 points 20), and T7 (2, 10) to be executed on three unit capacity processors using DPfair scheduling scheme.

Notation: $T_k(e, p)$ denotes a task T_k with execution time “e” and period “p”.

What is the workload of task T6 for the first time-slice?

- 5
- 6
- 3
- 4

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ce De processing using "Earliest Deadline First" scheduling scheme.

JOB ID	Arrival Time	Computation Time	Absolute Deadline
J1	0	10	33
J2	4	3	28
J3	5	10	29

What is the response time of job J1, J2 and J3, respectively?

0, 4, 5
 10, 3, 10
 23, 3, 12
 33, 28, 29

No, the answer is incorrect.
Score: 0

Accepted Answers:
23, 3, 12

4) Time taken by a task instruction can depend on whether: **2 points**

1. branch prediction was correct or wrong
2. interrupt occurs from a peripheral device
3. there is a hit or miss in the instruction cache
4. resource contention occur with other executing tasks

1 and 2
 2 and 4
 1 and 3
 3 and 4

No, the answer is incorrect.
Score: 0

Accepted Answers:
1 and 3

5) Consider a uniprocessor system processing three (implicit-deadline) periodic tasks T1, T2, **2 points** and T3, respectively. The task parameters are listed in the following table.

Task ID	Arrival Time	Computation Time	Period
T1	0	20	100
T2	0	40	150
T3	0	100	350

This task set is _____ under Rate-Monotonic (RM), and _____ under Earliest-Deadline First (EDF) algorithms?

Schedulable, Unschedulable
 Schedulable, Schedulable

- Unschedulable, Unschedulable
- Unschedulable, Schedulable

No, the answer is incorrect.

Score: 0

Accepted Answers:

Unschedulable, Unschedulable

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