





Embedded Systems-- Design Verification and Tes...

ed	JOB ID	Arrival Time	Computation Time	Absolute Deadline	
are	J1	0	10	33	
- II	J2	4	3	28	
s in	J3	5	10	29	
e		e time of job J1, J2 and	J3, respectively?		
; in d	0, 4, 5				
	0, 3, 10				
e II	23, 3, 12				
ting for bedded tware tems	33, 28, 29				
	No, the answer is incorrect. Score: 0				
	Accepted Answers:				
	23, 3, 12				
	, ,	task instruction can dep			
		ction was correct or wro urs from a peripheral de	-		
		or miss in the instruction			
	4. resource con	tention occur with other	executing tasks		
	1 and 2				
	2 and 4				
	1 and 3				
	3 and 4				
	No, the answer is incorrect. Score: 0				
	Accepted Answers: 1 and 3				
	5) Consider a uniprocessor system processing three (implicit-deadline) periodic tasks T1, T2,				

5) Consider a uniprocessor system processing three (implicit-deadline) periodic tasks T1, T2, **2** points and T3, respectively. The task parameters are listed in the following table.

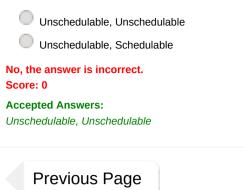
Task ID	Arrival Time	Computation Time	Period
T1	0	20	100
T2	0	40	150
T3	0	100	350

This task set is ______ under Rate-Monotonic (RM), and ______ under Earliest-Deadline First (EDF) algorithms?

Schedulable, Unschedulable

Schedulable, Schedulable

Embedded Systems-- Design Verification and Tes...



End