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Courses » Embedded Systems-- Design Verification and Test

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# Unit 3 - Modeling and Synthesis issues

## Course outline

How to access the portal

Introduction and Modeling

Modeling and Synthesis issues

- Modeling Techniques – 2
- Hardware/Software Partitioning - 1
- Hardware/Software Partitioning - 2
- Introduction to Hardware Design
- Quiz : Assignment-2

Architectural Synthesis of Hardwares

System-level Design

Temporal Logic

Model Checking

BDD and Symbolic Model

## Assignment-2

The due date for submitting this assignment has passed. As per our records you have not submitted this assignment. **Due on 2018-08-22, 23:59 IST.**

1) Consider the transition diagram of DES G1 and G2 shown in the figure. 2 points



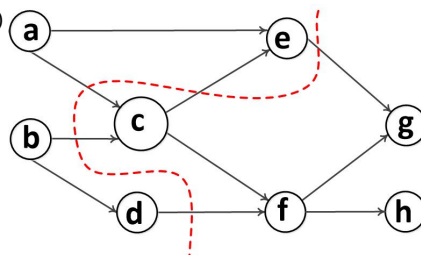
Compute the synchronous parallel composition of G1 and G2. The total number of (reachable / accessible) states in the composite model G1||G2 is:

- 6
- 9
- 5
- 4

No, the answer is incorrect. Score: 0

Accepted Answers: 5

2) 2 points



Consider the task graph shown above in which all edges are of unit cost. An initial hardware-software partition for the task graph is also shown through the cut line. With this as an input, a correct enumeration of the vertices on each side of the partition after the second iteration of the inner repeat



- Hardware Testing

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- Embedded System Hardware Testing - II

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- Advances in Embedded System Hardware Testing

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- Advances in Embedded System Hardware Testing - II

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- Testing for Embedded Software Systems

**No, the answer is incorrect.**  
**Score: 0**  
**Accepted Answers:**  
*Partition-1: a, c, e, g; Partition-2: b, d, f, h*

3) For Question 2, the absolute gain (g) at the end of the third iteration is: **2 points**

-2  
 2  
 -1  
 1

**No, the answer is incorrect.**  
**Score: 0**  
**Accepted Answers:**  
 -2

4) RTL (Register Transfer Logic) design is obtained as an output of the \_\_\_\_\_phase **2 points**

Architectural Synthesis  
 Logic Synthesis  
 Geometrical Synthesis  
 High-Level Synthesis

**No, the answer is incorrect.**  
**Score: 0**  
**Accepted Answers:**  
*Architectural Synthesis*  
*High-Level Synthesis*

5) Registers are connected to functional units via \_\_\_\_\_ and functional units are connected to registers via \_\_\_\_\_ **2 points**

MUXs, DMUXs  
 DMUXs, MUXs

**No, the answer is incorrect.**  
**Score: 0**  
**Accepted Answers:**  
*MUXs, DMUXs*

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