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Courses » Computer Organization and Architecture A Pedagogical Aspect

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Unit 8 - Week 7: Organization and Optimization of Micro-programmed Controlled Control Unit

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Course outline

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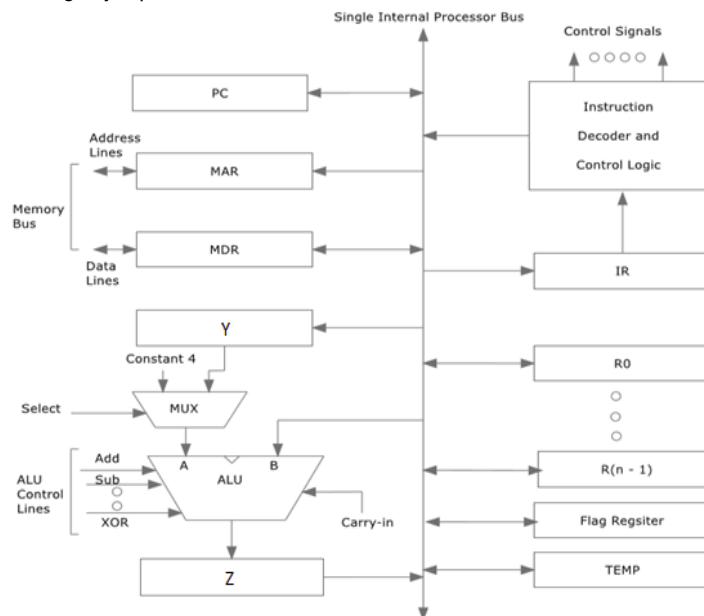
Assignment for Week 7

The due date for submitting this assignment has passed.

As per our records you have not submitted this
assignment.

Due on 2019-03-20, 23:59 IST.

1) For a CPU with single bus organisation as shown below, the control steps for completely
executing a "jump on Zero" instruction "JMPZ 3000" are: **1 point**



- 1) PCout , MARin , Read, Select=0, Add, Zin
- 2) Zout , PCin , Yin, WMFC
- 3) MDRout, IRin

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Organization and Optimization of Micro-programmed Controlled Control Unit

Handling Different Addressing Modes

Handling Control Transfer Instructions

Design of Hardwired controlled Control Unit

Quiz : Assignment for Week 7

Week 8: Organization and Optimization of Micro-programmed Controlled Control Unit

Week 9: Memory Sub-system Organization

Week 10: Memory Sub-system Organization

Week 11: Memory Sub-system Organization

Week 12: Input/output Subsystem

TEXT TRANSCRIPTS

5) Zout, PCin

- 1) PCout , MARin, Read, Select=0, Add, Zin
- 2) Zout , PCin , WMFC
- 3) MDRout, IRin
- 4) IRout, R1in

- 1) PCout , MARin, Read, Select=0, Add, Zin
- 2) Zout , PCin , Yin, WMFC
- 3) MDRout, IRin
- 4) Offset-field-of-IRout, Select=1, Add, Zin, If Zero Flag!=0 then END
- 5) Zout, PCin

No, the answer is incorrect.

Score: 0

Accepted Answers:

- 1) PCout , MARin, Read, Select=0, Add, Zin
- 2) Zout , PCin , Yin, WMFC
- 3) MDRout, IRin
- 4) Offset-field-of-IRout, Select=1, Add, Zin, If Zero Flag!=0 then END
- 5) Zout, PCin

2) For a CPU with single bus organisation shown in question 1, the control steps for completely executing a "jump on negative" instruction "BRN 3000" are:

1 point

- 1) PCout , MARin, Read, Select=0, Add, Zin
- 2) Zout , PCin , Yin, WMFC
- 3) MDRout, IRin
- 4) Offset-field-of-IRout, Select=1, Add, Zin, If Sign Flag!=1 then END

- 1) PCout , MARin, Read, Select=0, Add, Zin
- 2) Zout , PCin , Yin, WMFC
- 3) MDRout, IRin
- 4) Offset-field-of-IRout, Select=1, Add, Zin, If Sign Flag!=0 then END
- 5) Zout, PCin

- 1) PCout , MARin, Read, Select=0, Add, Zin
- 2) Zout , PCin , Yin, WMFC
- 3) MDRout, IRin
- 4) Offset-field-of-IRout, Select=1, Add, Zin, If Sign Flag!=1 then END
- 5) Zout, PCin

None of the above

No, the answer is incorrect.

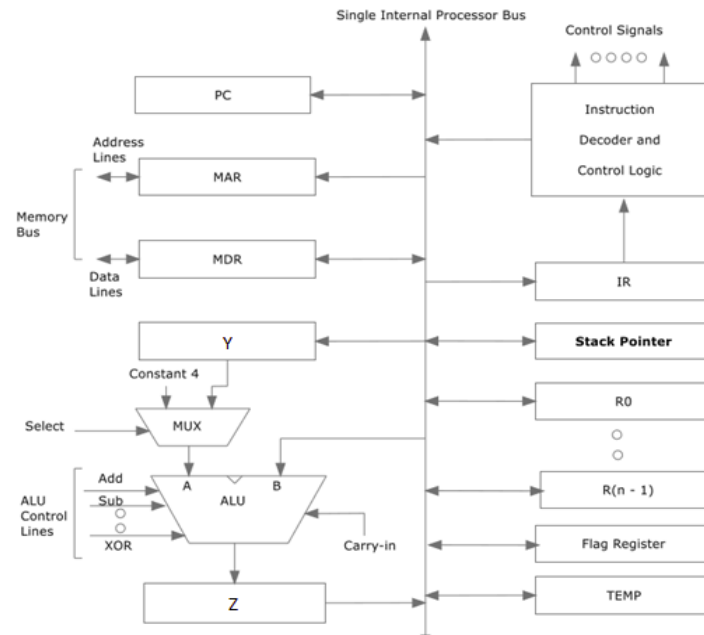
Score: 0

Accepted Answers:

- 1) PCout , MARin, Read, Select=0, Add, Zin
- 2) Zout , PCin , Yin, WMFC
- 3) MDRout, IRin
- 4) Offset-field-of-IRout, Select=1, Add, Zin, If Sign Flag!=1 then END
- 5) Zout, PCin

3) For a CPU with single bus organisation shown below, the control steps for completely executing a "CALL FUNC" instruction are:

1 point



1. PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , Yin, WMFC
3. MDRout, IRin
4. SPout, MARin, Write
5. WMFC, Offset-field-of-IRout, Select=1, Add, Zin
6. Zout, PCin

1. PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , Yin, WMFC
3. MDRout, IRin
4. PCout , MDRin
5. SPout, MARin, Write
6. WMFC, Offset-field-of-IRout, Select=1, Add, Zin
7. Zout, PCin

1. PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , Yin, WMFC
3. MDRout, IRin
4. PCout , MDRin
5. WMFC, Offset-field-of-IRout, Select=1, Add, Zin
6. Zout, PCin

☐ None of the above

No, the answer is incorrect.

Score: 0

Accepted Answers:

1. PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , Yin, WMFC
3. MDRout, IRin
4. PCout , MDRin
5. SPout, MARin, Write
6. WMFC, Offset-field-of-IRout, Select=1, Add, Zin
7. Zout, PCin

4) For a CPU with single bus organisation shown in question 3, the control steps for

1 point

completely executing a "RETURN" (from function FUNC from question 3) instruction are:



1. PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , Yin, WMFC
3. MDRout, IRin
4. PCout, MARin, Read
5. WMFC
6. MBRout, PCin



1. PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , Yin, WMFC
3. MDRout, IRin
4. IRout, MARin, Read
5. WMFC
6. MBRout, PCin



1. PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , Yin, WMFC
3. MDRout, IRin
4. SPout, MARin, Read
5. WMFC
6. MBRout, PCin



None of the above

No, the answer is incorrect.

Score: 0

Accepted Answers:

1. PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , Yin, WMFC
3. MDRout, IRin
4. SPout, MARin, Read
5. WMFC
6. MBRout, PCin

5) Consider the instruction "LOAD R1, M" (Data from memory location M is loaded to register R1). We assume that length of instruction is 1 (constant). The first two control steps used to fetch the instruction "LOAD R1, M" (question 1) are given below

1. PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , WMFC

After step-1	
Register	Value
PC	X
MAR	X
MDR	-

After step-2	
Register	Value
PC	--
MAR	--
MDR	--

The values in the PC, MAR and MDR after Step 1 is shown above. What are the values of PC, MAR and MDR after Step 2?



PC = X; MAR = X+1 ; MDR = LOAD R1, M;



PC = X+1; MAR = X ; MDR = LOAD R1, M;



PC = X; MAR = X ; MDR = LOAD R1, M;



None of the above

No, the answer is incorrect.

Score: 0

Accepted Answers:

$PC = X+1; MAR = X; MDR = LOAD \ R1, M;$

6) Which of the following options represents the action of the 1st control step in question 5 in the best manner? **1 point**

- ☐ Program counter value is assigned to the memory buffer register
- ☐ The memory buffer register waits for memory read operation to be completed
- ☐ The memory address register waits for memory read operation to be completed
- ☐ None of the above

No, the answer is incorrect.

Score: 0

Accepted Answers:

None of the above

7) Three control steps (after fetch) are required to execute the instruction "LOAD R1, M" (question 1). Which of the following options describe that sequence of control steps? **1 point**

- ☐
 1. IRout, MARin, Read
 2. WMFC
 3. MDRout, R1in
- ☐
 1. WMFC
 2. IRout, MARin, Read
 3. MDRout, R1in
- ☐
 1. WMFC
 - 2.. MDRout, R1in
 3. IRout, MARin, Read

- ☐
 1. IRout, MARin, Read
 2. WMFC
 3. MDRin, R1out

No, the answer is incorrect.

Score: 0

Accepted Answers:

1. IRout, MARin, Read

2. WMFC

3. MDRout, R1in

8) Consider the indirect addressing mode instruction "Load R1, (M)". **1 point**

Task of the instruction: Load the content of Memory Location M1 to Register R1. There are five control steps (after fetch) that are required to execute the instruction "LOAD R1, (M)", as shown below.

1. -----
2. WMFC
3. MDRout, MARin
4. WMFC
5. MDRout, R1in

Which of the following describes most appropriately, the step marked above with-----?

- ☐ MDRin, MARout
- ☐ Zout, PCin, WMFC

☐ Zout , PCin

☐ IRout, MARin, Read

No, the answer is incorrect.

Score: 0

Accepted Answers:

IRout, MARin, Read



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