X

Unit 7 - Week 6: Organization and Optimization of Micro-programmed Controlled Control Unit

Register for Certification exam

Course outline

How to access the portal

Week 1: Fundamentals of Digital Computer

Week 2: Fundamental of Digital Computer

Week 3: Addressing Modes, Instruction Set and Instruction Execution Flow

Week 4: Addressing Modes, Instruction Set and Instruction Execution Flow

Week 5: Addressing Modes, Instruction Set and Instruction Execution Flow

Week 6:

Assignment for Week 6

The due date for submitting this assignment has passed.
As per our records you have not submitted this assignment. **Due on 2019-03-13, 23:59 IST.**

1) The clock-cycle grouping in the fetch cycle could *1 point*

- Avoid conflicts between operations
- Maintain the proper sequencing of instructions
- Save time for the fetch cycle
- All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
All of the above

2) Which of the following is NOT a micro-operation? *1 point*

- Register transfer
- Arithmetic
- Loop
- Shift

No, the answer is incorrect.
Score: 0

Accepted Answers:
Loop

3) The fetch cycle consists of 4 micro-operations given below *1 point*

t1: ----------
t2: MEMORY → MBR

- PC → PC+1
- PC → MBR
- PC → IR

No, the answer is incorrect.
Score: 0

Accepted Answers:
PC → MAR

4) Which of the following is TRUE? ***1 point***

- In micro-programmed control unit, the logic of the control unit is specified in a memory.
- Hardware control unit is slower in execution compared to micro-programmed control unit.
- For some control signal sequence there cannot be any Hardware control unit.
- For some control signal sequence there cannot be any micro-programmed control unit

No, the answer is incorrect.
Score: 0

Accepted Answers:
In micro-programmed control unit, the logic of the control unit is specified in a memory.

5) Which micro-operation must be executed at time step t3 for an interrupt cycle shown below? ***1 point***

t1 : MBR <- PC
t2 : MAR <- Address to save the contents of PC
PC <- Address of start of interrupt service routine
t3 : ----------

- MAR <- PC
- Memory <- MBR
- Memory <- MAR
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
Memory <- MBR

6) The 4 micro-operations of an instruction fetch cycle are shown below. Which of the following clock cycle groupings are possible? ***1 point***

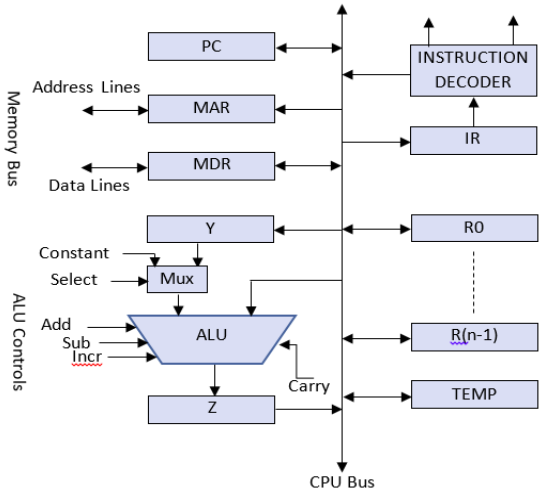
$t_1 : PC \rightarrow MAR$
$t_2 : MEMORY \rightarrow MBR$
$t_3 : PC + 1 \rightarrow PC$
$t_4 : MBR \rightarrow IR$

- t1 & t2
- t2 & t3 OR t3 & t4
- t2 & t4 OR t3 & t4
- All of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
t2 & t3 OR t3 & t4

7) The block diagram of a CPU with single bus organization is given below. ***1 point***



which of the following control steps are required to execute the instruction “ST R1, 32” (store the content of R1 at memory location 32)?

1. IRout, MARin
2. MDRin, R1out, Write
3. MDRout, WMFC

1. WMFC
2. IRout, MARin, Write
3. MDRout, R1in

1. WMFC
2. MDRout, R1in
3. IRout, MARin, Write

1. IRout, MARin, Read
2. MDRin, WMFC
3. MDRout, R1in

No, the answer is incorrect.
Score: 0

Accepted Answers:
1. IRout, MARin
2. MDRin, R1out, Write
3. MDRout, WMFC

8) The first three steps used to fetch the instruction “ADD R1, R2” (In the CPU with single bus organization shown in question 7) are given below ***1 point***

1. PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , WMFC
3. MDRout, IRin

After step-1	
Register	**Value**
PC	X
MAR	X
MDR	-
IR	-

After step-2	
Register	**Value**
PC	X+1
MAR	X
MDR	ADD R1, R2.
IR	-

After step-3	
Register	**Value**
PC	------
MAR	------
MDR	ADD R1, R2.
IR	-----

The values in the PC, MAR, MDR and IR after Step 1 and Step 2 are shown above. What are the values of PC, MAR and IR after Step 3?

- PC = X+1; MAR = X ; IR= ADD R1, R2.;
- PC = X+1; MAR =X+1 ; IR = ADD R1, R2.;
- PC = X; MAR =X ; IR = ADD R1, R2;
- None of the above

No, the answer is incorrect.
Score: 0

Accepted Answers:
PC = X+1; MAR = X ; IR= ADD R1, R2.;

9) What is the 6th control step involved in completely executing the instruction “”ADD R1, R2”” ***1 point*** (in the CPU with single bus organization shown in question 7)?
1.PCout , MARin, Read, Select=0, Add, Zin
2. Zout , PCin , WMFC
3. MDRout, IRin
4. R2out, Yin
5. R1out, Select=1, Add, Zin
6._____

- Zin, R1in
- MDRout, R1in
- Yin, R1in
- Zout, R1in

No, the answer is incorrect.
Score: 0

Accepted Answers:
Zout, R1in

Previous Page End